Afroz Ali Shaik¸ U Yedukondalu / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 4, Jul-Aug 2013, pp.662-666

A Lower Power, Low Complexity And Memory Free Implementation Of Novel Recursive DFT And IDFT Algorithms

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Abstract—

A Recursive Discrete Fourier Transforms (RDFT) design is proposed in this project. The proposed algorithm reduces the number of multiplications and additions considerably in comparison with the existing techniques. Proposed algorithm reduces multiplication by 74% and additions by 73% compared to the latest RDFT algorithms. By this a considerable power saving is achieved. Also this design can shorten the computation time. In addition the proposed algorithm doesn't use big memories, Proposed design requires only 2 multipliers and 12 adders hence it is memory free. The architecture will be developed low-computational, complexity and low-cost keeping DTMF requirements in consideration. The proposed algorithm will be implemented through VHDL after verifying the simulation results the code will be synthesized on Xilinx FPGA. For computing the 212 and 106 point DFT coefficients, the proposed algorithm can reduces computing cycles by 47% compared to latest architectures.

Index Terms-- Dual-Tone Multi frequency (DTMF), Discrete Fourier transform (DFT), Recursive Discrete Fourier transform (RDFT), Recursive filters.

I. INTRODUCTION

The Discrete Fourier transform (DFT) has been widely applied in the field of signal processing. However in some applications we need to compute the DFT for some of selected output bin indices only. One of such example is signal monitoring and spectrum estimation technique in signal intelligence applications. The Dual-tone multi-frequency (DTMF) is also another example where specifically interested to see the energies at specific frequency values only.

Well-known methods such as the prime-factor DFT algorithms and the prime-factor DCT/discrete sine transform algorithms have been presented over the past three decades. Recently, have proposed the mixed prime-factor DFT algorithm with the Chinese remainder theorem (CRT) to solve the problem of frame size un supporting the radix-2n DFT and to reduce the number of multiplications. However, their design has higher hardware costs for implementing the non-radix 2n DFT circuit. An efficient solution is suggested adopting Recursive Architecture instead of parallel DFT architecture. In this way, the hardware costs can be reduced greatly. In this brief, we present a novel architecture and a fast algorithm using a simple hardware based on our previous works. The results show that the proposed method reduces the computational complexity of the RDFT greatly. The rest of this brief is organized as follows: version 2 presents the low-cost and low-complexity DFT and inverse DFT (IDFT) computations. Below compares and contrasts the differences in performance between the proposed recursive design and other designs. Finally, conclusions are discussed in results.

Dual-tone multi-frequency (DTMF) approaches to the voice-over-packet (VoP) network [3] use Goertzel's algorithm [4] to compute the interested frequency. To meet the International Tele communications Union frequency specifications [5], Felder *et al* suggest using two different frame sizes for both the high group (a frame size of 212) and low-group (a frame size of 106) frequency specifications.

These architectures for recursive DFT (RDFT) algorithms have been completely developed and have the advantages of high data throughput, low power use, and small area requirement compared to digital-signal-processing-based designs. However, the computational complexities (multiplications and additions) of these RDFT algorithms [6]–[21] are quite high; thus, a low-cost and low-computational-complexity version of the RDFT algorithm should be developed and explored. Recently, Lai et al. [10] have proposed a novel RDFT algorithm for computing arbitrary-length DFTs. The computational complexity of this algorithm is still high, although the design does have low-cost and low-complexity advantages compared with other RDFTs. Lei and Yao proposed a memory-free method to reduce the chip area and coefficient requirements in hardware implementation of variable-length MDCTs. In order to reduce the coefficient requirements to meet the variable- length computations, a memory-free algorithm must be developed.

In this brief, we present a novel architecture and a fast algorithm using a simple hardware. The results show that the proposed method reduces the computational complexity of the RDFT greatly. The rest of this brief is organized as follows represents

the low-cost and low-complexity DFT and inverse DFT (IDFT) computations. Below compares and contrasts the differences in performance between the proposed recursive design and other designs. Finally results and conclusions are discussed.

II. PROPOSED LOW-COST RDFT AND IDFT ALGORITHMS

A. *RDFT Algorithme*

The Discrete Fourier Transform converts discrete data from a time wave into a frequency spectrum. Using the DFT implies that the finite segment that is analyzed is one period of an infinitely extended periodic signal.

The proposed technique in paper describes the usage of two DFT point computations that are 106 and 212. But we can implement the DFT with N= 212 for all 8 different frequencies detection in DTMF applications which is more resolution wise better than 106 point DFT. Hence we implemented the first version of the DTMF detection with 8 parallel detectors each containing the above architecture.

The DFT formula can be derived as follows by reordering the index and expressing the sigma function:

$$X[k]=\sum_{n=0}^{N-1} x[n]\times W_N^{nk}$$

$$=\sum_{n=N-1}^{0} x[N-1-n]\times W_N^{(N-1-n)k}$$

$$=W_N^k\left(x[N-1]+W_N^k.x[N-2]+W_N^{2k}.x[N-3]+\ldots+W_N^{(N-2)k}.x[0]\right)$$

$$\cdots\cdots\cdots\cdots(1)$$

Then, it yields a recursive form as follows:

$$x[k]=W_N^{-k}.(W_N^{-k}.(W_N^{-k}.(W_N^{-k}.(W_N^{-k}\ldots\ldots.W_N^{-k}.(W_N^{-k}.x[0]+x[1])$$
$$x[2])+x[3])+\cdots+x[N-1])\cdots\cdots\cdots$$

(2)

The kernel function of the difference equation is defined as

$$m[n]=W_N^{-k}(m[n-1]+x[n])\ldots\ldots(3)$$

$$m[n]=W_N^{-k}(W_N^{-k}(m[n-2]+x[n-1])+x[n])$$

The function *m* of *n* is derived as follows via (2) and (3), and then the output of *X*[*k*] will be obtained at time $n = N - 1$:

$$X[k]=m[N-1]\ldots\ldots(4)$$

This means that the proposed algorithm uses the number of *N* iterative cycles for the whole DFT calculation. Now, the difference equation (4) can be expressed as a *z*-transform.

The transfer function *H*(*z*) is obtained as

$$\frac{M(z)}{X(z)}=H(z)$$

$$=\frac{W_N^{-k}}{1-W_N^{-k}z^{-1}}$$

$$=\frac{W_N^{-k}(1-W_N^{k}z^{-1})}{1-2\cos\theta(k)z^{-1}+z^{-2}}$$

$$=\frac{\cos\theta(k)+j\sin\theta(k)-z^{-1}}{1-z^{-1}(2\cos\theta(k)-z^{-1})},\ where\ \theta(k)=\frac{2k\pi}{N}$$

…….(5)

According to (4) and (5), it is easily mapped into a novel algorithm. To reduce the number of multiplications of $cos\ \theta\ (k)$ in the implementation, the coefficients of $cos\ \theta\ (k)$ and $2^{cos\ \theta\ (k)}$ can be shared. Then, all multiplications can be calculated using one real multiplier.

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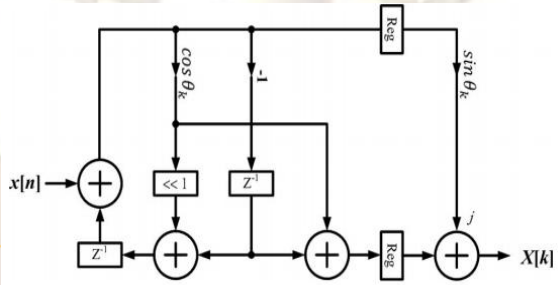


Figure 1 Novel RDFT algorithm with a multiplier-sharing scheme.

The above figure is the corresponding second order recursive calculation flow. Here, it is apparently that Goertzel algorithm only needs two real multiplications and four real additions to pick up the amplitude of the specified frequency component.

The Sharing multiplayers and adders reduce the complexity of design. Design with low complexity leads to a design which is low power consumption and memory free implementation. block Recursive DFT

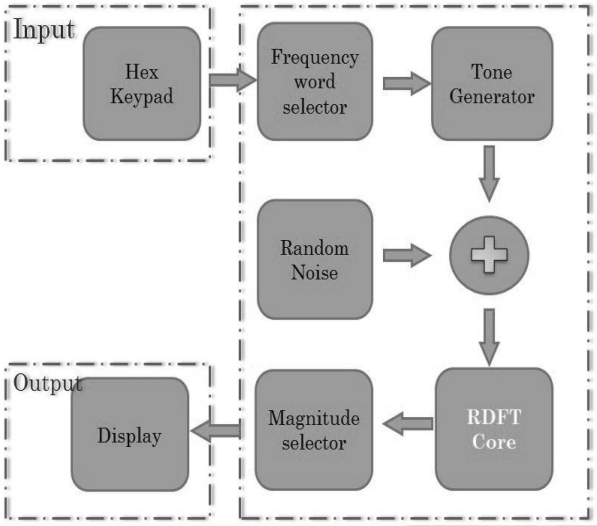


Figure 2 Block Diagram.

B. Recursive IDFT Formula

The IDFT of an N-point input sequence X[k] is defined as

$$x[n] = \frac{1}{N}\sum_{k=0}^{N-1} X[k] \times W_N^{-nk} \quad \ldots (6).$$

Where n=0 to N-1

The efficient computational algorithm caused by the DFT and the IDFT involves the same kernel. After taking the complex

$$x^*[n] = \frac{1}{N}\sum_{k=0}^{N-1} X^*[k] \times W_N^{-nk}$$

It can be seen that the IDFT can be performed by the DFT. The only difference is in the complex conjugate of the input/output sequence. In summary, there are three steps to achieving the recursive IDFT: First, take the complex conjugate of the input sequence. Then, apply the proposed DFT algorithm. Finally, take the complex conjugate of the output sequence and divide it by *N*. Conjugate of (13), the same kernel can be obtained,

Table II Shows the amount of memory required to store the sine and cosine coefficients of the proposed algorithm compared with others with 212- and 106-point frames. The results show that the proposed algorithms required the least amount of memory to implement the RDFT algorithm. Regarding our previous work [10], the amounts of coefficient requirements based on [10] are totally equal to (*N* - 2) words.

Table I
Coefficients required for various DFT Algorithms

Algorithms	Multiplier	Adder	ROM	Critical Period*
[4]	6	8	636	T_m+3T_a
[7]	4	8	636	T_m+2T_a
[8]	10	17	318	T_m+2T_a
[21]	N+4	N+18	260	T_m+T_a
[10]	2	13	314	T_m+2T_a
Proposed	2	12	0	T_m+2T_a

After we estimated the number of coefficient requirements of Meher *et al.* [21] based on Fig. 5 in their paper, it was found that the number of coefficients was totally equal to (1.25*N* - 5) words. Thus, the total memory requirements of Meher *et al.* [21] and the previous work [10] are 260 and 314 words, respectively.

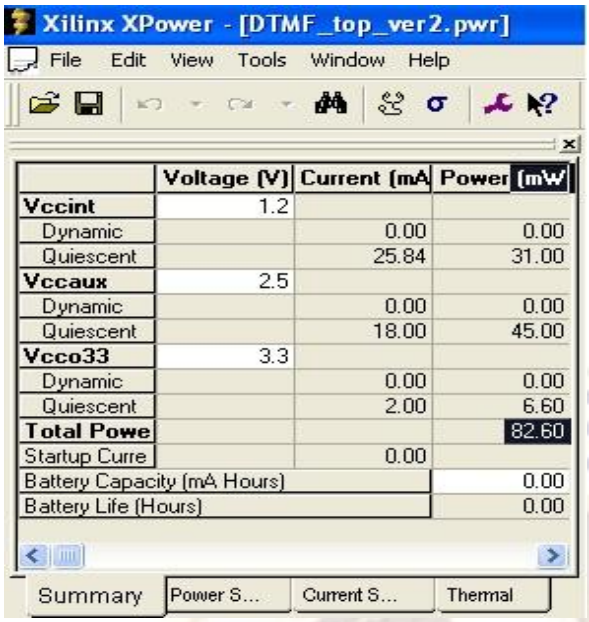
Compares hardware costs for various RDFT algorithms. The proposed design only requires 2 multipliers and 12 adders less than others. The coefficient-ROM storing the sine and cosine values for the proposed algorithm can be 100% smaller than those needed for other recursive algorithms [4]– [21]. For critical period comparison, the proposed algorithm and Va n *et al.*'s [7] and [8] taking one T_m and two T_a are shorter than those of [4] and [6]. Therefore, the proposed architecture is more suitable for VLSI implementation than previous works.

A bit-level SNR simulation was employed to compare the proposed algorithm with other RDFT approaches [4], [8], [10] for hardware accuracy analysis. The parameters were set as follows: 1) 16-bit input word length; 2) internal word length ROM 16–24 bits, where the word length of the integer is 6 bits, and the word length of the fraction is from 9 to 17 bits;

Table II

FPGA Device	Altera EP2S60F 1020C5
Combinational ALUTS	780 / 48,352 (2%)
Dedicated local registers	780 / 48,352 (2%)
Total Block memory bits	0 / 2,544,192 (0%)
DSP block 9-bit elements	16 / 288 (6%)
Max. clock rate	69.31 MHz

Modelsim Xilinx Edition (MXE) and Xilinx ISE will be used for simulation and synthesis respectively. The Xilinx Chipscope tool will be used to test the FPGA inside results while the logic running on FPGA. Xilinx Xpower tool will be used for power analysis of the implemented FPGA based core.



III. CONCLUSION

This brief has presented low-complexity low-cost fast-computing architecture for RDFT and IDFT algorithms. The proposed algorithm and architecture not only outperform previous works but can also be implemented using simple hardware. This design is suitable for DTMF detecting in VoP applications.

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