Don P John / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 4, Jul-Aug 2013, pp.655-661

High Frequency 32/33 Prescalers Using 2/3 Prescaler Technique

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ABSTRACT

Frequency synthesizer is one of the important element for wireless communication application. The speed of VCO and prescaler determines how fast the frequency synthesizer is. A dual modulus prescaler contains logic gates and flip-flops. To fulfill the need of high frequency and low voltage circuit suitable flip-flops must be selected. Four different classes of flip-flops like master-slave, pulse-triggered, differential and dual-edge triggered (DET) are analyzed. Higher clock load in pulse-triggered FF and switching on both side of clock cycle in DET made them unusable in practical design for prescaler circuits. Due to this reason dual-edge triggered and pulse-triggered flip-flops are not taken for the comparison. Divide-by-2/3 prescaler is implemented by TSPC, ETSPC master-slave and differential type of flip-flops. Different 32/33 prescalers are implemented by choosing various combinations of 2/3 prescaler and flip-flops. Prescalers using different FFs are compared in terms of operating frequency, power, delay and power-delay-product. The operations of prescalers are ensured in cadence virtuoso simulator under 180nm technology.

Keywords **-** D flip-flop (DFF), extended TSPC (ETSPC), frequency divider, operating frequency, power-delay-product (PDP), prescaler, stacked structure.

I. INTRODUCTION

Frequency division is one of the important applications of flip-flops. A wide-band frequency synthesizer implemented by phase-locked loop (PLL) uses prescaler (also called N/N+1 counter) as fundamental block. In PLL high frequency output of VCO is coupled directly to the prescaler directly [1]. As process technology is reducing, channel length and supply voltage is decreasing rapidly. Therefore prescaler has to work at high frequency as well as low operating voltage. Due to incorporation of additional logic gates between the flip-flops to achieve the two different division ratios, the speed of the prescaler is affected by creating another propagation delay and the increases the switching power. Since flip-flop works as a part of the clock network, it consumes 30-50% of chip energy [2], [3]. This creates an importance in the selection of various flip-flop designs and way in which logic gates are incorporating.The NORA technique [4], an extensive no-race approach and domino technique [5] associated successfully both two-phase and dynamic CMOS circuits are some of the earliest techniques used for clocking strategies. Later a true-single-phase-clock (TSPC) policy was introduced [6]. Single-phase-clock policies are superior to the others due to the simplification of the clock distribution on the chip and reducing the transistor number. They reduce the number of clock-signal requirements and the wiring costs also they have no problems with phase overlapping. Thus, higher frequencies and simpler designs can be achieved. Further enhancement in the design is achieved by using extended true-single phase clock (ETSPC) FFs, which reduces number of stacked structure in transistor and body effect [7]. They are used for low power and high speed applications [8] and [9].

The simplification of logic part will reduce the circuit complexity and the critical path delay. Many ETSPC designs [10], [11] has come out with embedding one extra pMOS/nMOS transistor can form an integrated function of AND/OR logic and flip-flop. Design in [12] loss their performance advantage when working under low $V_{DD,}$ since it has increased number of transistor stacked connection (up to five and four respectively). By introducing an extra pMOS transistor between V_{DD} and the FF in [13] switch off the unused FF and reduce the power consumption during divide-by-2 mode. In the proposed design ETSPC FFs use only one pass transistor to select the divide control logic. This design is able to work at high frequencies and low voltage compared to other designs. Later a high frequency and low voltage divide-by-32/33 dual-modulus perscaler, which is highly suitable for high resolution fully programmable frequency synthesizer is introduced. The fully programmable divider is accomplished by the Dual modulus prescaler (N/N+1), programmable P and S-counters to achieve the required division ratio determined by (NP+S) in [14] and [15].

II. GENERAL NANOMETER FLIP-FLOPS

A flip-flop is a bistable circuit which stores a logic state of 1 or 0 in response to a clock pulse with one or more data inputs. It is difficult to understand and select the appropriate choice of flip-flop topology for a particular application, since a large number of existing topology and depends on power dissipation, transistor sizing and area exists [16]. Generally there are four different classes of flip-flops such as master-slave, pulse-triggered,

dual-edge triggered and differential flip-flop [16]. Pulse-triggered flip-flops can be classified into two types, implicit and explicit, and this classification is based on the pulse generators they use. In implicit-pulse triggered flip-flops (ip-FF), the pulse is generated inside the flip-flop where in explicit-pulse triggered flip-flops (ep-FF), the pulse is generated externally.

An ideal dual edge-triggered flip-flop allows the same data throughput as a single edge-triggered (SET) flip-flop while operating at half the clock frequency and sampling data on both edges of the clock[17][18]. As per the name master-slave flip-flop contains two parts master and slave where data will capture by master during first half of cycle where slave will hold the previous data at that time. During the second half of period slave will transparent to data which master holds in the first half of period [19]. Differential flip-flop contains differential data inputs which provide both outputs Q and Q_{bar}, which avoids additional inverter delay for complementing the output Q.

Since dual-edge triggered will switch the output at both high to low and low to high, it will give output frequency same as of input frequency. Therefore dual-edge triggered flip-flops cannot use as a frequency divider circuit. Clock signal is the only input of a prescaler circuit. Pulse triggered flip-flops requires an additional clock generating circuit which uses cascaded inverters and NAND gate. This creates large device size and increased clock load which make them to operate at reduced operating frequency and high power. Due to this pulse triggered flip-flops are not using in prescaler circuits. Therefore master-slave and differential flip-flops are better for frequency divider circuits out of the four classes. From master slave flip-flop write port master slave (WPMS) flip-flop [20] is selected since it contain lower number of pMOS transistors, design simplicity and less complex layout with respect to others.

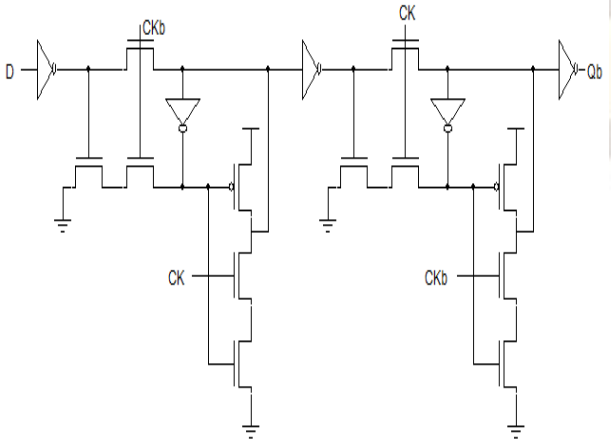

Fig 1: Schematic of WPMS

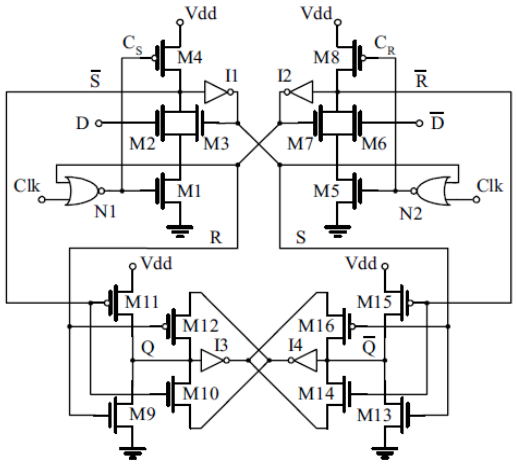

Fig 2: Schematic of STFF

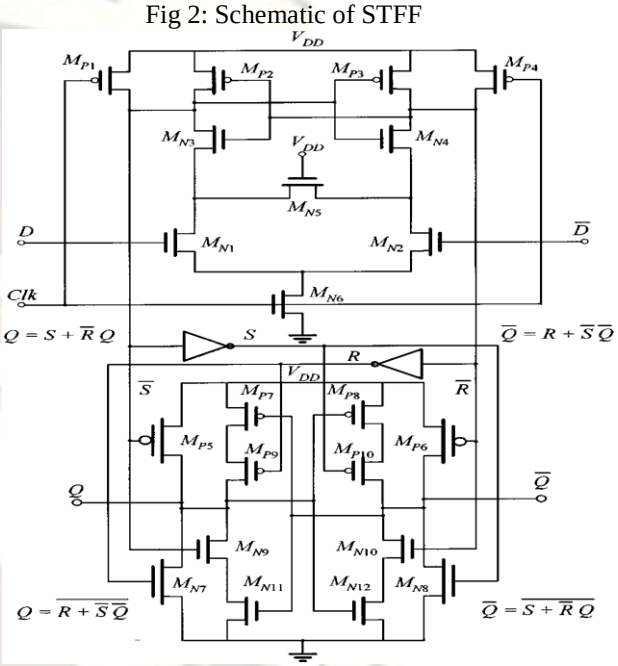

Fig 3: Schematic of MSAFF

Fig 1 and Fig 2 represents the schematic of WPMS and STFF respectively. Fig 3 shows the schematic of MSAFF flip-flop. Since no feedback path exists from output to input modified sense amplifier flip-flop (MSAFF) [21] and skew tolerant flip-flop (STFF) [22] is taken from differential flip-flops due to its simple design regarding the timing parameters.

III. CONVENTIONAL TSPC BASED DIV-BY-2/3 PRESCALER

The TSPC architecture has the advantage of a higher operating frequency compared to that of master-slave and differential flip-flops. Inorder to reduce the power consumption and propagation delay digital gates are embedded into the flip-flops where the conventional 2/3 prescaler consists of an OR gate, AND gate and two D flip-flops [13]. The conventional 2/3 prescaler uses two DFFs where

DFF1 is loaded by an OR gate and DFF2 is loaded by DFF1, an AND gate and an output stage which makes a larger load. This large load on DFF2 causes substantial power dissipation and limits the speed of operation. The difficulty in embedding the OR, AND gates into the DFF introduces additional delay by the digital gates which limits the speed of operation in conventional one. A low power and improved speed 2/3 prescaler implemented in the TSPC logic format is proposed in [13]. Fig 4 shows the new prescaler which uses two embedded NOR gates instead of an OR and an AND gate for the conventional 2/3 TSPC prescaler. This arrangement reduces the number of switching nodes from 12 to 7 and consumes less power compared to the conventional 2/3 prescaler.

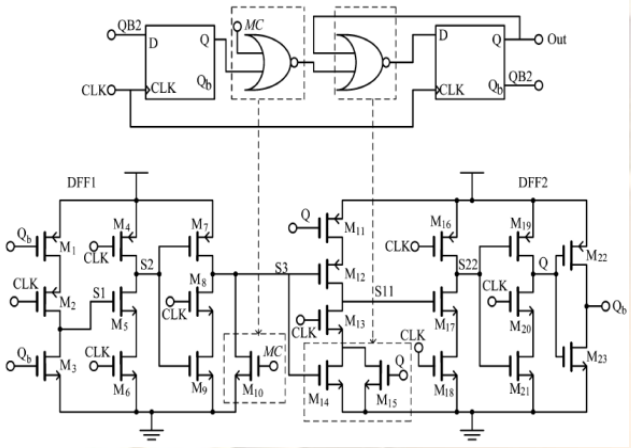

Fig 4: Design-I TSPC 2/3 prescaler circuit and equivalent gate level schematic.

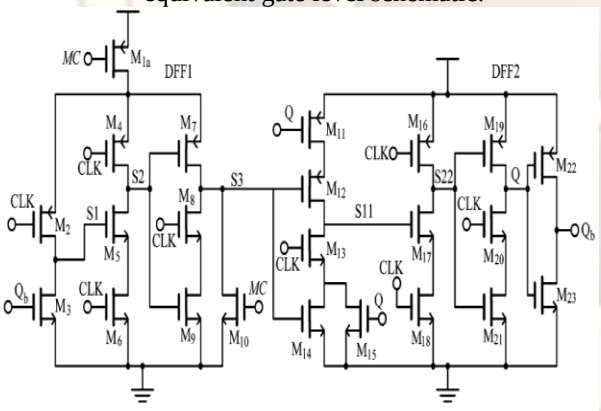

Fig 5: Design-II TSPC 2/3 prescaler

Later an ultra-low power 2/3 prescaler (Design-II) in [13], a further improved version of the Design-I is shown in Fig 5. In this design a pMOS transistor, connected between power supply and DFF1 with the control logic signal MC selects the divide-by-2 or divide-by-3 mode. When MC is logically high DFF1 will disconnected from the power supply and DFF2 alone work to form the divide-by-2 operation. Therefore the short circuit power and switching power of DFF1 is removed. When the control signal MC goes low pMOS transistor will turns on and both flip-flops combine give the divide-by-3 operation. Operating frequency is directly related to the supply voltage. Since due to the Vds drop across transistor M1a, DFF1 operates at a decreased voltage level which limits the maximum operating frequency [13]. However, by decreasing the stacked connection in the first stage of Design-II similar to the design in [10] improves the frequency range to almost same as that of the Design-I.

IV. ETSPC 2/3 PRESCALERS

As a part of increasing operating frequency and reducing supply voltage ETSPC FFs outstand the TSPC FFs. The two major conventional divide-by-2/3 ETSPC designs are in [10] and [11]. Design in [10] causes redundant power consumption in the div-by-2 mode operation. Design in [11] overcomes the toggling of FF1 during divide-by-2 operation by changing the control logic from output of FF1 to its input. But the first stage in design [11] causes larger power consumption. Eventhough both designs are simpler, the inverter between both flip-flops and parallel connected transistor introduce extra delay and larger parasitic capacitance [7]. To prevent these issues a new method is proposed using ETSPC technique.

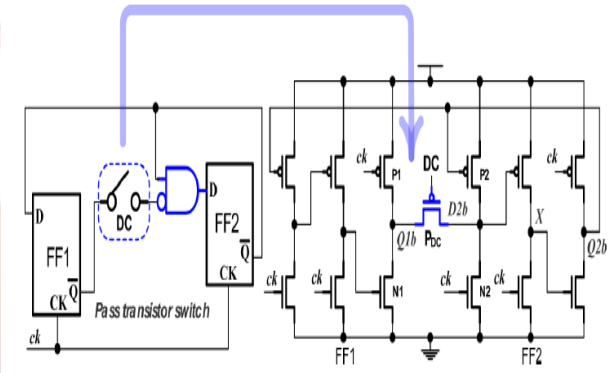

Fig 6: Schematic of proposed E-TSPC based divide-by-2/3 prescaler.

Fig 6 shows the schematic of proposed ETSPC design. The structure shows that output Q_{bar} of FF1 is complemented and given to one of the AND gate's input. The pMOS transistor with input DC acts as a control switch, selects the mode of operation. The proposed method has the advantage of reduced propagation delay by avoiding the inverter implementation between two flip-flops and integrating the logic gates without any extra transistors. When control signal DC is logically high, the FF1 will disconnect from FF2 and it alone does the divide-by-2 operation.

Fig 7 shows prescaler work as a divide-by-2 counter. Alternatively when DC is low pMOS transistor will turn on and both flip-flops are linked to form divide-by-3 operation. Fig 8 shows prescaler functioning as a div-by-3 frequency divider. Besides

the reduction of supply voltage and capacitance load, the proposed prescaler reduces the area since it uses only 13 transistors to perform divide-by-2 or divide-by-3 compared to the conventional prescalers. The minimum height transistor stacked connections create less capacitance load for the previous stage and reduce the dynamic power consumption. However, reduced stacked connection increases short circuit power.

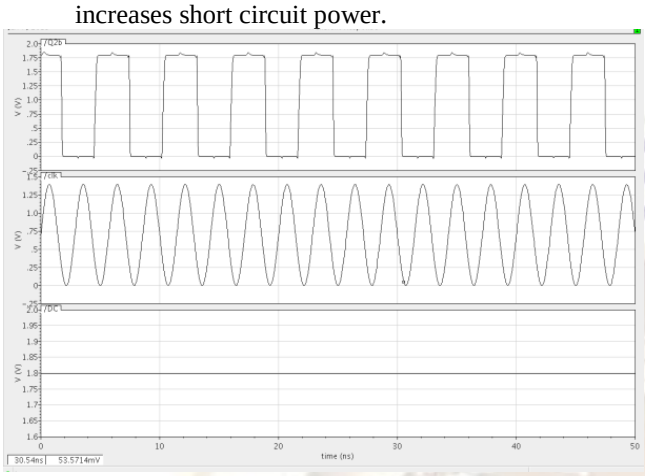

Fig 7: Prescaler at divide-by-2 operation.

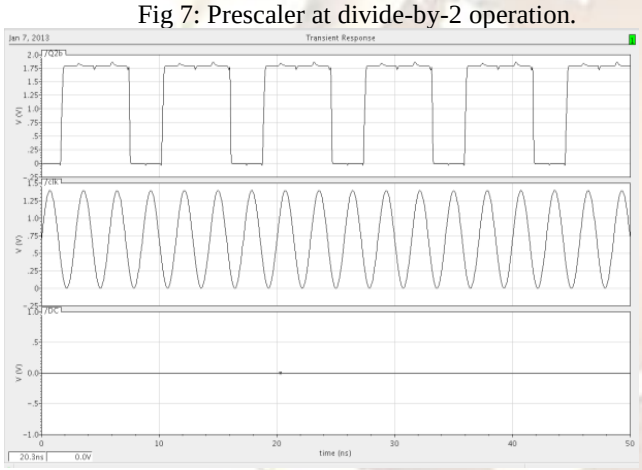

Fig 8: Prescaler at divide-by-3 operation.

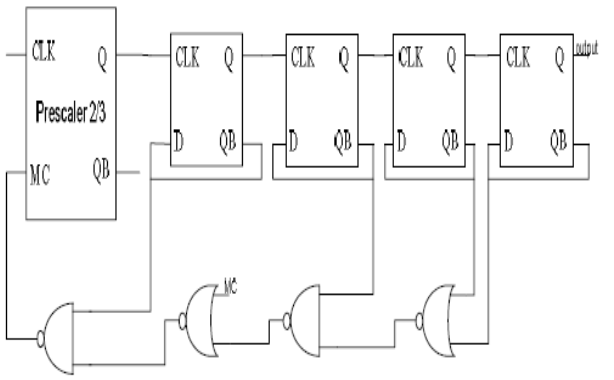

Fig 9: Logic structure of divide-by-32/33 counters design.

V. DIV-BY-32/33 PRESCALERS

Fig 9 shows the topology of a general 32/33 prescaler. The circuit contains one 2/3 prescaler unit, combination of NAND and NOR gates and four stages of toggled divide-by-2 units using DFFs. When the control signal MC is logically high, the 32/33 prescaler function as divide-by-32 unit and the control logic signal MC to the 2/3 prescaler goes logically high allowing it to operate in divide-by-2 mode for the whole 32 clock cycles. When control logic signal MOD is logically low, the 32/33 prescaler unit function as divide-by-33 unit during which 2/3 prescaler operates in divide-by-3 mode for 3 input clock cycles and in divide-by-2 mode for 30 input clock cycles [13].

VI. EXPERIMENTAL RESULTS

A comparison and complete analysis of the performance of various prescalers is carried out using Cadence virtuoso for 180nm CMOS process. TABLE 1 shows the simulation results of the operating frequency and power consumption of dual-modulus prescaler using different flip-flops for the operations of divide-by-2 and divide-by-3. The simulations are done at a supply voltage of 1.8V. Flip-flops, which are selected for prescaler designs come under different classifications such as master-slave, differential, TSPC and ETSPC technique. Fig 10 shows the logic block diagram of proposed 2/3 prescaler where FF1 and FF2 are replaced by WPMS, MSAFF and STFF flip-flops and results are compared with Design-II and proposed ETSPC design grouped in to the TABLE 1.

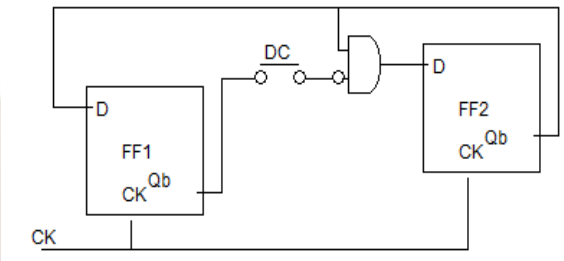

Fig 10: Logic block diagram of proposed 2/3 Prescaler

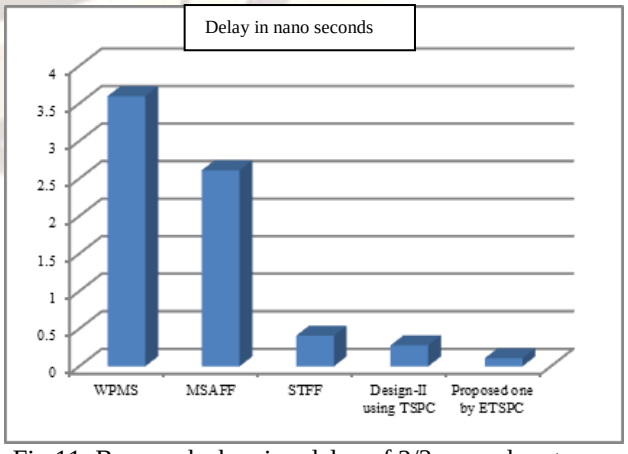

Fig 11: Bar graph showing delay of 2/3 prescaler at divideby-2 operation using different Flip-Flops.

Fig 11 and Fig 12 shows delay of dual modulus prescaler for divide-by-2 and divide-by-3 operation respectively. The operation speed of proposed design is 33.3% and 63.5% faster than WPMS, which took maximum delay, in divide-by-2 and divide-by-3 respectively. From both figures it is understood that ETSPC technique obtain less delay compared with others. This is due to the advantage of reduced transistor stacked height and load capacitance of ETSPC technique

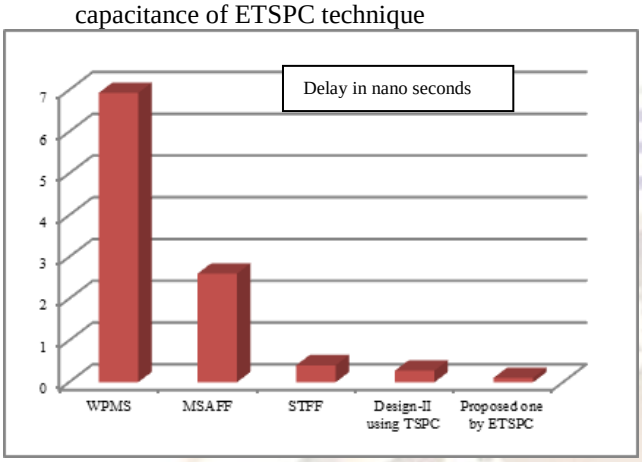

Fig 12: Bar graph showing delay of 2/3 prescaler at divide-by-3 operation using different Flip-Flops.

Design-II method uses TSPC flip-flops which have only one phase for clock signal. It avoids the overlap between clock signals and has less delay compared with MSAFF, STFF and WPMS. Since differential flip-flop give differential outputs, it avoid the extra delay of inverter circuit which is required by a master-slave flip-flop. In differential flip-flop STFF achieves minimum delay. The cross coupled inverter connection in the first stage of MSAFF makes it delay higher than STFF, having only two stacked nMOS connections. Due to the master-slave property, data will capture in one half of the clock cycle and retrieve only in the next half. Therefore it increases the data transmition time from input to output and the propagation delay of WPMS will increase.

From the TABLE 1 it is clear that at same supply voltage proposed design using extended TSPC technique has the highest frequency. Since operating frequency and propagation delay are inversely proportional to each other [11], flip-flop which has minimum delay has higher operating frequency. Reduced capacitance load decreases dynamic power consumption of proposed technique [1]. However decreased stacked connection leads to higher short circuit current in the ETSPC technique. This result in large power consumption for ETSPC compared to other flip-flops. When compared to ETSPC, TSPC has some more stacked connections which reduce the probability for getting short circuit and consumes less power than ETSPC. Power of WPMS, STFF and MSAFF is mainly depends on switching power. Reduced number of transistors and switching nodes in WPMS leads less power consumption when compared to STFF and MSAFF.

TABLE 2 shows the performance results of various 32/33 prescalers at a supply voltage of 1.8V. From the table it is understood that prescalers using proposed ETSPC prescaler achieves higher operating frequency.

TABLE 1: FEATURE COMPARISON OF VARIOUS DIVIDE-BY-2/3 COUNTER DESIGNS UNDER 180NM TECHNOLOGY.

Flip-Flop	V_{DD} (V)	Operating frequency	Div-by-2 P(mW)	Div-by-3 P(mW)
WPMS	1.8	300 MHz	0.8	1.27
MSAFF	1.8	335 MHz	1.16	1.26
STFF	1.8	351 MHz	0.58	1.372
Design-II using TSPC	1.8	3.25 GHz	1.159	1.665
Proposed design using ETSPC	1.8	5 GHz	1.663	2.217

TABLE 2: COMPARISON OF VARIOUS 32/33 PRESCALER UNITS UNDER 180NM TECHNOLOGY.

Various 32/33 Prescalers	V_{DD} (V)	Operating Frequency	Div-by-32 P(mW)	Div-by-33 P(mW)
Design-II 2/3 prescaler + TSPC FFs	1.8	2.59 GHz	1.33	1.365
Proposed ETSPC 2/3 Prescaler + TSPC FFs	1.8	4.84 GHz	1.4	2.572
Proposed ETSPC 2/3 Prescaler + ETSPC FFs	1.8	4.95 GHz	4.7	6.2

The minimum stacked connection of ETSPC flip-flops causes reduced load capacitance resulting less delay compared to the Design-II TSPC prescaler. But it hardly affects the short circuit power.

Eventhough the proposed 2/3 prescaler with ETSPC flip-flops acquires higher operating frequency; the higher power consumption leads to practically unusable them in mobile

communications. Therefore it is better to choose proposed prescaler with TSPC flip-flops for a 32/33 prescaler. To further verifying the results and to come across a good comparison power-delay-product (PDP) of various 32/33 prescalers are found over different supply voltages in the range of 1.5 to 1.8 volts. For an efficient design, prescaler having minimum power-delay product is preferred. Even though increasing the supply voltage reduces the operating delay, it will increase the power consumption of device. Since prescalers are using in mobile communications power should be optimized. Therefore a circuit having minimum power delay product has to be selected. Fig 13 and Fig 14 shows the simulation results of power-delay-product, a combined performance of speed and power, versus supply voltage for div-by-32 and div-by-33 prescalers.

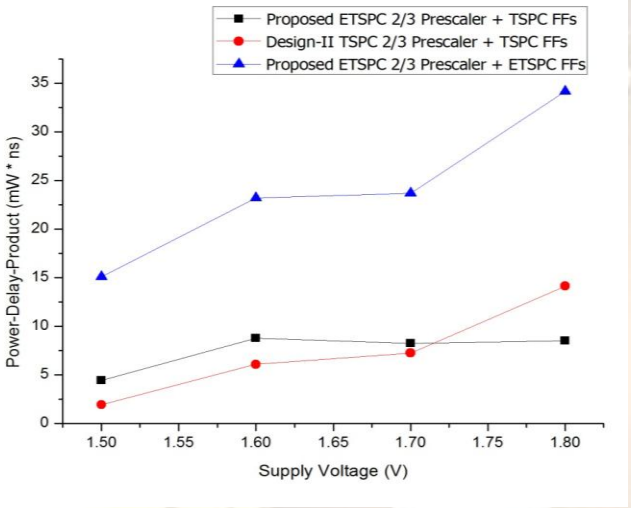

Fig 13: Power-delay-product versus supply voltage of prescalers at div-by-32 mode.

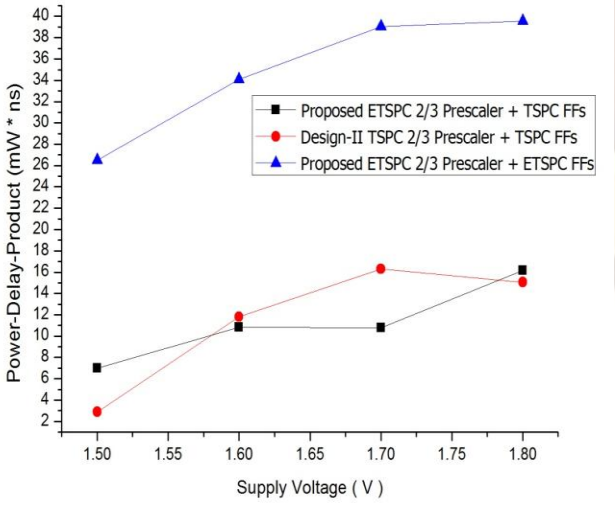

Fig 14: Power-delay-product versus supply voltage of prescalers at div-by-33 mode.

The 32/33 prescaler using proposed 2/3 ETSPC prescaler plus ETSPC FFs consumes maximum PDP in both div-by-32 as well as div-by-33 operation. Since ETSPC flip-flops have minimum stacked height, it creates higher short circuit power and increased PDP. The maximum power-delay-product of Design-II TSPC 32/33 prescaler and proposed ETSPC prescaler with TSPC flip-flops are almost similar during div-by-33 mode. But maximum PDP of Design-II TSPC 32/33 prescaler is 1.65x greater than proposed ETSPC prescaler with TSPC flip-flops in div-by-32 operation. Therefore ETSPC prescaler with TSPC flip-flops having higher operating frequency than Design-II TSPC 32/33 prescaler is the best topology for 32/33 prescaler.

VII. CONCLUSION

Dual modulus 2/3 and 32/33 prescaler using different flip-flop class is compared and analyzed based on power, delay, power-delay-product and operating frequency. Prescaler using ETSPC flip-flops have minimum delay and higher operating frequency. The structural advantage of ETSPC helps them to improve its operating frequency and reduce critical path delay. However the minimum height of stacked transistor connection cause higher short circuit current in ETSPC prescalers. The complex structure and difficult in embedding control logic between flip-flops increases the delay and reduction of operating frequency of master-slave and differential flip-flops. Reduced frequency range and lower short circuit current leads to low power in prescaler using WPMS, MSAFF and STFF flip-flops. In various 32/33 prescalers, proposed ETSPC 2/3 prescaler with TSPC flip-flops has better overall performance. Also it has the advantage of minimum PDP in div-by-32 mode. Therefore it can be used in the design of low power fully programmable frequency synthesizers.

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