DESIGN AND TESTING OF HIGH SPEED MULTIPLIERS BY USING LINER FEEDBACK SHIFT REGISTER

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Abstract

In today's Integrated Circuits (IC's) designs Built-in Self Test (BIST) is becoming important for the memory which is the most necessary part of the System on Chip. BIST is a design technique that allows a circuit to test itself. The technique can provide shorter test time compared to an externally applied test and allows the use of low-cost test equipment during all stages of production. Due to the randomness properties of Linear Feedback Shift Registers (LFSRs), this requires very little hardware overhead. In this paper, structure design and optimization of a Built-In Self-Test (BIST) design based on Linear Feedback Shift Registers (LFSRs) are described and different types of the Multipliers like Booth Multipliers and Array Multipliers Architectures are designed and tested by the using of LFSR and Proposed Low Transition LFSR (LT LFSR).

Index Terms— LFSR, BIST, Power Dissipation, Booth Multiplier, Array Multiplier, Test Patterns

I.   INTRODUCTION

Power dissipation is a challenging problem for today's system-on-chips (SoCs) design and test. In general, power dissipation of a system in test mode is more than in normal mode [1]. This is because a significant correlation exists between consecutive vectors applied during the circuit's normal mode of operation, whereas this may not be necessarily true for applied test vectors in the test mode. Low correlation between consecutive test vectors (e.g. among pseudorandom patterns) increases switching activity and eventually power dissipation in the circuit. The same happens when applying low correlated patterns to scan chains .Increasing switching activity in scan chain results in increasing power consumption in scan chain and its combinational block. This extra power (average or peak) can cause problems such as instantaneous power surge that causes circuit damage, formation of hot spots, difficulty in performance verification and reduction of the product yield and lifetime.

Now a day's many circuits include on chip structures that enable self testing known BIST. The power dissipation during the test mode 200% more than in normal mode. hence it is an important aspect to optimize the power during testing. The main sources of power dissipation in CMOS devices are summarized by the following expression

$$P = 0.5.C.VDD2.f.N+QSC.VDD.f.N+Ileak.VD \quad (1)$$

Where, p denotes the total power, vdd is the supply voltage and f is the frequency of operation. The first term in equation (1) corresponds to the power involved in charging and discharging circuit nodes. C represents the node capacitance and N is the switching activity i.e., the number of gate output transitions per clock cycle(also known as transition density)is the energy involved in charging or discharging a circuit with node capacitance C and is the average number of times per second that the node switches. The second term in (1) represents the power dissipation due to current flowing directly from the supply to ground. During this period that the pull-up and pull-down networks of the CMOS gate are both conducting when the output switches. This current is often called short circuit current. The factor represents the quantity of charge carried by the short circuit current per transition. The third term in (1) is related to the static power dissipation due to leakage current. The transistor source and drain diffusions in a MOS device from parasitic diodes with bulk regions. Reverse bias current in these diodes dissipate power.

The low power test pattern generator presented in [3] is based on cellular automata, reduces the test power in combinational circuits. Another low-power test pattern generator based on a modified LFSR is proposed in [4]. This scheme reduces the power in circuit under test (CUT) in general and clock tree in particular. A low-power BIST for data path architecture, built around multiplier-accumulator pairs, is proposed in [5]. The drawback is that these techniques are circuit-dependent, implying that non-detecting subsequences must be determined for each circuit test sequence. A low power BIST based on state correlation analysis proposed in [6].Modifying the LFSR, by adding weights to tune the pseudorandom vectors for various probabilities, decreases energy consumption and increases fault coverage [7] [8]. A low-power random pattern generation technique to reduce signal activities in the scan chain is proposed in [9]. In this technique, an LFSR generates equally probable

random patterns. The technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power. Authors in [10] proposed a method to select an LFSR's seed to reduce the lowest energy consumption using a simulated-annealing algorithm. Test vector inhibiting techniques [11] filter out some non-detecting subsequences of a pseudorandom test set generated by an LFSR. These architectures apply the minimum number of test vectors required to attain the desired fault coverage and therefore reduce power.

The rest of this paper is organized as follows. Section II describes our BIST Architecture Design with a new random pattern generator. Section III describes the Multiplier designs architectures, Section IV describes The Previous work of LFSR, Section V describes implementation of the proposed technique of low-Transition test pattern generation, The experimental results are discussed in Section VI. Finally, the concluding remarks are in Section VII.

II. BIST ARCHITECTURE

Built-in Self Test (BIST) is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, thereby reducing dependence on external automated test equipment (ATE).

A typical BIST architecture [3] consists of LFSR, reference circuit, Circuit under test, Multiple input signature register (MSIR), comparator, and BIST controller unit (BCU). The LFSR generates the test pattern. The outputs of the LFSR are used as the inputs to the reference circuit and CUT, which is c432 ISCAS-85 a benchmark circuit of interrupt controller [6].The output of the reference circuit and CUT is driven by MISR, which efficiently map different input streams to different signatures with every small probability of alias. Then output of the MISR is fed to the comparator, which is a test response analyzer (TRA). The comparator compares the output of reference circuit and CUT. If both the outputs are same, this indicates no fault in the CUT. If both the outputs are not same, this indicates fault in the CUT. The BCU controls the execution of all the blocks. This approach allows applying at-speed tests and eliminates the need for an external tester.
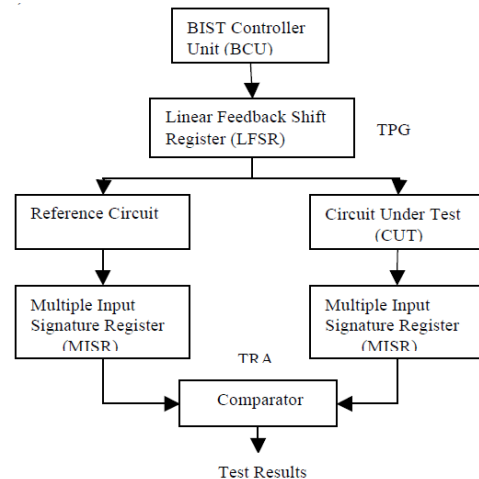

Fig 2.1: BIST Architecture

The components of BIST architecture is given below.
1. Test pattern generator (TPG): it generates test patterns for CUT. It is generally a LFSR or ATPG.
2. Circuit under test (CUT): it is the circuit to be tested. It can be either combinational, sequential or memory.
3. Multiple input signature register(MISR): it is designed for signature analysis, which is a technique for data compression.
4. Test response analysis (TRA): it compares the value of primary output with the expected output.
5. BIST control unit (BCU): it controls the test execution and manages all the components of a BIST circuit. And it is activated by a go/no go signal.

III. MULTIPLIER

Multipliers have large area, long latency and consume considerable power. Reduction of power consumption makes a device reliable. Therefore, low power multipliers with high clock frequencies play an important role in today's digital signal processing. Digital signal processing (DSP) is the technology at the heart of the next generation of personal mobile communication systems. Most DSP systems incorporate a multiplication unit to implement algorithms such as convolution and filtering. Multiplications are basic arithmetic operations used virtually in all applications involving digital signal processing. Multiplication can be considered as a series of repeated additions. Design of portable battery operated multimedia devices requires energy efficient multiplication circuits.

Types of Multiplier
Multipliers are classified by the format in which words are accessed namely:
1. Serial multiplier
2. Parallel multiplier
3. Serial-parallel multiplier
1) Serial Multiplier: It uses a successive addition algorithm .It has a simple structure because both the operands are entered in a serial form .Therefore the

physical circuit requires minimum amount of area and less hardware.

2) Parallel Multiplier: Most of the digital systems incorporate a parallel multiplication unit to carry-out high-speed operation due to the operands is entered in parallel which consumes less time.

3) Serial-Parallel Multiplier: The serial parallel multiplier serves as a good tradeoff between time consuming serial multiplier and area consuming parallel multiplier .These multipliers are used when there is a demand for both high speed and small area. In a device using serial-parallel multiplier, one operand is entered serially and the other is stored in parallel with a fixed number of bits.

A. Introduction to Array Multiplier: Each partial product is generated by taking into account the multiplicand and one bit of multiplier each time. The impending addition is carried out by high-speed carry-save algorithm and the final product is obtained employing any fast adder – the number of partial products depends upon the number of multiplier bits.
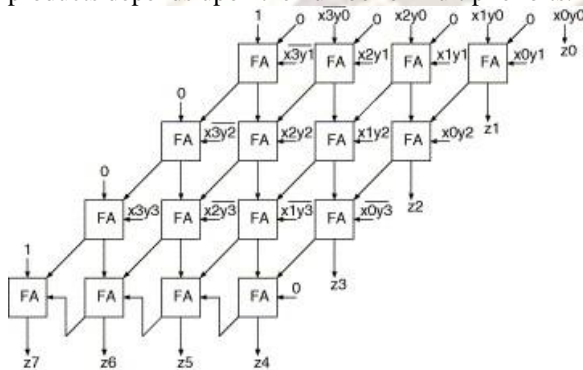

Fig 3.1: Array Multiplier

B. Booth Multiplier: The Fig. 3.2 shows the booth multiplier which performs both Signed and Unsigned operations. The main objective of designing the booth multiplier is to perform the partial products to reduce the delay and to increase the speed of the circuit. In this it also reduce the area of the chip used so the power consumption is also reduced in this circuit. The main operation of the booth decoder is to convert the given input to the equivalent booth value. So it contains more number of zeros.

The maximum delay time in the tree type binary multiplying circuit can be determined by the sum of a time in which partial products are formed from the output of the booth decoder having a multiplier provided and a multiplicand, and a time in which the thus formed partial products are added.
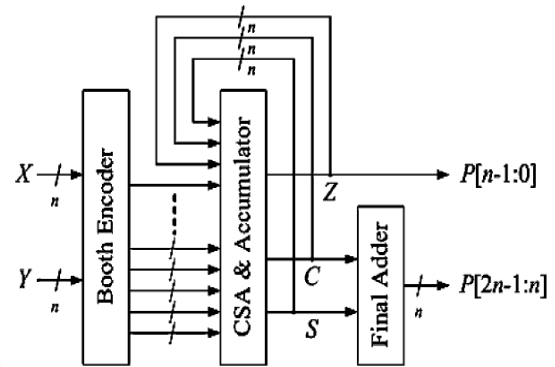

Fig 3.2: Booth Multiplier for Signed and Unsigned operation

By combining the booth decoders with the partial product generating circuits, the partial products of (m+1) bits should be generated from m multiplicand.

IV.   PRIOR WORK

A. Linear Feedback Shift Register (LFSR): Linear Feedback Shift Register is a circuit consisting of flip-flops connected in series with each other. The output of one flip-flop is connected to the input of the next flip flop and so on. The feedback polynomial which is also known as the characteristic polynomial is used to determine the feedback taps which in turn determines the length of the random pattern generation.

An example below in Figure 4.1 is used to illustrate a correlation between the LFSR, its characteristic polynomial and matrix theory. In the circuit the feedback taps are shown to be from the output of the 4th and 1st register.

These taps are indicative of the generator polynomial. Using the matrix theory the companion matrix required for relating the present to the next state is depicted. The actual sequence of the LFSR is represented as BT, BT2, BT3, ….where B is the seed vector. The determinant of the T matrix is called the characteristic polynomial and the generator polynomial is the inverse of the characteristic polynomial.

The increased power consumption by the device in the manufacturing test environment therefore can in most cases exceed the maximum power consumption specification of the IC resulting in un-repairable device failures begins with a pattern generated using a conventional LFSR causing significant loss of yield. Earlier Techniques for reducing the power dissipation during testing are

1. RSIC (random single input change) test generation, which is used to generate low power test pattern. In this method power consumption is reduced but at the additional cost is between 19% and 13%.

2. Another technique was proposed in [3] that is Low transition LFSR for BIST

applications. This reduces the average and peak power of circuit during testing.

3. In [4], a Fault model& ATPG algorithm is chosen first, and then test patterns are generated to achieve the desired fault coverage.
4. F.corno et al proposed a Low power test pattern generation for sequential circuit in [5]. In this paper redundancy is introduced during testing. This will reduces the power consumption without affecting the fault coverage.
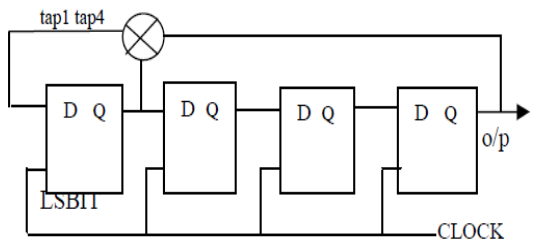
Standard LFSR:

Fig 4.1: Standard LFSR Architecture

A Linear Feedback Shift Register (LFSR) is a type of pseudorandom number generator. To illustrate an LFSR operation, consider a register that is 4 bits wide.

Start by loading it with an initial seed value. Shift it to the right, and XOR the bit at the output of the last flip-flop and first flip-flop. Then the output of XOR gate is fed to the input of first flip-flop. For this example, we'll use a seed of 0101.

0101 shifted is 1010 and a 1 fell off.
1010 shifted is 1101 and a 0 fell off.
1101 Shifted is 0110 and a 1 fell off.
1100 shifted is 0011 and a 0 fell off.

The number of values that an LFSR cycles through before repeating is its period. LFSRs that are maximal period cycle through 2^n-1 values before repeating, where n is the width of the register.

In this approach, the transitions are high which reduces the correlation between consecutive test patterns generated by the LFSR. Reduction in correlation increases the power dissipation during testing, thereby increases the power consumed by BIST.

V.   PROPOSED METHOD

A. Algorithm for Low Transition LFSR (LT LFSR) LFSR is a shift register which consists of series of flip flops and is used to generate test patterns for BIST externally. The initial value of LFSR is called seed value. It poses a significant effect on energy consumption [6]. The output that influences the input is called tap. LFSR is represented by a polynomial known as characteristic polynomial, which is used to determine appropriate feedback taps. A common clock signal is applied to the flip flops

which enable the propagation of bits from input to output of flip flops. The correlation between the bits can be achieved by adding more number of test vectors which reduces the switching activity so that the power consumption is reduced.
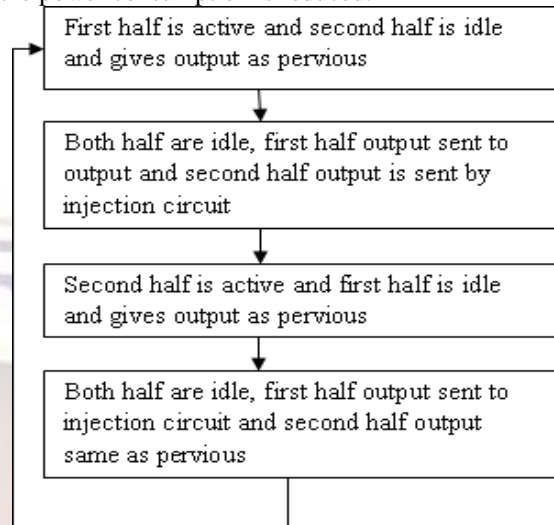

Fig 5.1: Proposed LT LFSR

The TPG is activated by two non-overlapping enable signals (en1 and en2). Each enable signal activates one half of the LFSR. In other words, when en1en2=10, first half of the LFSR is active and the second half is in idle mode. The second half is active when en1en2=01. MUX selects either the injection bit or the exact bit in the LFSR.

The proposed approach consists of two half circuits. The algorithm steps says the functions of both half circuits is

Step1: First half is active and second half is idle and gives out is previous, the generating test vector is Ti.

Step2: Both halves are idle First half sent to the output and second half's output is sent by the injection circuit, the generating test vector is Ti1.

Step3: Second half is active First half is in idle mode and gives out as previous, the generating test vector is Ti2.

Step4: Both halves are in idle mode, First half is given by injection circuit and Second half is same as previous, the generating test vector is Ti3.

After completing step 4 again goes to step1 for generating test vector Ti+1.

The first level of hierarchy from top to down includes logic circuit design for propagation either the present or next state of flip-flop to second level of hierarchy. Second level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output which provides more power reduction compared to having only one of the RI injection and Bipartite LFSR techniques in a LFSR due tohigh randomness of the inserted patterns.

VI.   RESULTS

The Questa Sim 6.5 e Menter Graphics EDA tool is used in which conventional and low Transition

LFSR is coded in verilog hardware description language. The outputs of Booth Multiplier and Array Multiplier Testing by using Low Transition LFSR is Shown in Fig 6.1 and 6.2.and Low Transition LFSR is Shown in Fig 6.3.
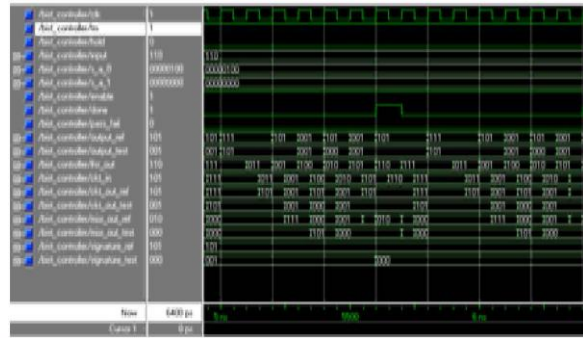

Fig 6.1: Simulation Result of Booth Multiplier Testing Using LT LFSR
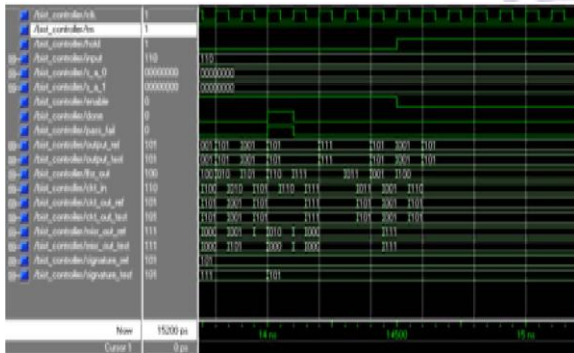

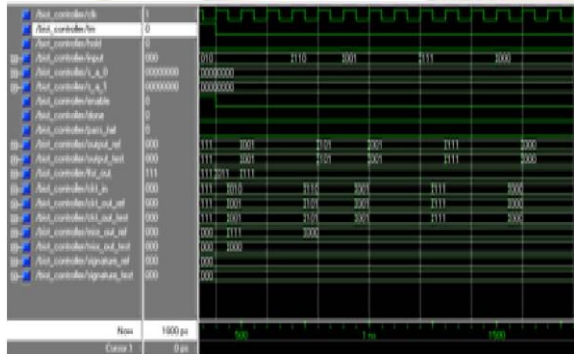Fig 6.2: Simulation Result of Array Multiplier Testing Using LT LFSR

Fig 6.3: Simulation Result of Low Transition LFSR

Table 6.1: Comparison of Different types of Multipliers by Using LT LFSR

Parameters	Delay(ns) With LT LFSR
8bit Booth Multiplier	40.002
8bit Array Multiplier	41.698
16bit Booth Multiplier	71.867
16bit Array Multiplier	78.465
32bit Booth Multiplier	125.523
32bit Array Multiplier	136.869

VII.   CONCLUSION

The proposition is an attempt to invoke research on the test pattern generator itself. The techniques available so far have focused upon reducing the switching activity from the test patterns generated from the generator. Embedding the switching activity minimizing techniques with a power efficient test Pattern generators will be a good step ahead.

Therefore a modification is proposed in the conventional LFSR by embedding it with control logic module and bit interchanging module. This culminates into a novel architecture of the test pattern generator (TPG). By Using the modified TPG architecture is, We Test the High Speed Multipliers and Calculate the Performance of The Multipliers. The benefit of the proposed TPG is that it can be used with any other low power technique to have further reduction in power.

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