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Design and Implementation of a Microcontroller Based PWM Sinewave Inverter for PV Applications

***Aminu Tukur * **I. G. Saidu, *M. Momoh, ***Zainab U **A. S Mindaudu, ***M.I Ilyasuand ***M.A. Yusuf**

*Physics Department, Usmanu Danfodiyo University, Sokoto
**Sokoto Energy Research Centre,
***Physics/Electrical Department, Sokoto State Polytechnic,

ABSTRACT

A major factor worthy of consideration in the overall performance of any PV system is how the installed system can exploit the sun's energy most effectively by ensuring that arrays have full access to most of the solar resource. This research was therefore concerned with the modification of inverters to enhance the period for which energy is extracted from a PV system and to extend the range of voltages from PV that could operate inverters. To achieve this, the output of a 12V PV system was boosted to 24V then regulated back to 12V before inversion. A Microcontroller-based Pulse Width Modulated (PWM) Power Inverter for PV systems, suitable for use at homes as alternative power source for AC loads was designed, simulated and constructed. The most important feature of this system is that it is suitable for PV systems and highly effective in driving variable loads. Other features include provision for sensing the load voltage to adjust the pulse width to meet the load demand at every instance. It also provides the user with shutdown option in case of the system being idle (on no-load), the system can be put to standby mode instead of switching off the entire device. When on standby mode it consumes very small current of few milliamperes. The system was built around ATMEL™ version of 8051 microcontroller AT89C2051.When tested the system was found to provide a constant sinusoidal voltage of 240V even with a varying voltages at the input.

INTRODUCTION

Inverters have input voltage window beyond which they could fail (Albert, 1999). For stand-alone PV systems the input power is derived from PV modules that are exposed to solar radiation. Most inverters convert the incoming DC into AC, and then use a transformer to step up the output AC signal to mains voltage level. In doing this, one major consideration is that of how can an inverter perform this operation efficiently in order to avoid wastage of the voltage from battery, solar panel or other DC sources.

The amount of current produced by a solar panel is a function of the solar radiation falling on it. Solar radiation however fluctuates from zero in the night then gradually increases in the morning while peaking at midday and finally gradually decreases to zero as darkness sets in (Rodríguez, 2000). PV module voltages are also affected by temperature. As the temperature decreases PV modules voltage actually increases (voltage and temperature of a PV have an inverse relationship) (Rodríguez, 2000). If the voltage from the array ever drops below the minimum power point tracking voltage – usually due to high heat conditions that occur on sunset days or as a result of PV position, the inverter won't be able to continue operating and will shut down. This means that the inverter could shut down due to low voltage on bright sunny day (Rodríguez, 2000). PV modules can perform for many years, but are not perfect as in the course of years the modules output power (a function of voltage and current) will degrade (Nabae*et.Al.*, 1981). This means with time the PV will not be able to keep up with the inverters request. On another hand, most PV modules designed to provide an output of 12V really actually do so (Rodríguez.,2000). The implication of this is that an inverter with a transformer designed to step up the 12V to 240V (transformation ratio of 20) would produce erratic output due to fluctuations in the input voltage.

The aim of this research is to design an inverter that operates even at low solar radiations and PV environmental conditions. This, it is hoped would extend the hour of power extraction per day and the window of voltage input useful to the inverter.

Circuit Design of the Various Modules

In the design presentation that follows, a modular format is adopted as each design procedure of the blocks is presented one after the other. The presentation starts with the choice of Voltage regulator to yield the required input voltage. The second stage was the DC-DC converter to give the calculated voltage regulation. The third stage was the design of the inverter stage followed by the output transformer and the filter stage. The design of the PWM and Schmitt trigger control were then presented.

Voltage Regulator Stage

To achieve a constant voltage output despite variations in the input voltage or load a voltage

regulator was employed. The regulator ensures that the output voltage is independent of increase in the supply voltage or in the current drawn from the supply resulting in a constant voltage. The voltage regulation was based on LM7812. This regulator is expected to provide a steady 12V for inversion.

Design of the Inverter

The inverter was designed based on the block diagram of Fig. 1

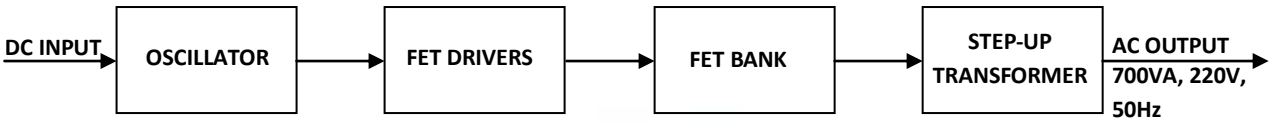

Fig. 1 Block Diagram of the Inverter

Design of FET Drivers

The FET bank are array of FETs connected together to achieve high power for the inverter. In operation the FETs in the array needs to be driven by a circuit that acts as a switch. This is done using transistor circuit connected to operate at the cut-off and saturation points. For this purpose, a TIP41A NPN transistor was used for switching the FET bank due to its being readily available locally and cheap.

The figure (Fig. 2) depicts the circuit configuration of the FETs driver unit

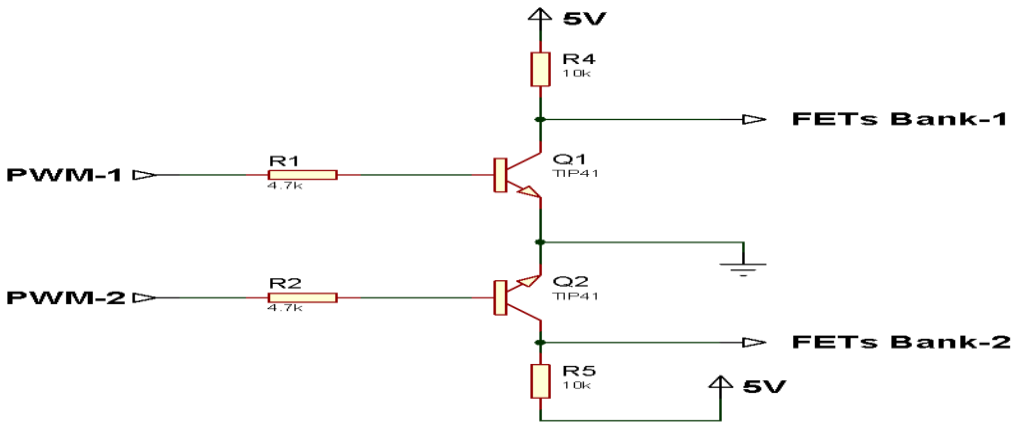

Fig. 2FET Driver Unit

Two NPN transistors TIP41A were wired as switches. The two transistors conduct alternately; in other words, when one is ON, the other is OFF. Resistors R_1 and R_2 were used to provide safe operating current to the two transistors while R_4 and R_5 are load resistors. From manufacturer's datasheet, specifications for TIP41 transistor include:

Absolute maximum ratings:

Emitter-base voltage $V_{EBO} = 5V$;

Base current $I_B = 600mA$

Therefore, the value of the base resistance for each of the two resistors is obtained as follows:

$$R_B = \frac{V_{EBO}}{I_B} = \frac{5}{600\times10^{-6}} = 3k\Omega$$

To ensure that the operating current is always safe for the transistor, 4.7kΩ was used in the circuit.

FET Bank Design

The FETs bank is an array of MOSFETs, connected such that it drives the load comfortably. The FET bank is one of the factors that determine the power of the inverter. They are either connected in half bridge or full bridge format. A half bridge requires a minimum of two pairs of FETs that conducts alternately, while full bridge requires four numbers of FETS that conducts with two diodes at each state. The FET bank design was based on the half bridge configuration with three FETs on each half bridge to take care of the power requirement. This type has the advantage of requiring lesser number of FETs. The circuit of the half switching mode is as shown in Fig 3. The main advantage the FET has over BJT is that when switched ON it has almost zero resistance and when switched OFF it has infinite resistance (Theraja and Theraja, 2005). This feature of the FET leads to higher efficiency.

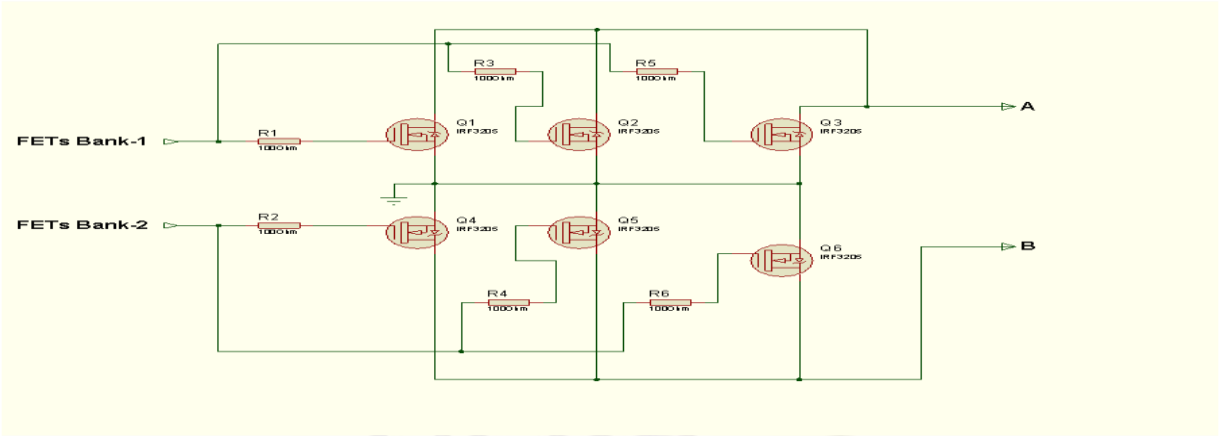

Fig. 3 FETs Bank Circuit

As shown in the figure above, each three MOSFETs are connected in parallel. The MOSFET used in this design is the IRF3205 and as each of the MOSFETs can drive 180-Watts load or drain current of up to 80 Amperes, . Hence, the maximum power that the circuit can deliver is 180×4 = 720W. Also, the maximum current drain by each MOSFET $I_{D(max)}$ = 40A, therefore a protection fuse was added against overload. Since the gates have very high input impedance, a 100Ω resistor was connected in series with each gate to ensure safe operating voltage at the input. **NAND Schmitt Trigger Design**

The NAND Schmitt trigger is a circuit that is used for pulse shaping. Essentially, it is similar to a bistable multivibrator with very short transition time. The CD4093 was used in this design.

Fig. 4is the circuit configuration for this application.

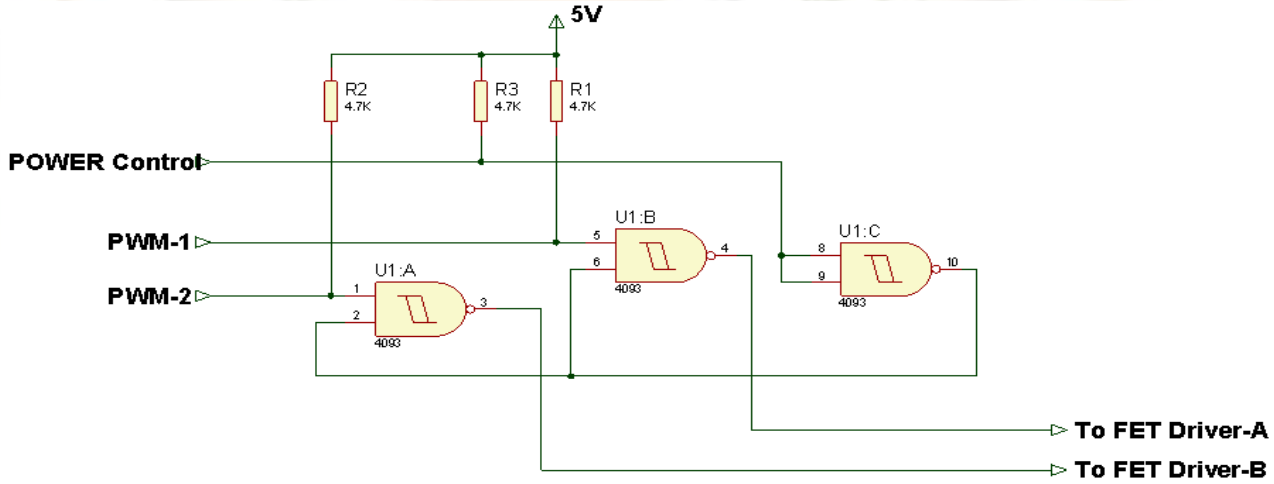

Fig. 4 CD4093 Circuit

As seen from the circuit diagram, three of the four NAND gates were used as explained below.

This section represents the microcontroller based sinusoidal PWM generator for the inverter for the photovoltaic application. The advantage of this inverter is the use of a low cost microcontroller that has built in PWM modules. Microcontroller 8052 is able to store the required commands to generate the necessary PWM waveforms.Sinusoidal pulse width modulation (SPWM) is widely used in power electronics to digitize the power so that a sequence of voltage pulses can be generated by the on and off of the power switches. The pulse width modulation inverter has been the main choice in power electronic for decades, because of its circuit simplicity and rugged control scheme. SPWM switching technique is commonly used in industrial applications or solar electric vehicle applications. SPWM techniques are characterized by constant amplitude pulses with different duty cycle for each period. The width of this pulses are modulated to obtain inverter output voltage control and to reduce its harmonic content.

The algorithm for the software development is illustrated bellow. It briefly describes the software operations for the microcontroller in generating the PWM signal.

- Initialize the user defined memory cells;
- Iinitialize the ports to be used as output.

- Initialize the modules used for the generation of PWM.
- Initialize all the desired interrupts
- Store the sampling value of sine wave in the look up table.
- Store the sampling value in the PDC register.
- The PTMR register generates the Triangular wave.
- The signal is made PWM signal with dead time.
- The microcontroller checks whether the generation is completed or not,
- If it is completed , it takes another sampling from the sine wave table.
- Otherwise it waits for the completion.

PWM Design Procedure

The microcontroller is configured to generate the PWM signals that is used to regulate the pulses of the half bridge circuit.

PWM or Pulse width Modulation is used to keep the output voltage of the inverter at the rated voltage irrespective of the output load. In a conventional inverter the output voltage changes according to the changes in the load. To nullify effect caused by the changing loads, the PWM inverter correct the output voltage according to the value of the load connected at the output.

The signal will include the fundamental component and harmonics.

We determined the location of the harmonics by using the relationship

$f = kM_R f_m$ (Lasseter, 1994)

Where, k is an integer (1, 2, 3 …).

The calculated values of the harmonics are tabulated in Table 1.

Table 1The Location of the fundamental and higher orderharmonics

k^{th}	f(Hz)
Fundamental 0	50
1	20000
2	40000
3	60000
4	80000

Filter Design:

The output signal normally contains the fundamental sinusoidal frequency and signals of higher harmonics. The higher frequency signal can be filtered out using appropriate filter circuit. According to the table above the first harmonic that will exist is at frequency 20 kHz. This value is more than two decade higher than the fundamental frequency which is at 50 Hz. A simple LC filter will adequately filter out the harmonics.

The filter was designed based on the cut-off frequency, f_c determined based on the location of the first harmonic. As calculated in section d) above, the first harmonic is at 20 kHz. Therefore, the cut-off frequency 400Hz is chosen in order to design this filter. By choosing the capacitor, C equal to 1mF the inductor, L can be calculated from

$$f_c = \frac{1}{\sqrt{\omega LC}}$$

$$\therefore L = \frac{1}{\omega C f_c^{\,2}} = \frac{1}{2\pi 50Hz \times 1mF \times 400Hz^2}$$

$$= 19.8944\ \mu H$$

We chose a 25µH inductor.

The eventual circuit diagram was constructed and subjected to voltage and power tests to see if it meets design specifications

TESTS

The project was finally subjected to tests by feeding a variable voltage at the input of the inverter while monitoring the output of the voltage regulator and that of the inverter as shown in plate 1

Plate 1Set-up Of The Final Tests

The setup of plate1 as represented block- diagrammatically in Fig 5 was used. The variable D.C Supply was varied from 7V to 14V in steps of 1V. The corresponding values at A, B and C were measured Using V1, V2 and V3 respectively. The shape obtained after filteration was displayed using oscilloscope. .

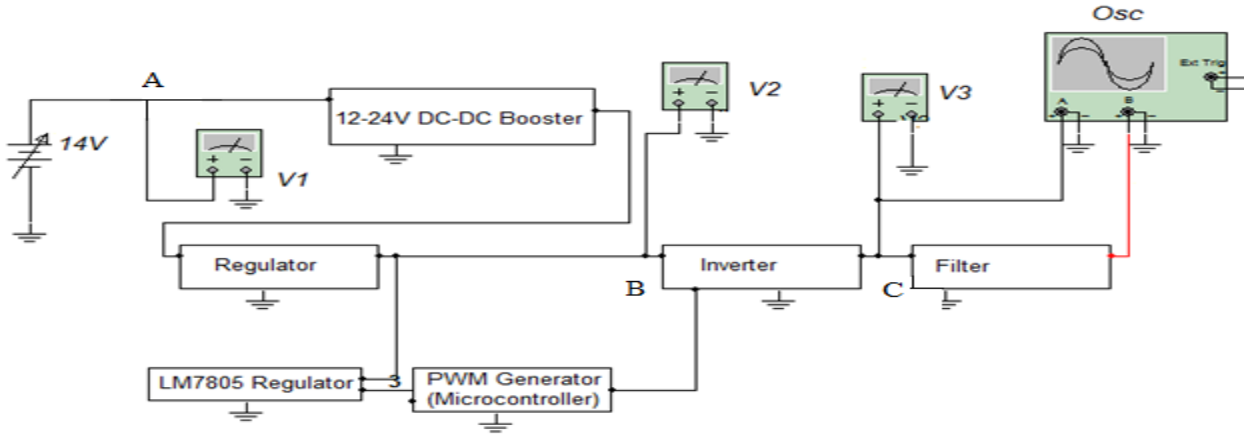

Fig. 5 Block diagram representation

RESULTS AND DISCUSSIONS

Table 2 shows the result of the voltage tests experiment of the inverter.The result is that of the input voltage to the inverter, output of the booster, outputs of the regulator and the final stage.

Table 2Result of the voltage tests experiment of the inverter.

V1 (volts)	V2 (volts)	V3 (volts)	V4 (volts)
14	27.89	11.95	238.86
13	25.86	11.87	238.84
12	23.78	11. 84	238.81
11	21.77	11.88	238.71
10	19.78	11.84	238.73
9	17.77	11.86	238.65
8	15.76	11.86	238.55
7	13.75	11.86	238.44

DISCUSSION

Table .2 indicates a fairly constant output of approximately 12 volts from the voltage regulator. Even though the input voltage was varied from 14V to 27.89V (V_2) the output voltage remained virtually regulated at approximately 239V (V_4). The implication of this is that the inverter will be able to operate even if the PV module is delivering voltage that varies widely from the expected value either as a result of variation in the PV temperature (Rodrigueze, 2000) or ageing of the PV (Nabea, *et. al.*, 1981).

The output signal is sinusoidal with a frequency of 50Hz and peak value of 349.5V and rms value of 246.902V. The output of the inverter is therefore suitable for a wide range of applications and for countries like Nigeria with a mains requirement of 240V and 50Hz.

In a nutshell, this research has carried out the design and construction of an inverter that is

suitable for use as alternative power source for electronic appliances. It was designed to address the problems faced by inverters that fail to work due to low voltage from PV arrays.

CONCLUSION

In this paper, a PWM sinewave inverter has been designed and constructed. The design is suited for the conversion of d.c power from PV panels to a suitable a.c form.

The designed boost converter was able to boost an output of 12V to a level of 24V and the relatively large transient present in its output was taken care of by using a resistive damper.

The output from the output filter was sinusoidal and largely constant at 240V even with significant variation in the input voltage which makes it suitable for PV applications.

It is also worthy of note that this design is not suitable for high power applications. If high power is demanded, then the voltage regulator should be replaced with a more powerful ones such as those based on power transistors.

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