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# Data Acquisition system based on FPGA

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**ABSTRCT:-The objective of this paper is to design and implement an data acquisition system(DAQ) by using serial RS-232 and SPI communication protocols on FPGA platform. The developed DAQ system should be able to acquire both analog signals as well as digital signals. The system converts the analog signals into digital data and send the data into the computer using RS-232 serial communication for further processing. The development of the system has been divided into two phases. The first phase is to the design of SPI interface, while the second phase is to the design of RS-232 interface. The SPI interface deals with the ADC and amplifier communication with FPGA and the RS-232 interface deals with the communication between PC and FPGA. The SPI and RS-232 communication protocol have been developed using VHDL programming language and implemented in Sparten3A/3AN board. The IDE tool Xilinx ISE 12.3i is used in out paper**

***Keywords*** **-**Field programmable gate arrays, Tagged image file format.

## I. INTRODUCTION

Data acquisition is the process of collecting and measuring real time signals. The acquired data is used by the computer for further processing. The paper was to design and implement and data acquisition system by using serial RS-232 and SPI protocol in an FPGA. This implementation would form a foundation for further research and practice into this form of embedded system design. Such a system has far reaching uses in the fields such as tomography, software radio, radar, image processing etc[2]. The process of designing and building a data acquisition
system to perform basic acquisition of analog signals such as voltage, power, temperature etc. In this paper, RS-232 asynchronous serial communication and SPI synchronours serial communication to acheve data rate of 1.5Msps with high accuracy for the system. The block diagram of Data acquisition system consists of an personal computer function generator, ADC and an programmable amplifier as shown in Fig.1. The serial ADC used will be and 14 bit LTC1407A-1 and the amplifier is LTC6912-1. In real Time application instead of function generator we have to use signal conditioner which converts the analog signals into electrical signals which can be applied to the ADC. The system acquires analog as well as digital signals [3]. In this Paper we have used Tektronix function generator. The personal computer chosen is any computer with Windows XP operating system. The LTC1407A-1 is a 14-bit, 3Msps ADC with two 1.5Msps simultaneously sampled differential inputs. The device draws only 4.7mA from a single 3V supply. The LTC6912 is a dual channel, low noise, digitally programmable gain amplifiers that are easy to use and occupy very little PC board space.

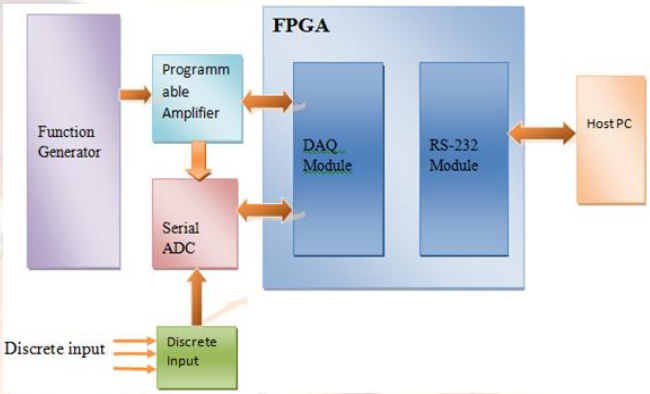


Fig 1. FPGA based data acquistion system

The gains for both channels are independently, programmable using a 3-wire SPI interface to select voltage gains of 0,1,2,5,10,20,50 and 100v and all gains for the amplifier is inverting. The system consists of two major parts. Data acquisition module and standard RS-232 module, both these modules are implemented in Spartan 3A/3AN FPGA starter kit using Xilinx ISE 12.3i tool described in VHDL. The system uses two communication protocols, Serial RS-232 communication protocol and SPI communication protocol. Serial protocol is used to communicate asynchronously between FPGA to host PC and SPI protocol is act as a master and slave which communicates synchronously between external on board ADC and FPGA. The main function of the developed system is to acquire analog as well as digital signals and converts the signals into equivalent digital form and send it to the PC for further usage. Xilinx has many commercial products in which FPGA found their way into consumer automotive and industrial applications [5]. Now applications of FPGAs include digital signal processing, software-defined radio, aerospace and defense systems, ASIC prototyping, medical imaging, computer vision, speech recognition, cryptography, bioinformatics, computer hardware emulation, radio astronomy and a

growing range of other areas.

## II. RS-232 PROTOCOL HARDWARE IMPLEMENTATION

### A. *Serial communication*

Serial communication enables different equipments to communicate with outside world, where information to be transformed is represented in serial data bits and will be sent in a serial way over a single line. Personal computer has a serial data bits and will be sent in a serial way over a single line. Personal computer has a serial port known as communication port or COM port in PC [6]. Serial ports are controlled by a special chip called UART (Universal asynchronous receiver transmitter). Different application use different pins on the serial port and this basically depend of the functions required. Devices that use serial cables for their communications are split into two categories DCE (Data communication equipment) and DTE (Data terminal equipment) device.

### B. *Interfacing DAQ with RS-232*

In order to establish the communication link between the PC and the data acquisition module it is necessary to use either serial or parallel communication channel. Information being transferred between data processing equipment and peripherals is in the form of digital data which is transmitted either in a serial or parallel mode; Parallel communications are used mainly for connections between test instruments or computers and printers, while serial is often used between computers and other peripherals. Serial transmission involves the sending of data one bit at a time, over a single communication line [7]. In contrast, parallel communications require at least as many lines as there are bits in a word being transmitted. In asynchronous serial communication the date is transmitted by a bit in order, in which two transition lines is needed to realize bidirectional communication. Serial communication is utilized in the DAQ system in order to simplify the hardware and save the cost, format and save your graphic images using a suitable graphics processing program that will allow you to create the images as PostScript (PS), Encapsulated PostScript (EPS), or Tagged Image File Format (TIFF), sizes them, and adjusts the resolution settings. If you created your source files in one of the following you will be able to submit the graphics without converting to a PS, EPS, or TIFF file: Microsoft Word, Microsoft PowerPoint, Microsoft Excel, or Portable Document Format (PDF).

### C. *RS-232 Serial port*

RS-232 is a telecommunication standard for binary serial communications between devices. It provides the roadmap for The way devices communicate each other using serial ports. The devices are commonly referred to as a DTE (Data terminal equipment) and DCE (Data communication equipment). Updated designations for the RS-232 protocols have included EIA-232 and the more current EIA/TIA-232. (Telecommunication industry association).

## III. SPI PROTOCOL HARDWARE IMPLEMENTATION

### A. *SPI Bus principle*

The serial peripheral interface bus is a synchronous serial data link standard named by Motorola that operates in full duples mode, sometimes SPI is called a “four wire” serial bus. There is one master and one or more slave devices in the communication. The general Master Slave configuration is as shown in Fig 2.

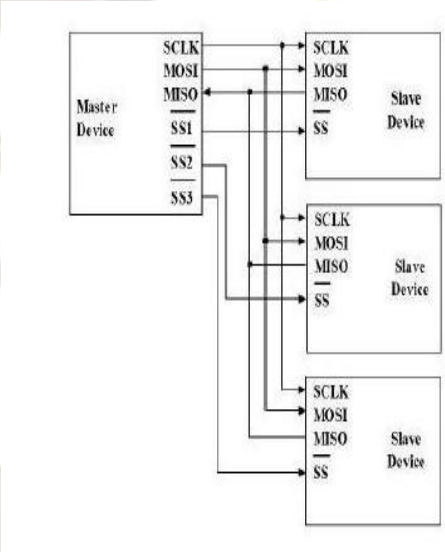


Fig 2. General SPI bus system with 1 Master device and with 3 slaves.

### B. *Analog circuit design*

The ADC- LTC1407A-1 and the pre-amplifier LTC6912-1 is used in the paper paper concurrently when sampling analog data using a serial peripheral interface as show in Fig 3. The input pin VINB is used solely to capture the analog wave form while the pin VINA is left connected.

The preamplifier scales the incoming analog signal. The output of the amplifier connects to the Linear Technology LTC1407A-1 ADC. Both the pre-amplifier and ADC are serially programmed or controlled by the FPGA. The analog capture circuit converts the analog voltage on VINA or VINB and converts it to a 14-bit digital representation as expressed in equation below

$$D[13:0] = GAIN \times \frac{(V_{IN} - 1.65V)}{1.25V} \times 8192$$

The reference voltage for the ADC and amplifier is 1.65V,
generated via an voltage divider and consequently 1.65v is subtracted from the input voltage on VINA or VINB. The ADC presents an 14-bit two's complement digital output.

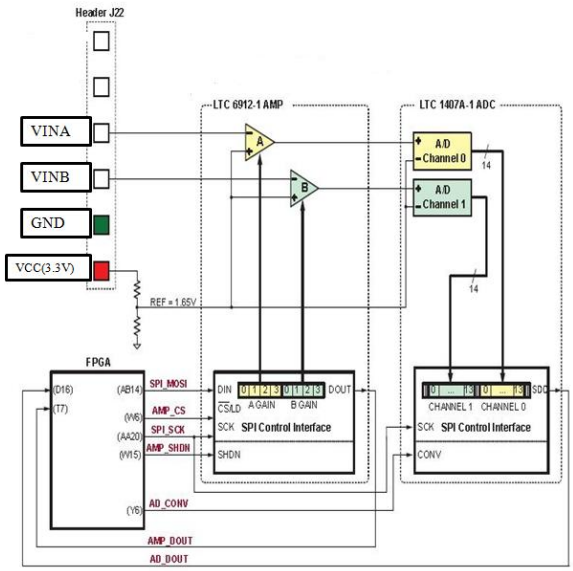


Fig 3. Detail view of analog capture circuit

## IV. DESIGN

### A. *VHDL implementation of amplifier communication*

The ASMD(Algorithmic state machine and data path) similar to normal flow chart. The main difference is that the register transfer operation in an ASMD chart is controlled by an embedded clock signal and the destination register is updated when the FSMD(Finite State Machine with Data path) exists the current ASMD block, but not within the block[8]. The ASMD for and amplifier communication as shown in Fig 4. Gain setting was chosen as "0001001" in order to obtain the maximum input voltage range. IDLE state initializes the amplifier, Set_Amp informs the amplifier to be ready to receive the gain setting Set_SCKCS_LOW generate SCK low signal. While the SCK to high and SCK_HIGH rotate the gain setting by 1 bit to the left. CHECK_AMP verify the value of bit_count and carry on with ADC process when the value is zero. If the value is not zero, repeat the loop and transmit the gain setting. Counter register ensure that SCk high and low are valid at least for 2 cycles of 50 MHz clock to be able to read by amplifier.

### B. *Simulation result for Amplifier communication*

Simulation result shows that each SCK high and low states take 401ns. Most high state takes 160ns and the whole process takes about 959ns as shown in Fig 5. The comparison of simulation result with the timing specified in data sheet as shown in Table 1. The whole process is constrained by 50MHz clock. Since this is a onetime process to set the gain setting of amplifier, small difference doesn't make any significance.

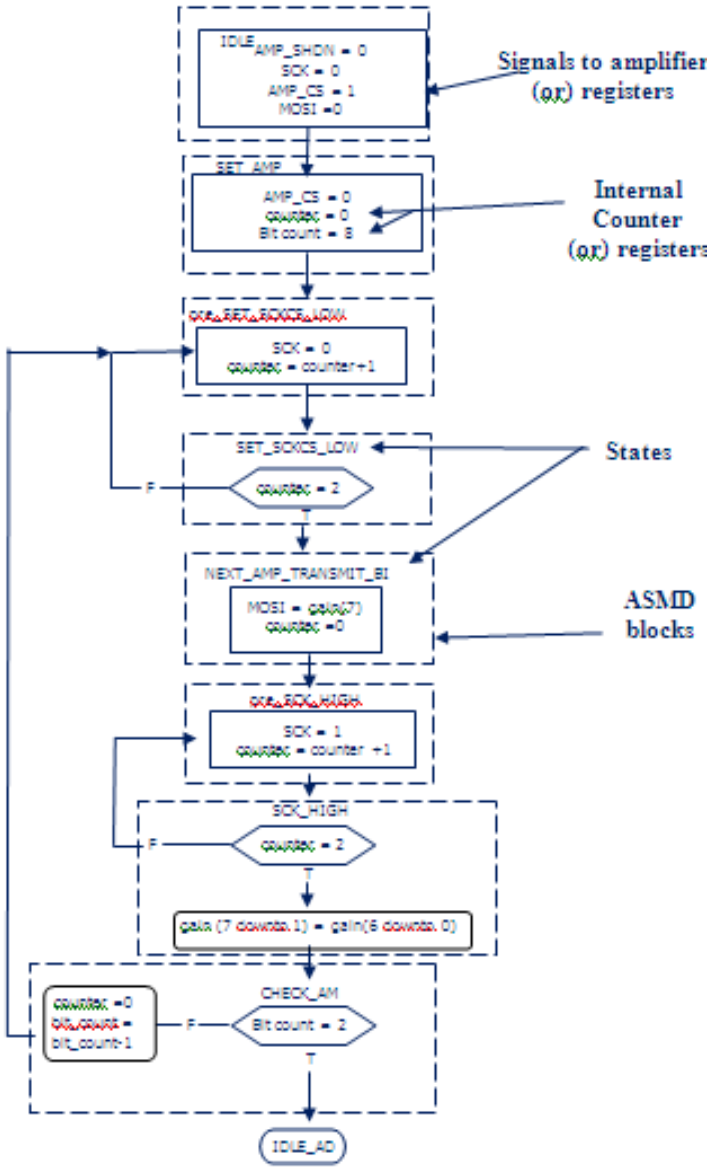


Fig 4. ASMD chart of amplifier communication

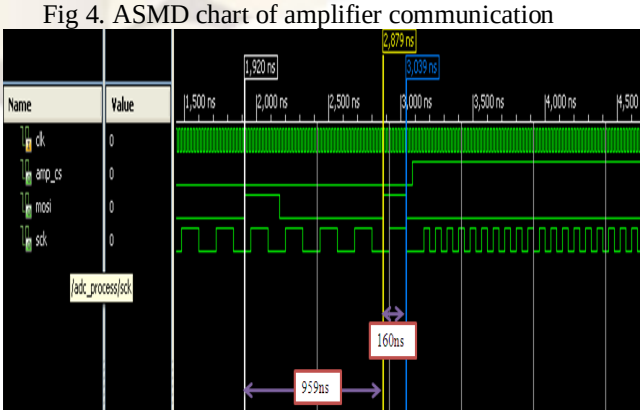


Fig 5. Simulation result of amplifier communication

Table 1. Timing comparison with data sheet.

| | Data sheet specification (ns) | Simulation result (ns) | Difference |
|---|---|---|---|
| SCK high, low | 50 | 40 | 10 |
| MOSI high | 115 | 160 | 45 |
| whole process | 860 | 959 | 99 |

### *C. VHDL implementation of ADC communication*

The state IDLE_AD initializes the SPI interface of ADC. START_AD initiates the ADC conversion process. HI_AD and LO_AD generate SCK high and low signals. 1 bit of ADC data from SPI_MISO pin are stored in ADC1 register while SCK signal is in low state. After counter reach to 34, the looping process starts again from START_AD. The detailed ASMD of ADC communication as shown in Fig 6.

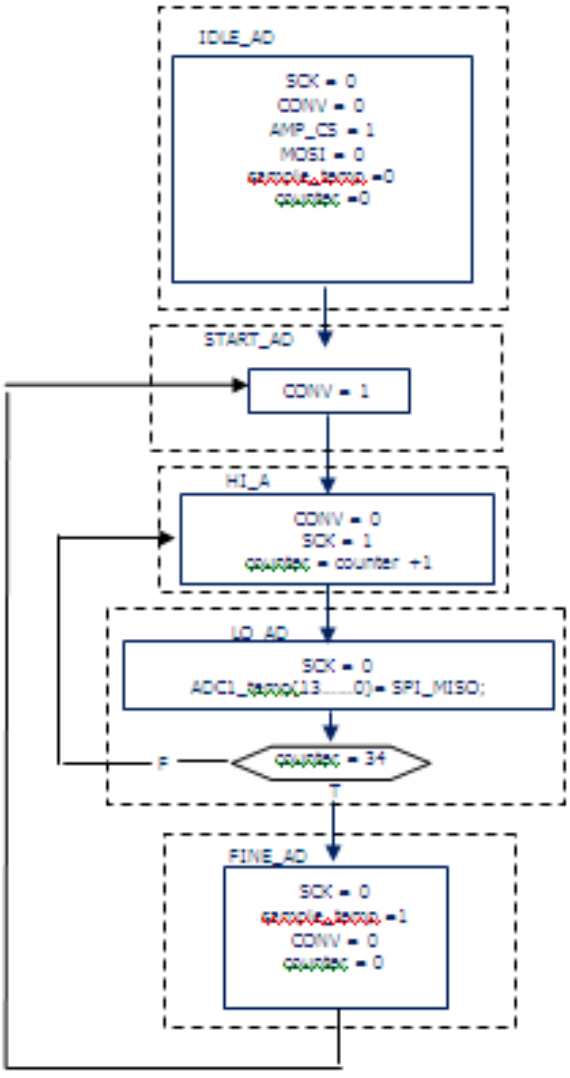


Fig 6. ASMD chart of ADC communication

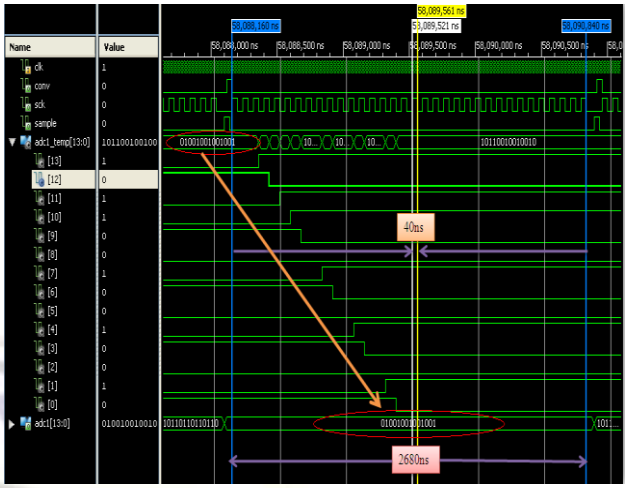


Fig 7. Simulation results for ADC communication

### *D. Simulation result for ADC communication*

The Spi_miso bits are manually generated in the test bench to test the functionality of the code. SCK takes 40ns to complete 1 cycle and adc1_temp2 stores the spi_miso bits when SCk is in low state. After the conversion process complete, data stored in adc1_temp are transferred to adc1. Sample flag is to indicate that the whole cycle of ADC conversion process is done and new ADC data is ready. The whole process of ADC conversion takes 2680ns to complete one cycle as shown in Fig 7. It should be noted that 1.5 MHz ADC sampling frequency can be achieved by reducing the SCK period to 20ns which is 50 MHz.

## V. RESULT ANALYSIS

The entire DAQ system hardware in a Spartan 3A/3AN FPGA board as shown in Fig 8. It also shows that the programmable amplifier and ADC are on board, the function generator and PC is connected externally. The DAQ module (SPI) and RS-232 protocols are implemented on FPGA.

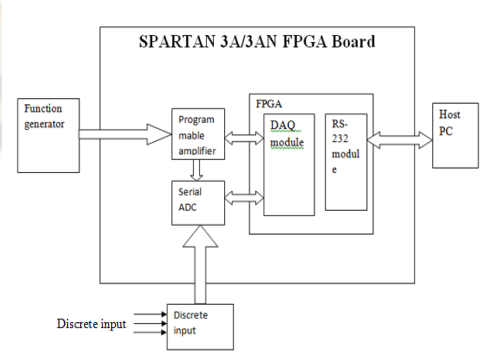


Fig 8. DAQ in Spartan 3A/3AN FPGA Board

### *A. Device Utilization Summary*

Selected Device: 3s700anfgg484-4

Table 2. Device Summary

| | |
|---|---|
| Number of Slices | 362 out of 5888 6% |
| Number of Slice Flip Flops | 342 out of 11776 2% |
| Number of 4 input LUTs | 606 out of 11776 5% |
| Number used as logic | 575 |
| Number used as Shift registers | 1 |
| Number used as RAMs | 30 |
| Number of IOs | 25 |
| Number of bonded IOBs | 10 out of 372 2% |

From the above synthesis report it is observed that the number of slices, LUTs, flip flops, shift register and IOs used by this paper is less.

### *B. Simulation Result for DAQ*

The simulation results for the DAQ is as shown in Fig 9 in which analog equivalent of digital data in hexadecimal in ADC output. The calculated output values for an input voltage level from 0.4 V to 2.9V for a gain of (-1) as shown in Table 3. The expected output value and measured output values are tabulated. The error also calculated and tabulated as shown. The percentage of error varies from .5% to maximum of 14% so that the accuracy achieved from this paper will be varied from 86% to 95.5%.


Fig 9. Final simulation result.

Table 3. Tabulated output values from the terminal and error calculation.

| vin | Decimal o/p expected | Hex o/p | | Hex o/p | Decimal Measured o/p | error | % of error |
|---|---|---|---|---|---|---|---|
| 0.4 | 8192 | 2000 | | 1fd7 | 8151 | 0.005005 | 0.50048828 |
| 0.5 | 7536.64 | 1D70 | | 1D49 | 7497 | 0.00526 | 0.52596382 |
| 0.6 | 6881.28 | 1AE1 | | 1AB9 | 6841 | 0.005854 | 0.58535621 |
| 0.7 | 6225.92 | 1851 | | 1852 | 6181 | 0.007215 | 0.72149979 |
| 0.8 | 5570.56 | 15C2 | | 15497 | 5527 | 0.00782 | 0.78196806 |
| 0.9 | 4915.2 | 1333 | | 1302 | 4866 | 0.01001 | 1.00097656 |
| 1.0 | 4259.84 | 10A3 | | 1078 | 4216 | 0.010291 | 1.02914663 |
| 1.1 | 3604.48 | 0E14 | | 0DE4 | 3556 | 0.01345 | 1.3449929 |
| 1.2 | 2949.12 | 0B85 | | 0B54 | 2900 | 0.016656 | 1.6655816 |
| 1.3 | 2293.76 | 08F5 | | 08C8 | 2248 | 0.01995 | 1.99497768 |
| 1.4 | 1638.4 | 0666 | | 636 | 1590 | 0.029541 | 2.95410156 |
| 1.5 | 983.04 | 03D7 | | 03A4 | 932 | 0.051921 | 5.19205729 |
| 1.6 | 327.68 | 0147 | | 121 | 289 | 0.118042 | 11.8041992 |
| 1.7 | -327.68 | FFFFFFFEB9 | 3E89 | FFFFFE89 | -375 | -0.14441 | -14.440914 |
| 1.8 | -983.04 | FFFFFFFC29 | 3BFA | FFFFFBFA | -1030 | -0.04777 | -4.7770182 |
| 1.9 | -1638.4 | FFFFFFF99A | 3968 | FFFFF968 | -1688 | -0.03027 | -3.0273437 |
| 2.0 | -2293.8 | FFFFFFF70B | 36D9 | FFFFF6D9 | -2343 | -0.02147 | -2.1466936 |
| 2.1 | -2949.1 | FFFFFFF47B | 344A | FFFFF44A | -2998 | -0.01657 | -1.6574436 |
| 2.2 | -3604.5 | FFFFFFF1EC | 31B9 | FFFFF1B9 | -3655 | -0.01402 | -1.4015891 |
| 2.3 | -4259.8 | FFFFFFEF5D | 2F2A | FFFFEF2A | -4310 | -0.01178 | -1.177509 |
| 2.4 | -4915.2 | FFFFFFECCD | 2C9A | FFFFEC9A | -4966 | -0.01034 | -1.0335286 |
| 2.7 | -6881.3 | FFFFFFE51F | 24EE | FFFFE4EE | -6930 | -0.00708 | -0.7080078 |
| 2.8 | -7536.6 | FFFFFFE290 | 2263 | FFFFE263 | -7581 | -0.00589 | -0.5885912 |
| 2.9 | -8192 | FFFFFFE000 | | 2000 | -8192 | 0 | 0 |

## VI. CONCLUSION AND FUTURE SCOPE

In this paper, and FPGA based platform is used to implement a data acquisition and processing system, as opposed to more traditional DSP or microprocessor platforms. We have achieved to get data rate of 1.5Msps and high accuracy of approximately 99% for our system. This paper describes the design of data acquisition system that is able to collect information from analog as well as digital. The SPI and Serial communication protocols are configured. SPI and serial transmission timing is very strict, so this paper design a reliable and stable clock generation and baud generation modules respectively.

Data transmission module is a simple and the transfer speed is faster. This paper has further future scope of improvements, they are to paper with real time signals and to improve the performance and data rate of analog signals.

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