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DTMF detection using Recursive DFT on FPGA

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Abstract

A low computational complexity and low cost recursive discrete Fourier transform (RDFT) design for DTMF application is proposed in this paper.The DFT is also used to efficiently solve partial differential equations, and to perform other operations such as convolution or multiplying large integers .There are lots of architectures available in literature which is of computing N point DFT type. Such algorithms are called as FFT computation algorithms. However in some applications we need to computer the DFT for some of selected output bin indices only. One of such example is signal monitoring and spectrum estimation technique in signal intelligence applications. The Dual-tone multi-frequency (DTMF) is also another example where we are specifically interested to see the energies at specific frequency values only. DTMF detection is used to detect DTMF signals in the presence of speech and dialling tone pulses.

A low power recursive discrete Fourier transform (RDFT) design is proposed in this project. The proposed algorithm reduces the hardware complexity which in turn reduces the memory. By this a considerable power saving is achieved. The recursive DFT is realized for DTMF detection applications. The architecture will be developed keeping DTMF requirements in consideration. The proposed algorithm will be implemented through VHDL. Modelsim (SE) will be used simulation. After verifying the simulation results the code will be synthesized on Xilinx FPGA.

Keywords - Dual tone multi frequency (DTMF), Recursive filters, recursive DFT

I. INTRODUCTION

The discrete Fourier transform (DFT) has been widely applied in the analysis and implementation of communication systems such as dual tone multi-frequency (DTMF)[1] .In this method ,the digits are represented with tones for transmission over an analog communication channel. DTMF tones are used by all touch tone phones to represent the digits on a touch tone keypad. DTMF technology provides a robust alternative to rotary telephone systems and allows user-input during a phone call. This feature has enabled interactive, automated response systems such as the ones used for telephone banking, routing customer support calls, voicemail, and similar applications. A DTMF tone consists of two superimposed sinusoidal signals selected from two frequency groups. The frequency groups represent rows and columns on a touch tone keypad as shown in Figure below. Each DTMF tone must contain one sinusoid from the high-frequency group (1209, 1336, 1477 and 1633 Hz) and one sinusoid from the low frequency group (697, 770, 852 and 941 Hz). This allows a touch tone keypad to have up to 16 unique keys.

The discrete Fourier transform (DFT) has been widely applied in the analysis and implementation of communication systems such as dual tone multi-frequency (DTMF) standards. In many applications, the complex sequences in the time domain are expected to be analysed in the frequency domain via DFT computation. Without loss of generality, the input data is assumed as complex-valued data.

In many applications, the complex sequences in the time domain are expected to be analyzed in the frequency domain via DFT computation. Without loss of generality, the input data is assumed as complex-valued data. From existing research, there are possible four categories for the structures of DFT/IDFT computations: 1) recursive-algorithm based architecture, 2) butterfly based architecture, 3) ROM operation based structure, and 4) multiplier-accumulator based structure

The architectures [5]–[10] for recursive DFT (RDFT) algorithms have been completely developed and have the advantages of high data throughput, low power use, and small area requirement compared to digital-signal processing-based designs. Recently, Van and Yang [9] and Van et al. [8] have proposed a high-performance and power-efficient very-large-scale integration (VLSI) architecture. However, the computational complexities (multiplications and additions) of these RDFT algorithms [7]–[10] are quite high; thus, a low-cost and low-computational-complexity version of the RDFT algorithm should be developed and explored. Recently, Laietal.[6] have proposed a novel RDFT algorithm for computing arbitrary-length DFTs. The computational complexity of this algorithm is still high, although the design does have low-cost and low-complexity advantages compared with other RDFTs. Fan and Su [5] presented a compact recursive method to compute 2n-point DFTs. The advantages of their design include fewer recursive loops and greater accuracy. However, this design cannot be applied to 212- and 106-point DFTs. Some approaches [3], [4] use trigonometric identities and addition and subtraction theorems to perform the

modified discrete cosine transform (MDCT) and recursive discrete cosine transform (DCT).

Recently, Kim et al. [2] have proposed the mixed prime-factor DFT algorithm with the Chinese remainder theorem (CRT) [15] to solve the problem of frame size unsupporting the radix-2n DFT and to reduce the number of multiplications. However, their design has higher hardware costs for implementing the non-radix 2n DFT circuit. An efficient solution is suggested adopting recursive architecture instead of parallel DFT architecture. In this way, the hardware costs can be reduced greatly.

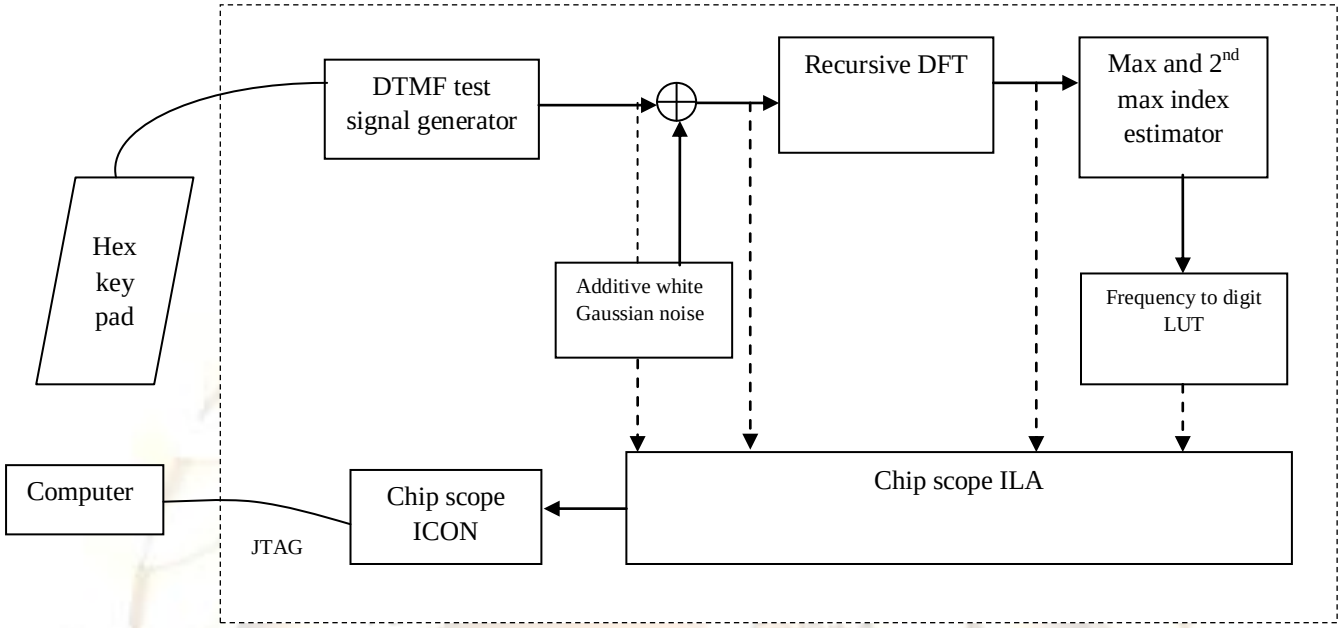

Fig.1. DTMF detection

II.RDFT Algorithm

The DFT formula can be derived as follows by reordering the index and expressing the sigma function:

$$X[k] = \sum_{n=0}^{N-1} x[n] * W_N^{nk}$$

$$= \sum_{n=N-1}^{0} x[N-1-n] * W_N^{(N-1-n)k}$$

$$= W_N^{-k}\left(x[N-1] + W_N^{-k} * x[N-2] + WN{-}2k{*} \quad xN{-}3{+}\ldots{+}WN{-}N{-}3{*}x0\right) \quad (1)$$

Then, it yields a recursive form as follows:

$$X[k] = W_N^{-k}(W_N^{-k}(W_N^{-k}(W_N^{-k}x[0] + x[1]) + x[2]) + \cdots + x[N-1]) \quad (2)$$

The kernel function of the difference equation is defined as

$$m[n] = W_N^{-k} = W_N^{-k}.(m[n-1] + xn. \quad (3)$$

The function *m* of *n* is derived as follows via (2) and (3), and then the output of *X*[*k*] will be obtained at time $n = N - 1$

$$x[k] = m[N\text{-}1]. \quad (4)$$

This means that the proposed algorithm uses the number of N iterative cycles for the whole DFT calculation. Now, the difference equation (4) can be expressed as a z-transform. The transfer function H(z) is obtained as

$$\frac{M[z]}{X[z]} = H[z] = \frac{W_N^{-k}}{1 - W_N^{-k}z^{-1}} = \frac{W_N^{-k}(1 - W_N^{k}z^{-1})}{1 - 2cos\theta(k)z^{-1} + z^{-2}} = \frac{cos\theta(k) + jsin\theta(k) - z^{-1}}{1 - z^{-1}(2cos\theta(k) - z^{-1})},$$

Where $\theta(k) = 2\pi k/N$ (5)

According to (4) and (5), it is easily mapped into a novel algorithm. To reduce the number of multiplications of cosθ(*k*) in the implementation, the coefficients of cosθ(*k*) and 2cosθ(*k*) can be shared. Then, all multiplications can be calculated using one real multiplier.

B. Recursive IDFT Formula

The IDFT of an N-point input sequence X[k] is defined as:

$$x[n] = \frac{1}{N}\sum_{k=0}^{N-1} X[k] * W_N^{-nk},$$

$$where\ n = 0\ to\ N-1$$

The efficient computational algorithm caused by the DFT and the IDFT involves the same kernel. After taking the complex conjugate of (13), the same kernel can be obtained, i.e.

$$x^*[n] = \frac{1}{N}\sum_{k=0}^{N-1} X^*[k] * W_N^{nk}$$

It can be seen that the IDFT can be performed by the DFT. The only difference is in the complex conjugate of the input/output sequence. In summary, there are three steps to achieving the recursive IDFT: First, take the complex conjugate of the input sequence. Then, apply the proposed DFT algorithm. Finally, take the complex conjugate of the output sequence divide it by N.

III. Block Diagram

The module DTMF (Dual tone multiple frequency) detection consists of

1. Hex key pad
2. DTMF test signal generator
3. Additive white Gaussian noise
4. Frequency Detection block
5. Magnitude / index estimator
6. Frequency to digit look-up table

A. Hex keypad:

Hex Keypad gives input to the module. It is an external component. In case of unavailability of hex keypad, the input is given from slide switches in FPGA.

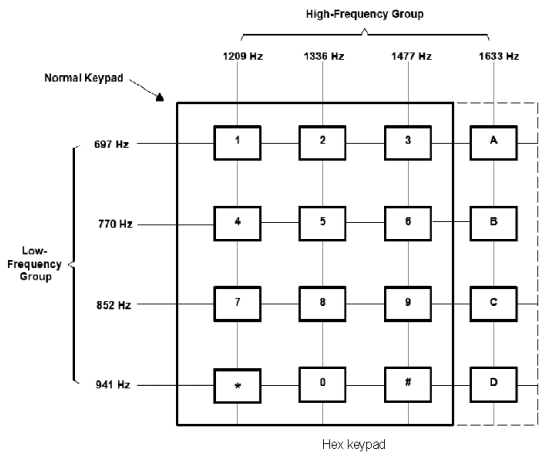

Fig.2. Hex keypad

B. DTMF test signal generator:

This block generates the carrier frequencies necessary. It consists of

B.1. Frequency word selector:

In this block the carrier waves are generated For example: If key 5 is being press the frequencies that are generated are 770 Hz(Low frequency group) and 1336 Hz (High frequency group). These frequency waves are generated by a DDS core.

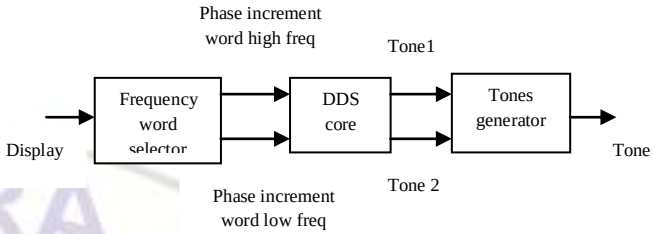

Fig.3. Internal blocks of DTMF test signal generator

B.2. DDS Core: The Logic CORE™ IP DDS (Direct Digital Synthesizer) Compiler core sources sinusoidal waveforms for use in many applications. DDS digitally generates a complex or real-valued sine wave. Due to the digital nature of the DDS functionality, it offers fast switching between output sine wave frequencies, fine frequency resolution, and operations over a broad frequency range. Core DDS can generate a sine or cosine waveform as well as the complex sinusoid. The DDS can be set to generate a waveform of a constant frequency and phase shift, or configured so the phase and frequency can be modulated at run time. A DDS consists of a Phase accumulator and a SIN/COS Lookup Table. These parts are available individually or combined via this core. Direct digital synthesis (DDS) is a method of producing an analog waveform—usually a sine wave— by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. Today's DDS devices are very compact and draw little power. The blocks of Direct Digital Synthesizer (DDS) are given below.

- Phase accumulator
- COS carrier generator.

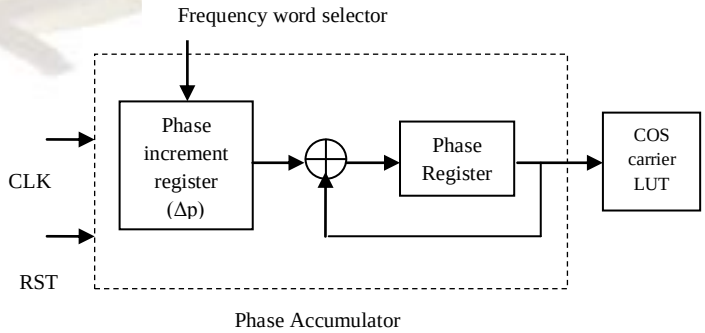

Fig.4.Direct Digital Synthesizer

B.2.1. Phase Accumulator:

The modulation controller loads phase increment value with one (ΔP=1) to generate, output frequency corresponding to input symbol '0' and with two (ΔP=2) which is to generate output frequency corresponding to input symbol '1'. This phase increment value is given by frequency word selector. The value of phase increment is calculated by the formula $\Delta P = (fs * 2^j)/ f_{clk.}$

Table.1.Phase Increment Values For 8 Different Frequencies

Frequency	*Phase increment value*	*(in hex)*
697	5846859.776	59374B
770	6459228.16	628F5C
852	7147094.016	6D0E56
941	7893680.128	7872B0
1209	10141827.07	9AC083
1336	11207180.29	AB020C
1477	12389974.02	BD0E56
1633	13698596.86	D10624

Where f_{clk} = 8kHz

Digital phase accumulator gives the instantaneous phase of a cosine signal according to a phase increment value (frequency word) given as input to accumulator by BFSK modulation controller.

When the accumulator exceeds a value equivalent to 2pi radians, it overflows, multiples of 2pi are discarded, and the incrementing process continues to the next cycle. The output of phase accumulator will produce synthesized instantaneous digital phase, which will be used to address the LUT.

B.2.2. COS carrier LUT:

The phase bits given by the accumulator is used to address a look-up table held in ROM (read-only memory) which gives corresponding amplitude bits. The COS carrier LUT consists of phase Vs amplitude table corresponding to one COS waveform.

B.2.3. Clock and control signal generator:

The phase accumulator has to reset (phase register becomes zero) whenever a new symbol is taken from frequency word selector. This is achieved by resetting the phase accumulator. The clock input for phase accumulator has to be derived from the master clock so that the output wave form gets an integer number of cycles for every symbol. The Clock distributor and control signal generator blocks generates necessary signals for above two requirements.

B.3. Tones generator:

The main propose of this block is take two cosine waves from DDS cores and add them in order to produce one wave called tone out.

C. Additive white Gaussian Noise:

The tone out, which is the output from tones generator, is mixed with noise in this module. The output is named as noise bits. Wideband Gaussian noise comes from many natural sources, such as the thermal vibrations of atoms in conductors (referred to as thermal noise or Johnson-Nyquist noise), shot noise, black body radiation from the earth and other warm objects, and from celestial sources such as the Sun. The AWGN channel is a good model for many satellite and deep space communication links. It is not a good model for most terrestrial links because of multipath, terrain blocking, interference, etc. However, for terrestrial path modelling, AWGN is commonly used to simulate background noise of the channel under study, in addition to multipath, terrain blocking, interference, ground clutter and self interference that modern radio systems encounter in terrestrial operation.

D. Frequency Detector:

The frequency detector block is RDFT core. Input to this module is noise bits, which is the output from additive white Gaussian noise. Output of the block is indices and magnitudes.. The RDFT algorithm is a digital signal processing (DSP) technique for identifying frequency components of a signal. While the general Fast Fourier transform (FFT) algorithm computes evenly across the bandwidth of the incoming signal, the RDFT algorithm looks at specific, predetermined frequencies. Some applications require only a few DFT frequencies.

One example is frequency-shift keying (FSK) demodulation, in which typically two frequencies are used to transmit binary data; another example is DTMF, or touch-tone telephone dialing, in which a detection circuit must constantly monitor the line for two simultaneous frequencies indicating that a telephone button is depressed.

RDFT algorithm reduces the number of real-valued multiplications by almost a factor of two relative to direct computation via the DFT equation. The recursive form of DFT algorithm is as follows.

$$X[k] = W_N^{-k}(W_N^{-k}(W_N^{-k}(W_N^{-k}x[0] + x[1]) + x[2]) + \cdots + x[N-1]) \quad (8)$$

E. Magnitude/Index Estimator:

In this block, the magnitudes are calculated at different frequencies. For all 256 samples the magnitudes are calculated in each RDFT block. Among all high frequencies which sample is having maximum magnitude and similarly for low

frequencies which low frequency is having maximum magnitude are estimated and given to frequency to digit LUT. Instead of calculating magnitude with conventional square root of[(x*x) +(y*y)], it is calculated by [x+(y/2)] , where 'x' is max and 'y' is the min of real and imaginary parts of the output of RDFT block respectively.

F. Frequency to Digit Look-up table:

In this block, 8 different 7 bit values are taken for 8 different frequencies which are unique in the peak_index for identification of corresponding keys pressed. For example

"0100" when "00100100011111",
means that 0010010=>697 Hz

0011111=>1209 Hz. That means it is concluded that if two frequencies that are assigned to 7 bit value which are unique are concatenated, then corresponding key has been detected. In the above case digit _1'has been detected. Likewise for all 16 digits in keypad.

III. SIMULATION AND IMPLEMENTATION

A low power recursive DFT for DTMF application is implemented on FPGA successfully. The circuit description is done using VHDL language and use ModelSim SE 6.2c software to verify the function. This simulation is called software simulation. Synthesis is done by using XST (xilinx synthesis tool) which is from xilinx ISE 9.2i. After the synthesis, bit file is generated. Bit file is dumped on to the FPGA hardware by using IMPACT tool. Xilinx chip scope tool will be used for on chip verification. This is called hardware simulation.

IV.CONCLUSION

This brief has presented low-complexity low-cost fast computing architecture for RDFT algorithm. The proposed algorithm and architecture not only outperform previous works but can also be implemented using simple hardware .This design is suitable for DTMF detecting in voice-over-packet (VoP) applications.

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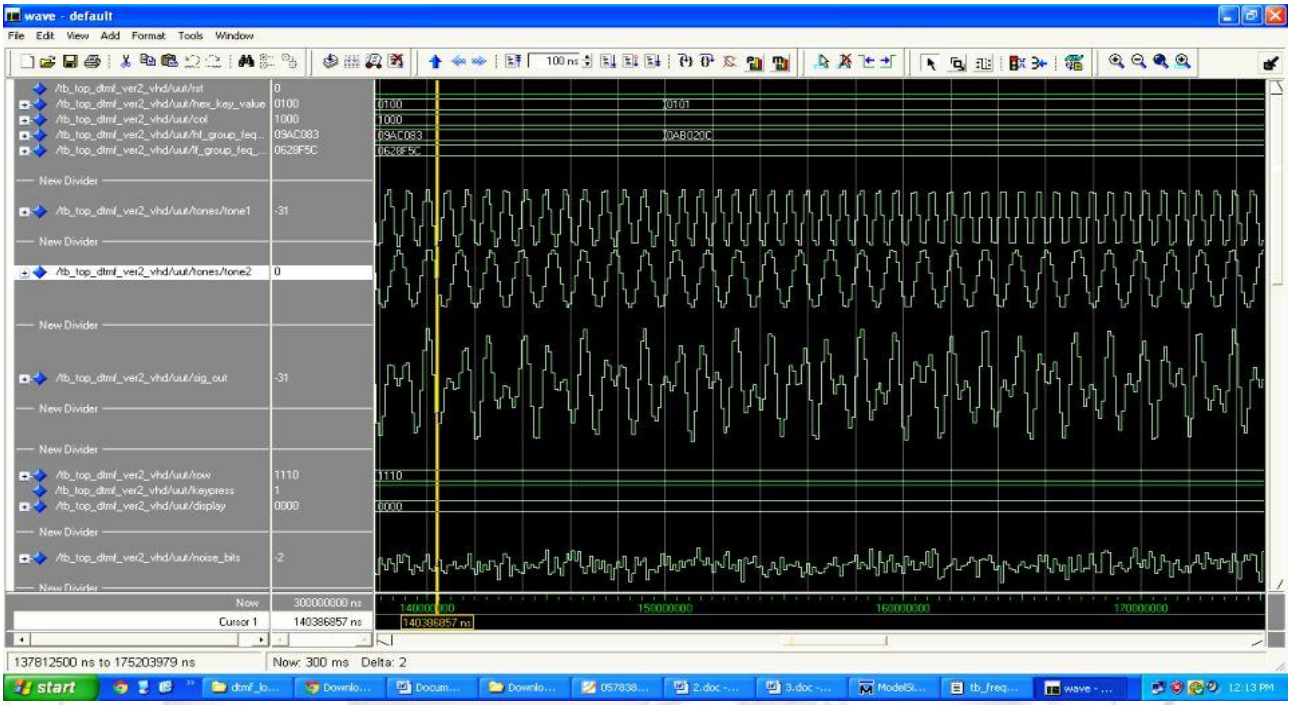

Fig.5. DTMF signal or sig_out

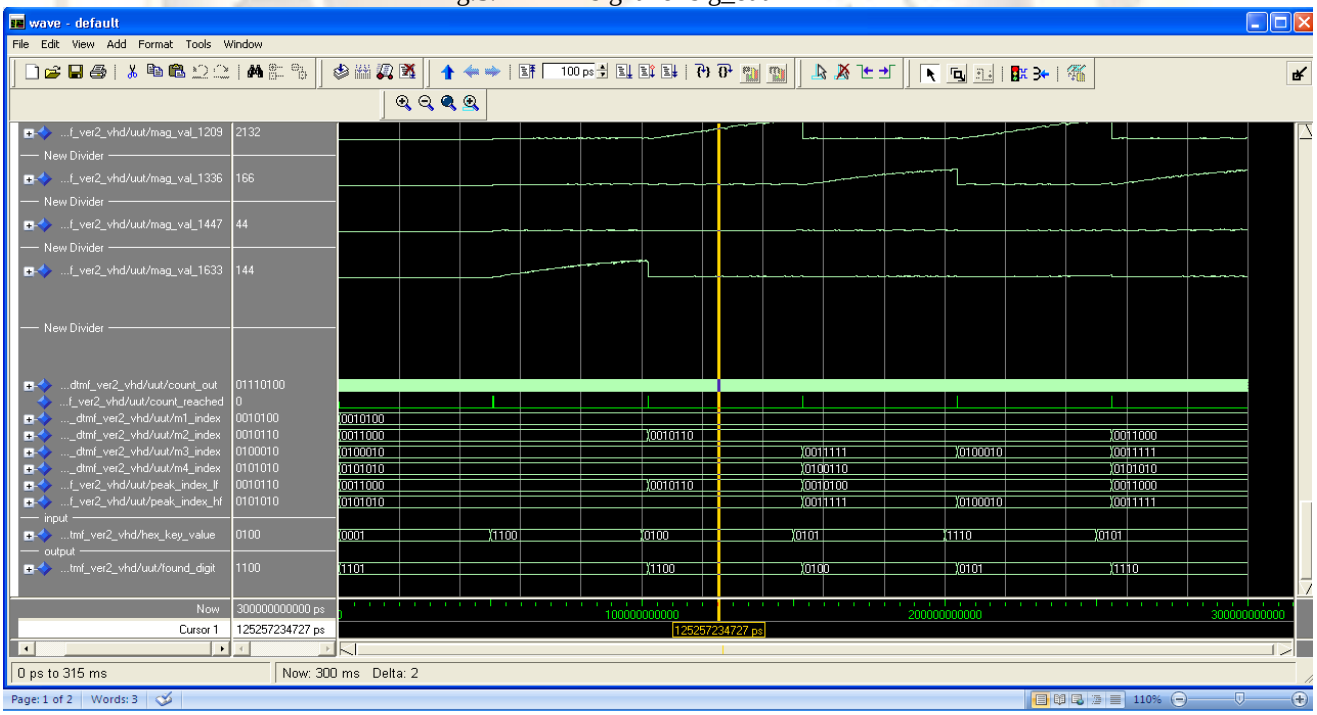

Fig.6. Output showing found digit or output digit