

Design and Simulation of High Speed Digital Phase Locked Loop

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Abstract: -

The digital phase locked loop is a circuit that used frequently in modern integrated circuit design. A digital phase-locked loop (DPLL) is designed using 0.18 μm CMOS process and a 3.3 V power supply. It operates in the frequency range 200 MHz–1 GHz. DPLL perform the function of generating a clock signal, which is locked or synchronized with the incoming signal. It consist of single charge pump (CP), low pass filter (LPF) and voltage controlled oscillator (VCO). DPLL circuit components as well as implementation using Tanner design tools are presented. Spectra simulations were also performed and demonstrated a significant improvement in the lock time of the DPLL.

Keywords — PFD, CP, LPF, VCO.

I. Introduction

With ever increasing performance requirements of microprocessors, more stringent requirements have been placed on clock generation networks. At heart of the clock generation networks is the digital phase locked loop (DPLL)..Phase-locked loops (DPLLs) are commonplace in applications like wireless transceivers, global positioning systems, clock generators and so on.

It is a feedback system that compares and locks the phase and frequency of an input signal respect to the available reference signal. A major characteristic of the DPLL is the lock time; it is the time that PLL takes to adapt and settle after a sudden change of the input signal frequency. The comparison is generally performed by a phase and frequency comparator which is technically known as phase frequency detector (PFD). The phasefrequency detector compares the phase of a periodic input signal against the phase of the VCO. Output of the PFD is a measure of the phase difference between its two inputs. The difference voltage is then filtered by the loop filter and applied to the VCO. The control voltage on the VCO changes the frequency in a direction that reduces the phase difference between the input signal and the oscillator [1]. When the loop is locked, the control voltage is such that the frequency of the VCO is exactly equal to the average frequency of the input signal.. As long as the initial difference between the input signal and the VCO is not too big, the PLL eventually locks on to the input

signal [7]. This period of frequency acquisition, is referred as pull-in time, this can be very long or very short, depending on the bandwidth of the PLL. The bandwidth of a PLL depends on the characteristics of the phase detector, voltage controlled oscillator and on the low pass filter .The output of the PFD is fed to a charge pump circuit to get a constant current at the output. The charge pump output is passed through a low pass filter to generate the control voltage for the VCO circuit. Hence there are four functional blocks in a DPLL circuit such as phase frequency detector (PFD), charge pump, low pass filter(LPF) and voltage controlled oscillator (VCO) [1,7] .

With Examples of conventional digital phase-locked loops (DPLLs) using 0.18 μm CMOS process are given in [1, 2]. The DPLL in [1] is a 55 MHz–1.43 GHz one with a lock time of 840 ns at 1 GHz and 1.22 ms at 1.43 GHz. The DPLL in [2] is a 1 GHz one with a lock time of 643 ns at that frequency. These two examples represent the state-of-the-art of conventional DPLLs using 0.18 μm CMOS process.

II. BLOCK DIAGRAM OF THE FLASH DPLL

The original block diagram of the Digital Phase locked loop is shown in Fig. 1. The circuit quickly and simultaneously compares the input frequency with many equispaced fixed frequencies covering the entire anticipated frequency range of operation. The diagram of a charge-pump based DPLL is shown in Fig.1

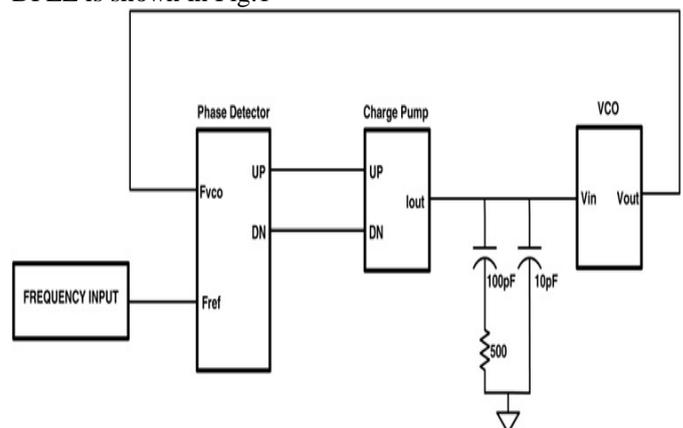


Fig 1 : Block diagram of the phase locked loop.

III. DESIGN OF THE DPLL

The circuit components of the DPLL of Fig.1 are given below:

a phase frequency detector (PFD), a charge pump, low pass filter and a voltage controlled oscillator

A . Phase frequency detector

The block diagram of the phase-frequency detector (PFD) is given in fig 2.. The PFD circuit is used to find the difference in phase and frequency between the two input signals reference frequency (Fref) and input frequency (Fin) which is fed back from the output of the VCO. It generates two output signals UP and DOWN that switches the output current of the pump. The outputs UP and DN (Down) depend on the frequency and lead/lag relationship between the input Fin and Fvco (VCO output frequency). When the loop is locked, the UP and DN remain low. [8]

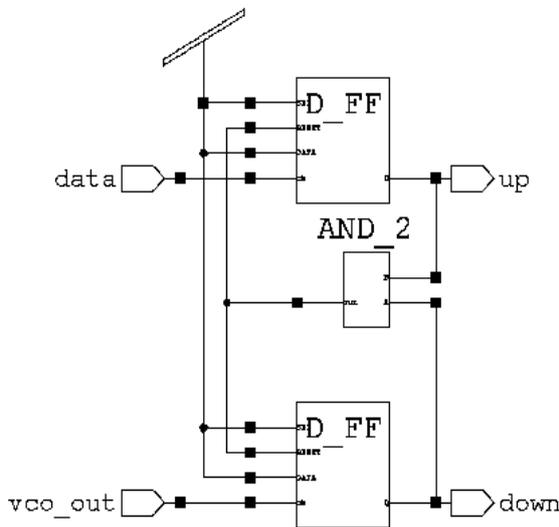


Fig2: Phase frequency dtector

The PFD implementation using inverters and nand gates as seen in fig 3. when the vco-out is lagging, the data the output of the PFD is the up pulse (indicating that the vco-out needs to speed up or occur earlier in time, that is VCO's control voltage should increase) when data is lagging Vco-out the down pulse goes high indicating vco_out should slow down [3,7].

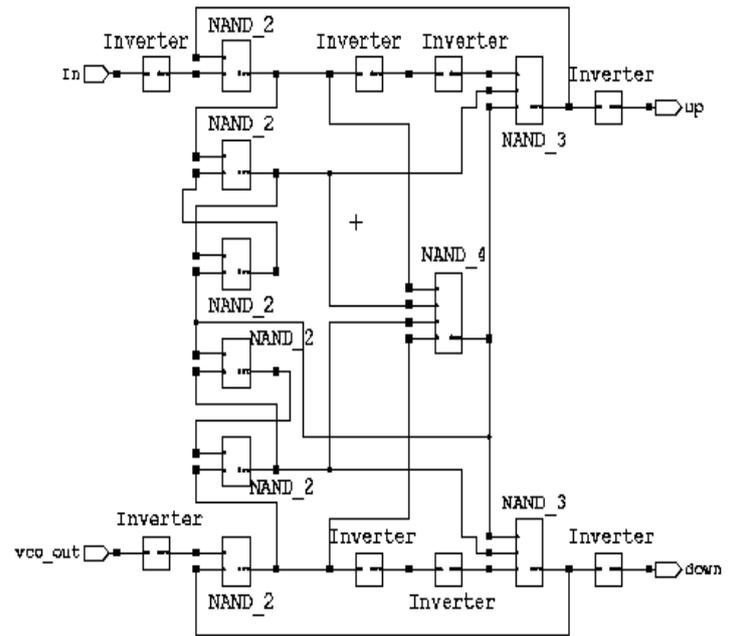


fig 3: Implementaion of PFD

B. Single Charge pump (CP) and LPF

A single CP and LPF is shown in Fig. 4. Charge pump is one of the important parts of PLL which converts the phase or frequency difference information into a voltage, used to tune the VCO. A precise current mirror is used to remove instability and ripple in the control voltage. The output control voltage Vctrl will increase/decrease depending on whether the UP/DN pulse occurs. Shown that MOS1 and MOS2 which placed in series, when PFD up signal goes high MOS2 turns on connecting the current source to the LPF.

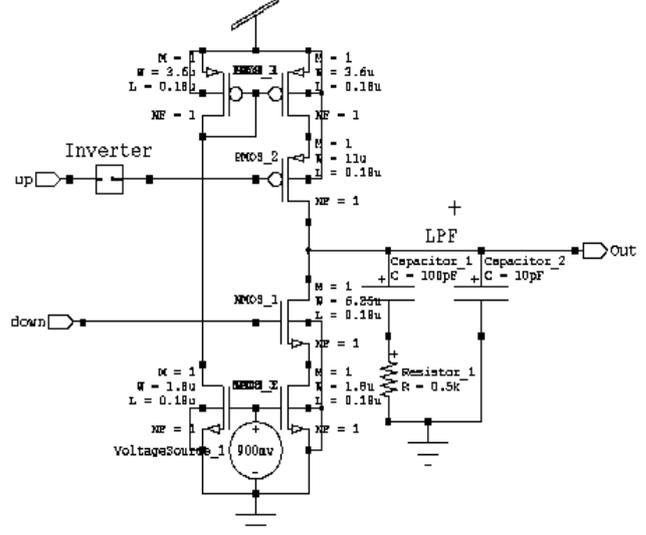


Fig 4: Single CP and LPF

A. Voltage-controlled oscillator

A current-starved VCO is built shown in fig 5, which is basically composed of an odd number of inverter stages, as given in [8]. For proper operation, M4 (connected to VDD) and M5 (connected to the VCO input Vcntrl) have to operate in the saturation region. The VCO oscillation frequency is given by [8].

$$f_{osc} = \frac{1}{N(t1 + t2)} = \frac{I_D}{N * C_{tot} * V_{DD}} \quad (1)$$

Where C_{tot} is the total load capacitance at the drain of inverters, and $t1$ and $t2$ are the charge and discharge times. A five-stage VCO was used because it requires less input voltage than that of a seven- or nine-stage VCO. Table 1 shows the required voltages needed to produce a specific frequency. Two inverters were used at the VCO output to give sharp waveform edges.[5,6]

In order to test the VCO, a ramp was used at the input to allow oscillations to begin. The ramp was set up to 1.36 V. The resulting F_{vco} was 2 GHz which agrees with Table 1.

TABLE 1
VCO FREQUENCY AGAINST VOLTAGE (VCNTRL)

Frequency	Voltage (Vcntrl)
250 MHz	865 mV
500 MHz	1.038 V
750 MHz	1.14 V
1 GHz	1.2 V
1.25 GHz	1.25 V
1.5 GHz	1.28 V
1.75 GHz	1.32 V
2 GHz	1.36 V

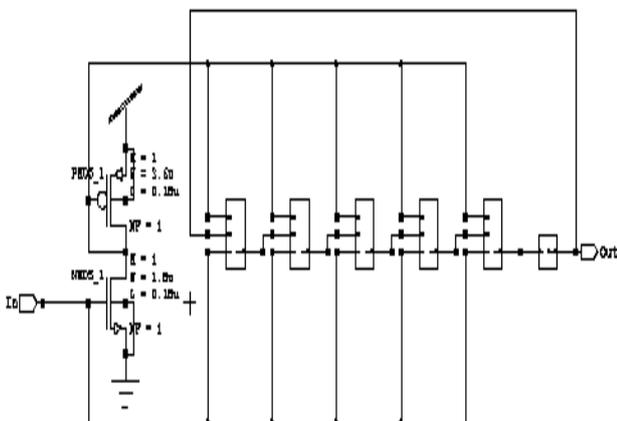


Fig 5: Voltage-controlled oscillator

IV. IMPLEMENTATION AND SIMULATIONS OF THE DPLL

To prove that the DPLL which locks the phase, Fig. 6 shows part of the DPLL, namely it is PFD, CP LPF and VCO. Many examples were performed in the frequency range 300 MHz–2 GHz. To determine the lock time, the voltage (Vcntrl) from the CP was monitored and the input frequency (F_{in}) was compared with the output frequency (F_{vco}). The DPLL is considered to be locked. The phase shift between F_{vco} and F_{in} becomes zero or constant. Example simulations for the frequency range 300 MHz–1.8 GHz are shown in Fig. 7.

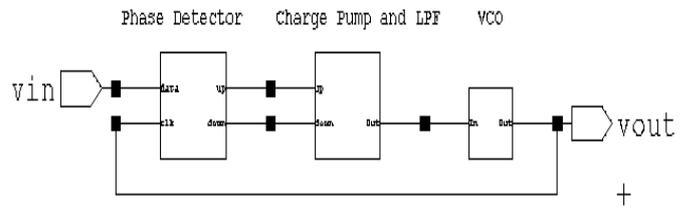


Fig 6:PLL simulation schematic

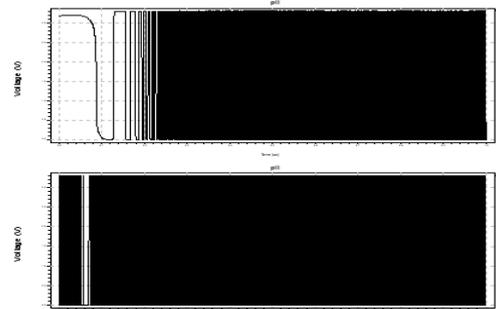


Fig7::PLL Result

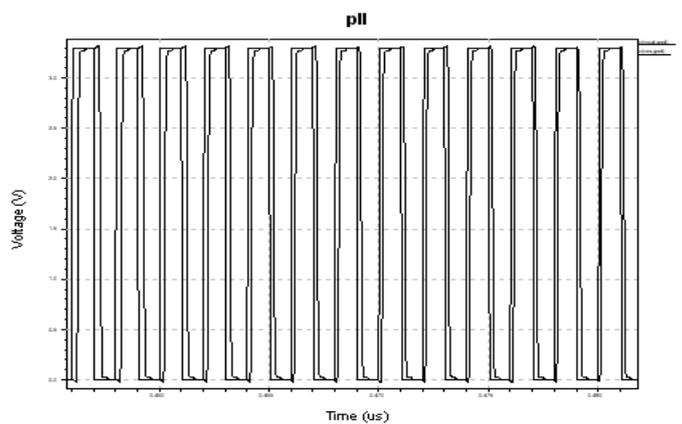


Fig7: Conventional DPLL 300 MHz–1.8 GHz (zoomed to view waveforms at locking) locked at .47μs

V. CONCLUSIONS

In this paper we presented a PLL with a better lock time which is designed in CMOS .18μm technology. The lock time of the PLL mainly

depends upon the of PFD architecture used and the parameters of the charge pump and LPFfilter. So by properly choosing the PFD architecture and adjusting the charge pump current and the loop filter component values we can achieve a better lock time. The simulation for the phase noise performance of the

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