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QCA Estimation of Low Power Reversible Circuits

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Abstract:

In recent years low power and small size are the keyword in the IC industry. This is where the importance of reversible gate and QCA (Quantum dot cellular automata) comes in. In non- reversible gates there is a definite amount of power loss involved. Interest in reversible computation arises from the desire to reduce heat dissipation, thereby allowing – higher densities and higher speed. The QCA offers a new transistor-less computing paradigm in nanotechnology. It has the potential for attractive features such as faster speed , smaller size and low power consumption than transistor based technology .By taking the advantages of QCA we are able to design interesting computational architecture. In this paper we are proposing a reversible gate and implementation of basic gates in reversible gate in QCA. Also comparisons with existing technologies are done.

I. Introduction:

Latest trend in IC technology involves scaling down as well as low power consumption and dissipation. According to Landauer's research, the amount of energy dissipated for every irreversible bit operation is at least, KTln2 joules, where K=1.3806505*10-23m2kg-2K-1 (joule/Kelvin-1) is the Boltzmann's constant and T is the temperature at which operation is performed [1]. (fig.1). A reversible circuit must have as many inputs as outputs. It's output should be balanced and unique. That is there should be a one to one correspondence between input and output. Power dissipation of reversible circuit, under ideal physical circumstances, is zero.

Quantum logic circuits are created by orientating pairs of quantum cells so that their

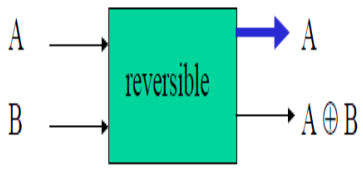


Fig.1 Reversible Logic Gate

relative positions determine their effect on each other. This is functionally analogous but structurally different from how individual gates in integrated circuits are combined to create logical and memory circuitry. The advantages of quantum-dot cellular automata over conventional circuitry are extremely small size/high density, low power requirements, and potentially high processing speeds. Disadvantages are difficulty of fabrication and low yield.

This paper is organized as follows: Section 2 gives the brief introduction of the reversible logic gates required for the present work. Section 3 describes the QCA. Section 4 gives comparative study of different reversible gates in QCA. Finally Section 5 concludes with a scope for further research.

II. Reversible Gates

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Also, in the synthesis of reversible circuits direct fan-out is not allowed as one–to-many concept is not reversible. However fan-out in reversible circuits is achieved using additional gates. A reversible circuit should be designed using minimum number of reversible logic gates.

For any deterministic device to be reversible

- The first condition is that its input and output be uniquely retrievable from each other - then it is called logically reversible.
- The second condition: a device can actually run backwards - then it is called physically reversible.
- and the second law of thermodynamics guarantees that it dissipates no heat.

From the point of view of reversible circuit design, there are many parameters for determining the complexity and performance of circuits .

- The number of Reversible gates (N): The number of reversible gates used in circuit.
- The number of constant inputs (CI): This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function.
- The number of garbage outputs (GO): This refers to the number of unused outputs present in a reversible logic circuit. One cannot avoid the garbage outputs as these are very essential to achieve reversibility.

- Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit.

2.1 Basic Reversible Gates

Feynman Gate: Fig.2 shows a 2*2 Feynman gate. The input vector is I (A, B) and the output vector is O(P, Q). The outputs are defined by P=A, Q=A⊕B. Quantum cost of a Feynman gate is 1.

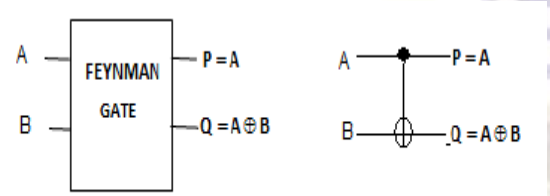


Fig.2 Feynman Gate

Double Feynman Gate (F2G): Fig.3 shows a 3*3 Double Feynman gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C. Quantum cost of double Feynman gate is 2.

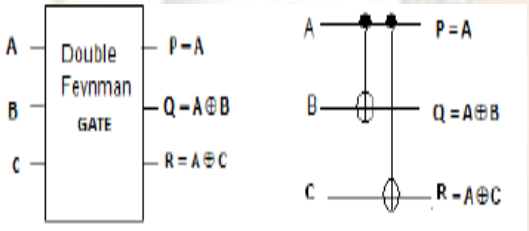


Fig.3 Double Feynman Gate

Toffoli Gate: Fig 4 shows a 3*3 Toffoli gate. The input vector is I(A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB⊕C. Quantum cost of a Toffoli gate is 5.

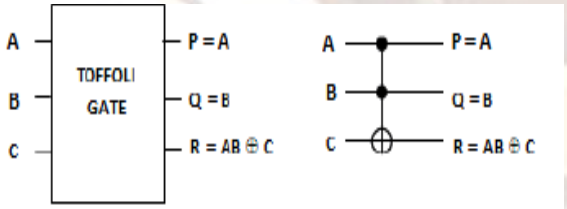


Fig.4 Toffoli Gate

Fredkin Gate: Fig 5 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B⊕AC and R=A′C⊕AB. Quantum cost of a Fredkin gate is 5.

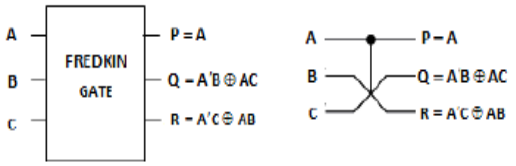


Fig.5 Fredkin Gate

Peres Gate: Fig 6 shows a 3*3 Peres gate . The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A⊕B and R=AB⊕C.Quantum cost of a Peres gate is 4.

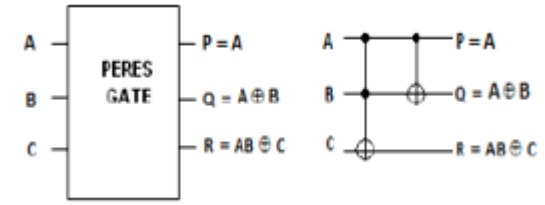


Fig.6 Peres Gate

Double Peres gate: Fig 7 shows a Double Peres Gate. The input vector is I (A, B, C,D) and the output vector is O (P, Q, R,S). The output is defined by P = A, Q = A⊕B, R=A⊕B⊕D and S=(A⊕B)D⊕AB⊕C.Iits quantum cost is calculated to be equal to 6 from its quantum realization.

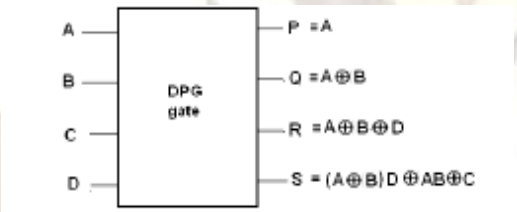


Fig.7 Double Peres Gate

Sayem gate : SG is a 1 through 4x4 reversible gate. The input and output vector of this gate are, Iv = (A, B, C, D) and Ov = (A, A'B ⊕ AC, A'B ⊕ AC⊕ D, AB ⊕ A'C ⊕ D). The block diagram of this gate is shown in Fig 8.

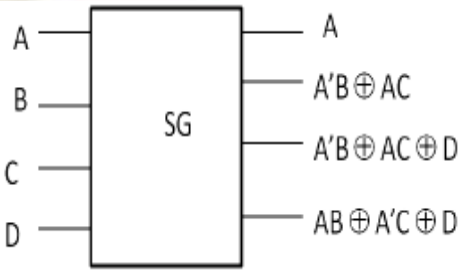


Fig.8 Sayem Gate

TS gate: TS Gate(TSG) is a 4*4 one through reversible gate. It can be verified that the input pattern corresponding to a particular output pattern can be uniquely determined. The input vector is I (A, B, C,D) and the output vector is O (P, Q, R,S). The output is defined by P = A, Q = A'C'⊕B', R= (A'C'⊕B')D and S=(A'C'⊕B')D⊕(AB⊕C).

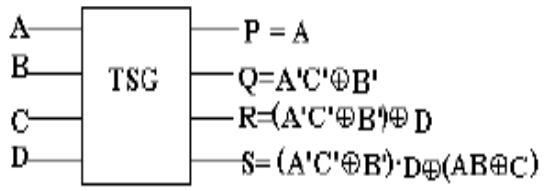


Fig.9 TS Gate

BME gate: BME gate is another new 4*4 reversible logic gate. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S).The output is defined by P=A, Q = AB⊕C,R=AD⊕C and S= A' B⊕C⊕D. The block diagram of BME gate is shown in Fig 10.

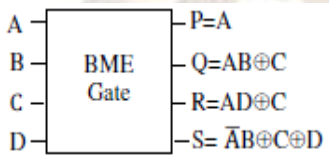


Fig.10 BME Gate

2.2 Proposed 4*4 reversible Gate

Here we are proposing a 4*4 Reversible gate for sequential circuits called KAS gate, as shown in fig 11. The input and output vector of this gate are, Iv = (A, B, C, D) and Ov = (A, A'B ⊕ AC, A'B ⊕ AC⊕ D, AB ⊕ C'). Its truth table is given in Table 1. Also it is realized using Verilog in Xilinx. The waveforms are given in Fig.12. Also D-latch realization using the proposed gate is discussed.

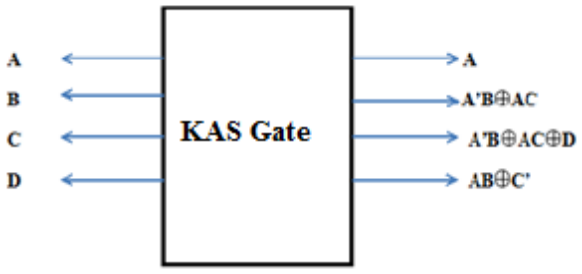
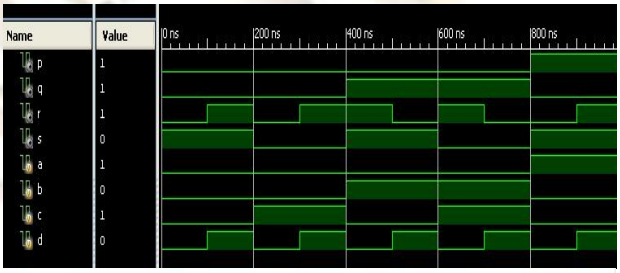


Fig.11 KAS Gate

Truth Table

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	0
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	1
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1

Table1: Truth Table



Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	2	4656	0%
Number of 4 input LUTs	3	9312	0%
Number of bonded IOBs	8	232	3%

Fig 12 Proposed Gate Waveform

D-latch

The characteristic equation of D-Latch is *Q+ =DE+E'Q*. It can be realized with one gate. It can be mapped with KAS by giving E, Q, D and 0 respectively in 1st, 2nd, 3rd and 4th input of KASG. Fig 13a shows the design of D-Latch with only Q output and Fig 13b shows the design of reversible D-Latch with both the output Q and Q+ .One Feynman Gate is needed to copy and produce the complement of Q from KASG for the design of Fig 13b.Fig.14 gives the necessary waveforms.

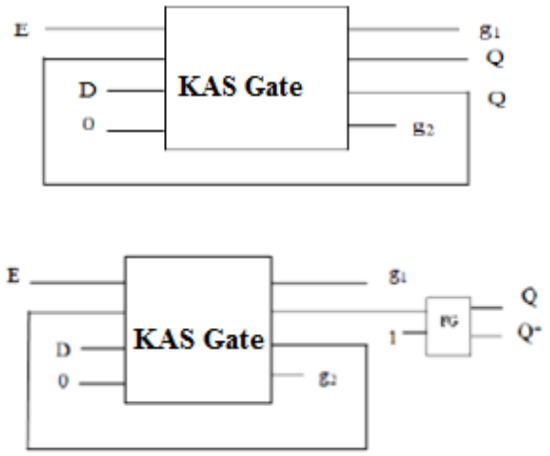


Fig.13 (a) D-latch implementation with Q o/p
(b) D-latch implementation with Q and Q^+ o/p

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	2	4656	0%
Number of 4 input LUTs	3	9312	0%
Number of bonded IOBs	6	232	2%

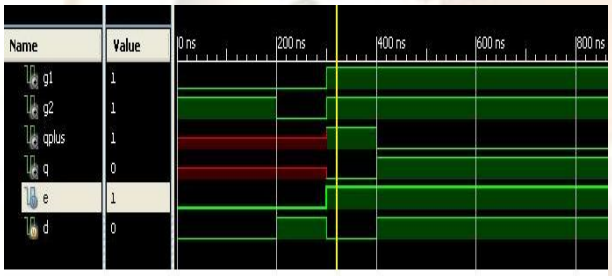
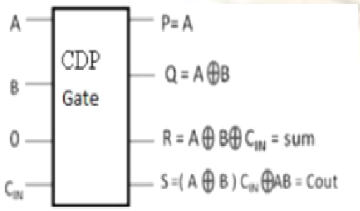


Fig.14 D-Latch waveforms

2.3 Cascaded Dual Peres Gate

The Cascaded Dual Peres Gate is shown in figure 15. The inputs and outputs are as shown in Table.2.The full adder using CDPG is obtained with C=0 and D= Cin and its quantum cost is calculated to be equal to 6 from its quantum realization [3] shown in Figure. 8



.
Fig.15 CDP Gate

INPUTS				OUTPUTS			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	1	0

Table 2.Truth Table of CDPG

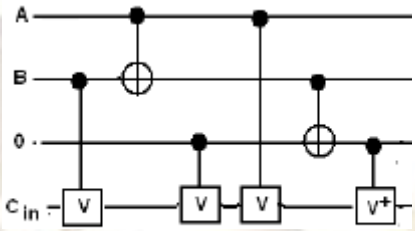


Fig 16.Full Adder using CDP Gate

A number of reversible full adders were proposed in. The proposed full adder using CDPG in Figure 16 requires only one reversible gate (one CDP gate) and produces only two garbage outputs. Hence, the full-adder design in Figure 16 using CDP gate is better than the previous full-adder designs in literature.

2.4 HIGH SPEED ADDER DESIGN

In this work the design of Carry Ripple Adder and Carry Select Adder is discussed. The delay of both the adders is compared and the high speed adder is selected for multiplier design.

Ripple Carry Adder: The full adder is the basic building block in the ripple carry adder. The full adder circuit using the proposed CDPG is used in this design. The ripple carry adder is obtained by cascading the full adders in series.(Fig 17).

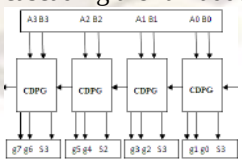


Fig 17. Ripple carry adder using CDPG full adder

It is clear from the above figure that for N – bit addition the proposed Ripple carry adder architecture uses only N reversible gates and produces only 2N garbage outputs. There also exists several Ripple carry adders in literature, but the proposed one is optimized.

Carry Select Adder: In Carry select adder two ripple carry adders are used one with input carry as zero and other with input carry as one. Based on the original input carry the output is selected from one of the adders using a multiplexer. Separate multiplexers are used for sum and carry out selection. In the proposed design Fredkin gate is used as multiplexer.

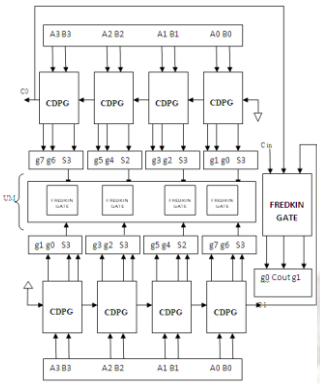


Fig 18. Reversible Carry select adder

III. Quantum dot cellular Automata

A QCA cell can be viewed as a set of four charge containers or "dots", positioned at corners of a square. The cell contains two extra mobile electrons which can quantum mechanically tunnel between dots, but not cells. The electrons are forced to the corner positions by Coulombic repulsion. The two possible polarization states represent logic "0" (polarization P = −1) and logic "1" (polarization P = +1), as shown in Fig.19. Unlike conventional logic circuits in which information is transferred by electrical current, QCA operates by the Coulombic interaction that connects the state of one cell to the state of its neighbors. This results in a technology of which information transfer (interconnection) is the same as information transformation (logic manipulation). Each cell has a side dimension of 18nm.

3.1 Clock

QCA circuits need a clock not only to synchronize and control the flow of information but also to provide the necessary power for the correct operation of the circuit. Contrary to the CMOS standard clock QCA clock has more phases. This schedule provides the power in addition to controlling the information flow in the circuit and reduces the power consumption. It also has the pipeline capability. The clock signal in the quantum cellular automata is multiphase. In fact, one array in QCA cells is divided into subarrays which hold advantages including multiphase clock and pipeline. The clock can do special calculations in a subarray and the generated output can act as the input for the next subarray. The cells of each zone of the clock signal make particular calculations. Then, the state of this zone becomes stable and can be applied as the input signal of the next zone. In the first phase which is the switch phase, the cells are firstly in non polar state and then they will be polarized. In this phase, the actual calculations are done. The second phase is hold, the third is release, and the forth is relax zone. In the third phase, the cells are in the low state and change into a non polar state. In the fourth phase, the cells are settled in the non polar state. Figure 20 shows the four phases of the clock in QCA.

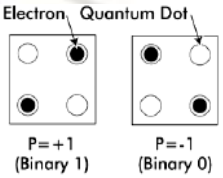


Fig 19 QCA cells showing how binary information is encoded in the two fully polarized diagonals of the cell

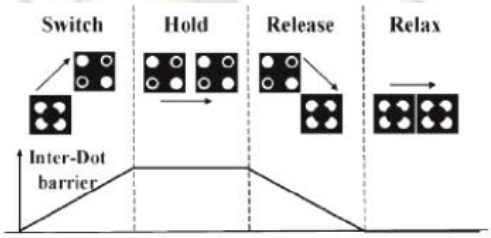
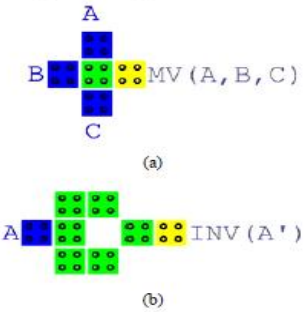


Fig 20 Clock phases in QCA

3.2 Implementation of Different Gates in QCA

One of the basic logic gates in QCA is the majority voter (MV) . The majority voter with logic function MV (A, B, C) = AB + AC + BC, which can be realized by only five QCA cells, as shown in Fig. 21. Logic AND and OR functions can be implemented from the majority voter by setting one input (the so-called programming or control input) permanently to a 0 or 1 value. The inverter is the other basic gate in QCA. Besides, an XOR gate forms an important gate in the QCA design of reversible gates.



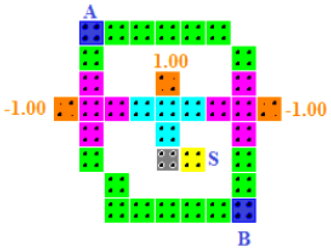


Fig.21 Implementation of various basic gates in QCA.(a)AND/OR (b)NOT (c)XOR Gates

IV. Comparison of different reversible gate implementation in QCA:

The comparison of various reversible gate with proposed KAS gate is shown in table 3. From the table it is clear that KAS gate is better than others

Gate	I/P & O/P Count	No. of gates	No. of cells
Sayem gate	4	9	161
BME Gate	4	8	150
TS Gate	4	9	159
KASgate	4	8	125

Table3 Comparison of gates

V. Conclusion

In this paper, Basic reversible gates were implemented using QCA. The gate is very useful for the future computing techniques like ultra low power digital circuits and quantum computers. The use of gate in the design and development of combinational and sequential circuits would prove to be beneficial in respect of power saving, reduction of garbage outputs and less amount of delay. Besides, being reversible will enjoy low energy dissipation, simple testability and increased fault detection features.

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