Design of Efficient Multi-Modulus Counter Using Low Power 2/3 Counter

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ABSTRACT

In this paper, an efficient multi-modulus counter is proposed to utilize both the counting logic and the mode preference control. This can be used to selectively divide the input frequency among multiple integer values. This can enhance the working frequency of the counter due to a reduced critical path between the E-TSPC flip flops.

Keywords- Extended true-single-phase clock flip flops (E-TSPC FF), prescaler.

1. INTRODUCTION

High speed N/N + 1 counter (also called prescaler) is a fundamental module for frequency synthesizers. Its design is crucial because it operates at a higher frequency and consumes higher power consumption. A N/N + 1 counter consist of flip-flops (FF) and extra logic, which determines the terminal count. The high speed FF based N/N +1 counter designs not only limits the frequency and current-drive capabilities, but also increases the total power consumption. Alternatively, FF based N/N +1designs adopt dynamic logic FFs such as true single-phase clock (TSPC).The designs can be further enhanced by using extended true-single-phase-clock (E-TSPC) FFs for high speed and low power applications.

II. 2/3 DUAL MODULUS COUNTER

A dual modulus counter is an electronic circuit used in high frequency designs to overcome the problem of generating narrowly-spaced frequencies that are however too high to be passed directly through the feedback loop of the system. The modulus of a counter is its frequency divisor. A 2/3 dual-modulus counter has two separate frequency divisors, usually 2 and 3.

2.1 TRUE SINGLE PHASE CLOCK

True-single-phase-clock dividers are well known for their low power consumption but their application is limited to relatively low Frequencies. True Single Phase Clock (TSPC) Flip Flop uses three transistors in each stage.

TSPC dynamic CMOS circuit is operated with one clock signal to avoid clock skew problems. TSPC logic circuits exhibit higher switching power.
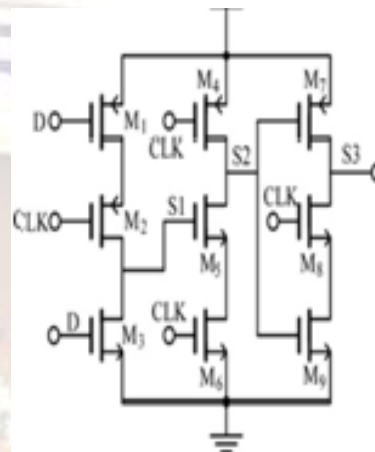

Figure.1 TSPC flip-flop

2.2 EXTENDED-TRUE SINGLE PHASE CLOCK

In each stage, Extended-True Single Phase Clock Flip Flop uses only two transistors. E-TSPC Flip Flop uses less switching power but significantly more short circuit power. This short circuit power exists every fourth clock cycle when Extended-True Single Phase Clock Flip Flop (E-TSPC) is operated as divide by2 circuit. E-TSPC has the merit of higher operating frequency when compared to TSPC.
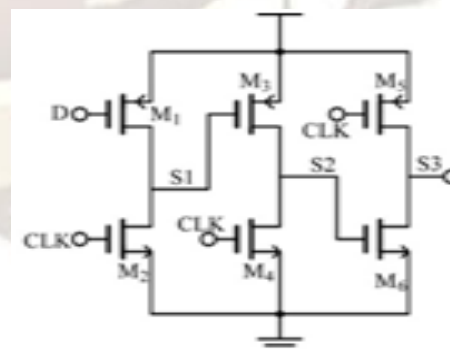

Figure.2 E-TSPC flip-flop

2.3 CONVENTIONAL 2/3 COUNTER DESIGNS

Here we discuss the different designs of 2/3 dual modulus counters based on different types of DFFs.
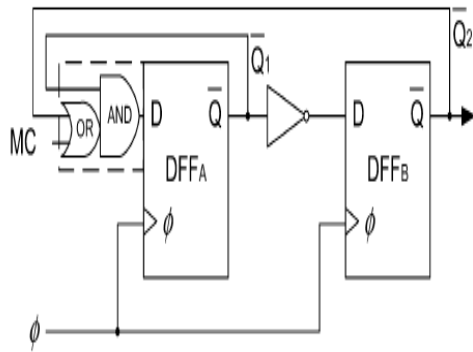
In this design,TSPC Flipflops are used as shown in Fig.3

Figure.3 TSPC 2/3 Counter design

The two operation modes are switched by the external control signal "MC." When "MC" is high, the feedback signal from DFFB is blocked and the counter operates in the same way as a divide-by-2 divider. When "MC" is low, the counter operates in the divide-by-3 mode. An advantage of this implementation is that the feedback logic gates, enclosed by the dash-lined box in Fig 3, can be absorbed by the first stage of DFFA and the logic depth is reduced.

In the divide-by-2 mode where DFFB is shielded from the signal path, the speed optimization can be focused on DFFA and it becomes a divider optimization Problem. The size of DFFB should be minimized from a divide-by-2 perspective to reduce loading to the output of DFFA. On the other hand, the divide-by-3 operation involves both DFFA and DFFB and has more logical states.
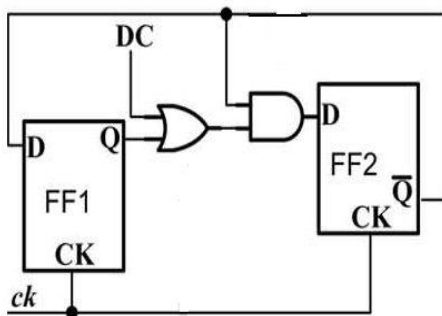

Figure.4 E-TSPC 2/3 Counter design-OR logic

A state-of-the-art divide-by-2/3 counter design is given in Fig.4 [7]. It contains two TSPC-based FFs and two logic gates i.e., an OR gate and an AND gate. When the divide control signal DC is "0", the OR gate (merged into output of FF1 design) is disabled. When DC is "1", the output of FF1 will be disabled and FF2 alone performs the divide-by-2 function. Since the input to FF1 is not disabled, FF1

toggles as usual and causes redundant power consumption in the divide by-2 mode operation. To overcome this problem, another 2/3 counter design presented in Fig.5
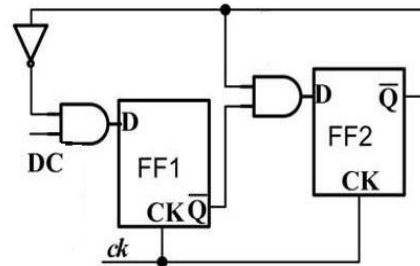

Figure.5 E-TSPC 2/3 Counter design-AND logic.

By pushing the divide control logic from the output of FF1 to its input, the output of the first stage in FF1 is frozen when DC=0. This refrains the following stage from any switching activities for the purpose of power saving. In spite of the circuit simplicity, the inverter between FF1 and FF2, which is essential to the logic of divide-by-3, causes extra delay.

Merging control logic with FF designs also introduces parallel connected transistors important to larger parasitic capacitance in adverse to both speed and power consumption. In view of these issues, our approach is keeping the circuit simplicity, so that the delay and the power consumption problems can be improved at a time.

2.4 LOW POWER 2/3 COUNTER DESIGN
To reduce the transistor count and also to reduce the power consumption, low Power 2/3 counter design is proposed. The logic structure of the low power 2/3 counter design is shown in Fig.6.
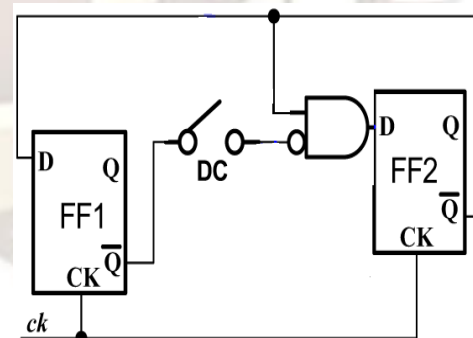

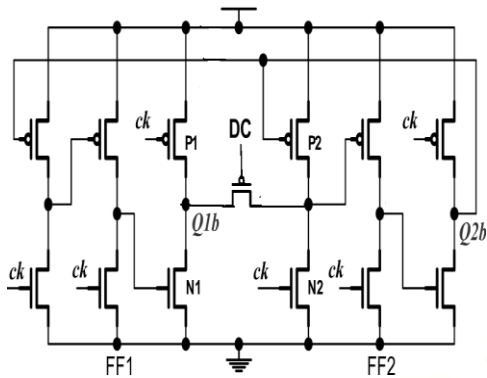Figure.6 Low power E-TSPC 2/3 Counter design

Figure.7 Schematic of E-TSPC Low Power 2/3 Counter

Figure.8 Proposed Multi-Modulus counter design

The two FFs and the AND gate are common in previous designs. The OR gate for the divide control is replaced with a switch. Note that there is a reversal bubble at one of the AND gate's input. The output of FF1 is thus inversed before being given to FF2. When the switch is open, the input from FF1 is disconnected and FF2 alone operates in divide by 2 modes. When the switch is close, FF1 and FF2 are linked to form a counter with three distinct states.

The PMOS transistor controlled by the divide control signal serves as the switch. The AND gate plus its input inverter are achieved by way of wired-AND logic using no extra transistors. . First of all, unlike any previous designs, the ETSPC FF design remains intact without any logic embedding. Both speed and power behaviors are not affected, which indicates a performance edge over the logic embedded FF design.

Secondly, the inverter to complement the one of the two E-TSPC FF outputs for divide by-3 operations is removed in this design. The circuit simplification, suggests the improvements in both speed and power performances.

III.   PROPOSED   MULTI-MODULUS COUNTER DESIGN

The proposed multi-modulus counter uses the low power 2/3 counter for its design. A 2/3 dual modulus counter can be operated in 2 and 3 mode. The multi-modulus counter is also similar to the N/N+1 based dual modulus counter but it can perform additional division operations such as 4/6,8/12,16/24,32/48 according to the mode selection input and divide control.

The proposed multi-modulus counter consists of low power 2/3 dual modulus counter and D-flip flops. In this proposed design, mode selection logic is used to select the flip flop which is used to perform particular counting operation.
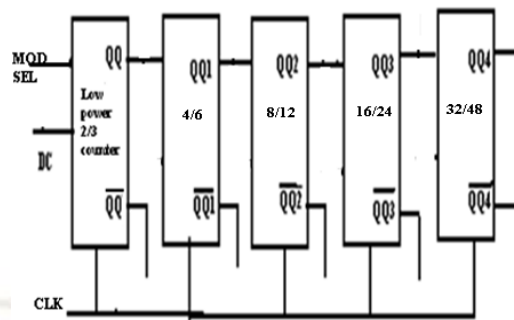
The mode select input and Divide Control (DC) signal are given to low power 2/3 counter. So that according to the Mode selection input, particular flip-flop performs the counting operation and the corresponding flip flop output is taken as an output in the divider output. Then the mode of operation among the two values can be chosen according to the DC value.

CASE 1: If mode select input is 000 and dc=1, then the output of QQ is 2.Then we get the divider output i.e., div out as QQ. If mode select input is 000 and dc=0, then the output of QQ is 3.Then we get the divider output i.e., div out as QQ.

CASE 2: If mode select input is 001 and dc=1, then the output of QQ1 as 4.Then we get the divider output i.e., div out as QQ1. If mode select input is 001 and dc=0, then the output of QQ1 is 6.Then we get the divider output i.e., div out as QQ1.

CASE 3: If mode select input is 010 and dc=1, then the output of QQ2 is 8.Then we get the divider output i.e., div out as QQ2. If mode select input is 010 and dc=0, then the output of QQ2 is 12.Then we get the divider output i.e., div out as QQ2.

CASE 4: If mode select input is 011 and dc=1, then the output of QQ3 is 16.Then we get the divider output i.e., div out as QQ3. If mode select input is 011 and dc=0, then the output of QQ3 is 24.Then we get the divider output i.e, div out as QQ3.

CASE 5: If mode select input is 100 and dc=1, then the output of QQ4 is 32.Then we get the divider output i.e., div out QQ4 as a result. If mode select input is 100 and dc=0, then the output of QQ4 is 48.Then we get the divider output i.e., div out as QQ4.

IV. SIMULATION RESULTS

All modern digital designs start with a designer writing a hardware description of the IC (using HDL or Hardware Description Language).A variety of CAD tools are available to synthesize a

circuit based on the HDL. Here a VHDL program is used.The Modelsim simulator is used to obtain the simulated output for the proposed multi- modulus counter. The simulated waveforms are obtained by assigning the mode select inputs at various DC levels of extraction and the corresponding outputs are obtained according to the input values. The simulated waveforms of the proposed work are shown.

4.1Simulation Result For proposed Design Using Modelsim software

Simulated Waveform of the Proposed counter when DC=1, it performs 2, 4, 8, 16 and 32 counting operations as shown in Fig.9
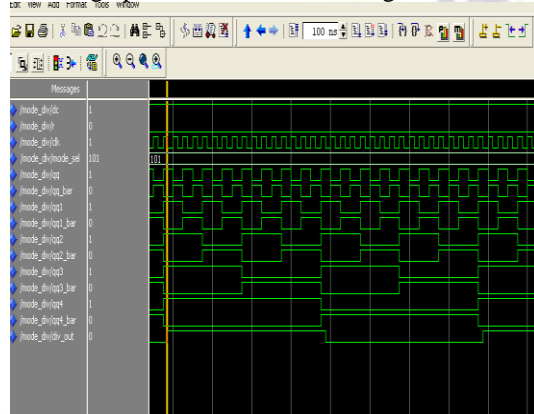

Figure.9 Simulation result for proposed multi-modulus counter (DC=0)

Simulated Waveform of the Proposed counter when DC=0, it performs 3, 6, 12, 24 and 48 counting operation as shown in Fig.10
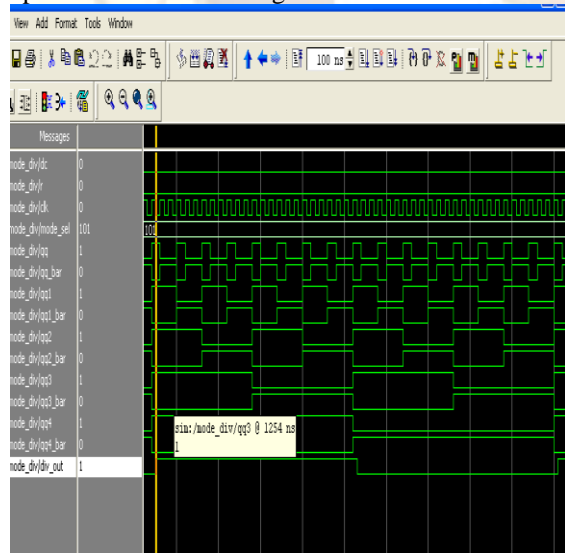

Figure.10 Simulation result for proposed multi - modulus counter (DC=1)

4.2 Power Results

Power report for low power 2/3 counter design shows that the total estimated power consumption is 61mW as shown in Fig.11
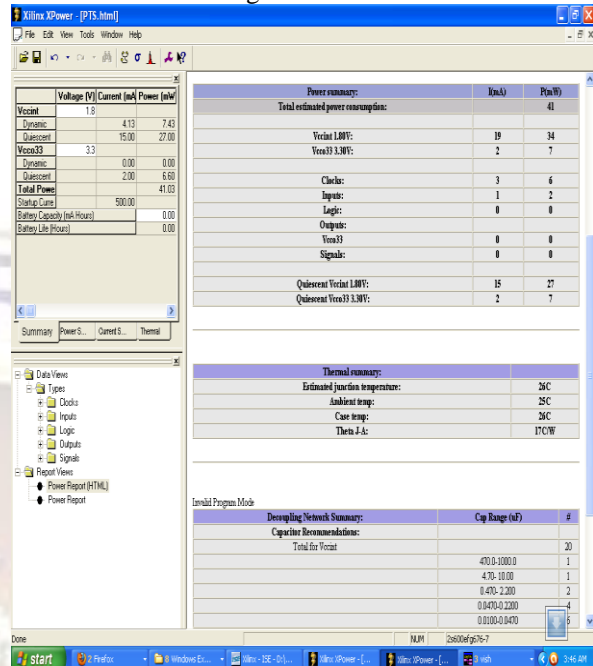

Figure.11 power report for low power 2/3 counter design

Power report for proposed multi-modulus counter design shows that the total estimated power consumption is 56mW as shown in Fig.12
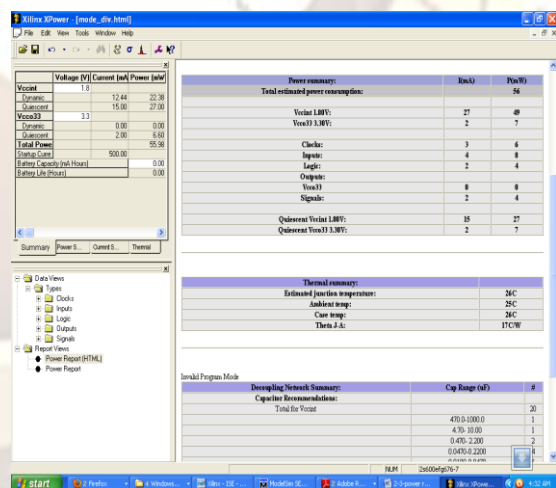

Figure.12 power report for proposed multi- modulus counter design

V. CONCLUSION

Besides the fixed-modulus counters, multi-modulus counters can also be synthesized in a similar way by using more than one E-TSPC DFFs and 2/3 counter. The proposed multi-modulus counter design which is suitable for high speed applications is presented. The proposed design successfully implements the mode selection logic

and performs multiples of counter operation. The usage of E-TSPC low power 2/3 counter leads to a shorter critical path and made it as efficient design.

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