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Cadence Design of Leakage Power Reduction Circuit in CMOS VLSI Design

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ABSTRACT

In this paper, a low-power novel design technique proposed in [1] to minimize the standby leakage power, in nanoscale CMOS very large scale integration (VLSI) systems by generating the reverse body-bias voltage, is applied to op-amp circuit and the stack circuit. The optimal reverse body-bias voltage is generated from the proposed leakage circuit, and calculated the subthreshold current (I_{SUB}) and the band-to-band tunneling current (I_{BTBT}). The proposed circuit will be simulated in Cadence 180 nanometer CMOS technology,

Keywords – Leakage currents, sub-threshold Leakage, Band to Band Tunneling currents

1. INTRODUCTION

As the technology is rapidly growing on day by day according to the moors law transistor density have been increasing and due to this huge density the power consumption has been reached to high peaks as we are unable to change the battery parameters so we are introducing some power reduction circuits in the design power consumption is of two types static power consumption mainly due to power sources and the dynamic power consumption which is mainly due to the switching activities and whenever the transistor is in the OFF condition the V_{dd} will be directly shorted to the ground which is called as sub-threshold leakage current .Leakage power is increasingly significant in CMOS circuits as the technology scales low, due to the exponential increase of sub-threshold and gate leakage currents with technology scaling.

Many leakage reduction techniques have been proposed. Forced stacking reduces leakage power by inserting an extra serially connected transistor in the gate pull down or pull up path and turning it off in standby mode. Input vector control uses the state dependence of leakage to apply a low-leakage input vector to the circuit in standby mode to save leakage power. The power cut off technique also called supply gating ,reduces leakage by disconnecting the global supply voltage in standby.

One common problem of all techniques is that they can only reduce the circuit leakage power in standby mode. Leakage is important in both standby and active operation modes. The leakage in active mode is significantly larger due to the higher die temperature in active mode. So, efficient leakage power reduction must target both standby and active leakage power.

The dual V_{th} technique uses high-threshold voltage devices on noncritical paths to reduce leakage while using low-threshold devices on critical paths to maintain circuit speed. It reduces both active and standby leakage. However, this technique does not reduce the leakage on critical paths. Thus, it does not help much for practical circuits, whose paths are usually well balanced. Supply voltage scaling developed for switching power reduction, also reduces both active and standby leakage power. But level conversion is needed at the interface whenever an output from a low V_{dd} unit drives a high V_{dd} unit input.

Bhatia , proposed dynamic leakage reduction using supply gating ,They use the Shannon expansion to identify the idle circuit parts and dynamically gate the supply to those parts to save active leakage power, to overcome all these problems

In this paper, we propose a leakage reduction of power technique using power leakage reduction circuit

2.LEAKAGE CURRENT COMPONENTS IN REVERSE BODY BIAS CONDITION

There are various types of leakages in the cmos circuit such as the drain to gate leakage [2], and leakages due to the gate oxide layer leakage due to the channel length and also leakage due to band to band tunnelling ,The leakage currents is the sum of the subthereshold currents and the band to band tunnelling currents

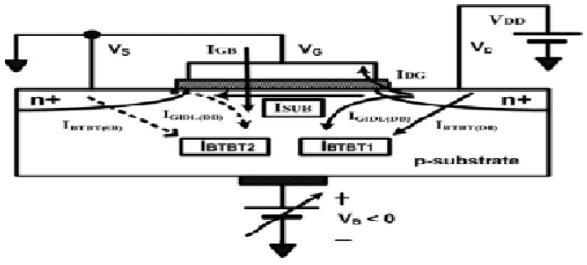

Fig 1.Leakage current components

2.1 SUB-THRESHOLD LEAKAGE:

This is the leakage [1] occurs is the current that flows between the source and drain of a MOSFET when the transistor is in subthreshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. The subthreshold region is often referred to as the weak inversion region. And this process of grounding the v_{dd} directly when the transistor is in the off state is called as sub-threshold leakage current

2.2. BTBT leakage:

Band to Band tunnelling current [1] flows through the drain-to-substrate junctions due to the twisting of Band gaps. With higher supply voltage, thinner oxide thickness, lightly doped drain, reverse body bias (RBB) technique[3], and high mobility channel materials having smaller band gaps.

2.3. GIDL :

The GIDL current, which is also called the surface BTBT current, is the drain-to-substrate leakage due to the BTBT current in very high field depletion region in the gate-drain overlap region. When the drain of an n-MOSFET is biased at the supply voltage (VDD) and the gate is biased at either zero or negative voltage, a depletion region is formed under the gate and drain overlap region

2.4. Gate to body leakage (I_{gb}):

I_{GB} is the gate-to-bulk oxide tunneling leakage current[1], and I_{DG} is the drain-to-gate oxide tunneling leakage current. As the gate oxide thickness scales below 2 nm, the direct tunneling (DT) gate leakage exponentially increases due to quantum mechanical tunneling. The direct tunnelling gate leakage current can not only increase the power dissipation but also limit the proper logic gate operation. Recently, a high-k dielectric base on Hafnium and dual metal gate has been introduced to increase the transistor performance. The high-k dielectric material reduces the gate leakage as the gate dielectric thickness can actually be increased while the gate capacitance is increased

3.BLOCK DIAGRAM:

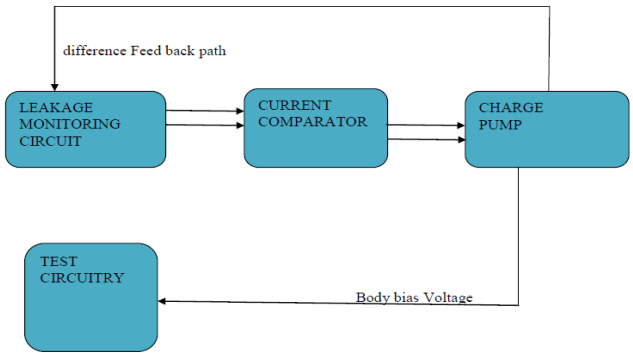

Fig.2. Block diagram of the proposed V_{Body} control system.

This block diagram consists the proposed V_{Body} control system that minimizes the overall power dissipation induced in the test circuit and this hardware allows the independent and the adaptive maintenance of the body bias voltages and according to the leakage in the test circuit the monitoring circuit will produce the body bias voltage when the operating conditions change. The proposed scheme consists of the leakage monitoring Circuit, the current comparator, and the charge pump. Leakage monitoring circuit monitors the subthreshold leakage current and then forwards the leakage current to the current comparator in which the current comparator detects the level and level is forwarded to the charge pump and there is a feed back control system between the monitoring circuit and the charge pump and this whole arrangement is fixed to the test circuitry and the body bias voltage in the test circuitry is balanced by the proposed circuit

3.1 CADENCE SCHEMATIC:

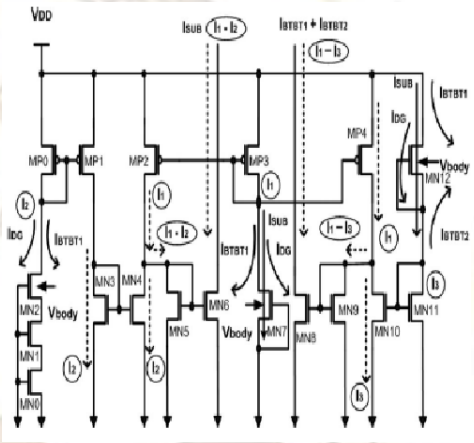

FIG3: v_{body} leakage circuit

The leakage control system consists of a comparator and charge pump, comparator compares the tunneling and sub-threshold leakage current and sent to the charge pump for the boosting purpose

3.2: Leakage control system

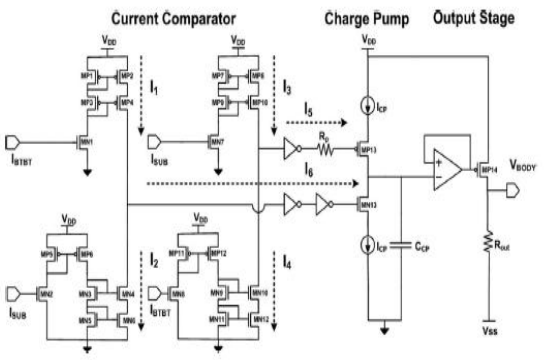

FIG4: Leakage control system

In analog and mixed-signal systems, an operational amplifier (op amp) is commonly used to amplify small signals, to add or subtract voltages, and in active filtering. It must have high gain, low current draw (high input resistance), and should function over a variety of frequencies, and the op amp transistor level has been drawn below

3.3: op-amp design:

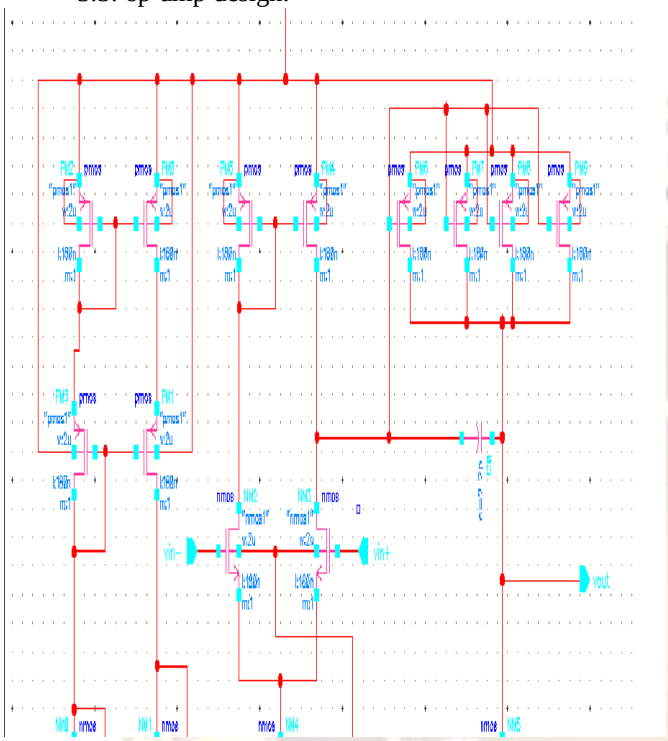

FIG5: op-amp design

Stacking is a process of adding an extra transistors in between the pmos and nmos so as to reduce the sub threshold leakage current, and the test circuitry is the inverter with the nmos stack transistors.

3.4 Test circuit (CMOS stack):

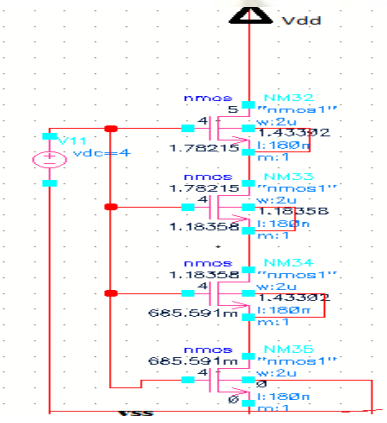

FIG 6**:** Test circuitry

4 : RESULTS WITH WAVE FORMS:

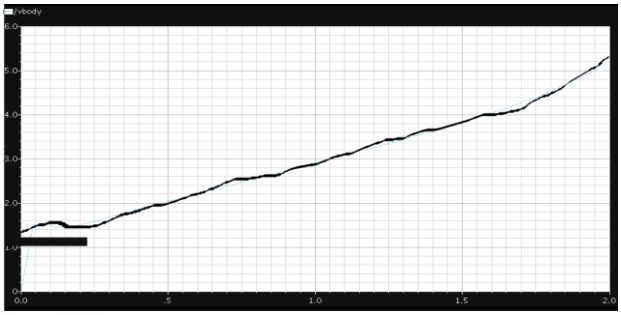

FIG 7: Wave form of the leakage control system

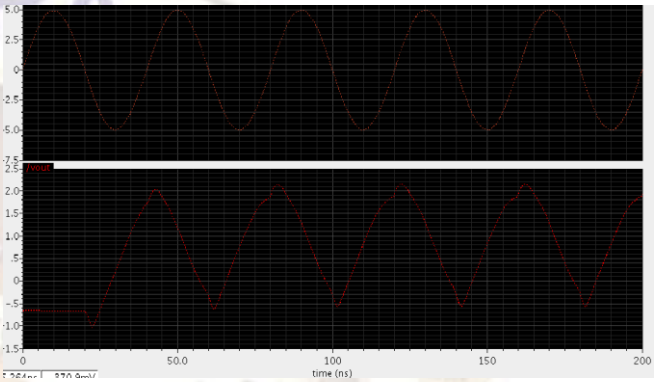

FIG8:waveform of the opamp

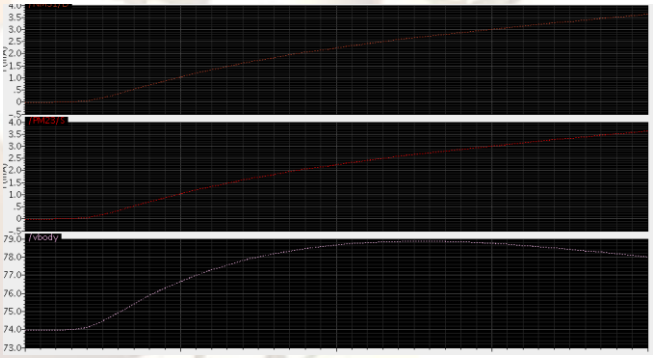

FIG 9:waveforms of the test circuitry of stack transistors

In the wave form of the test circuitry the leakage power has been reduced. By using CMOS stack circuitry most of the leakage currents have been reduced which is due to the increase in the threshold voltage and in the negative differential op-amp the result is the exact difference of the input signals and the outputs can be limited from the given inputs these all individual circuits are designed in the cadence 180 nm technology and if we add the whole process to the technology library and we can further use this design for reusability further experiments

5.CONCLUSION:

The proposed circuit in [1] was designed in cadence environment with 180nm technology and

the body bias voltage was generated . This circuit can be further involved in the huge analog VLSI circuits for the low power consumption. Due to the stack transistors the leakage power also reduced and the current components of the test circuitry has been found. To reduce the leakage power, this paper has presented a technique that generates the V_{Body}. By observing the BTBT leakage current (I_{BTBT}) and the subthreshold leakage current (I_{SUB}), the body-bias voltage is automatically generated and continuously adjusted by the control loop. By tuning the body bias voltage using the leakage-monitoring circuit, the circuit can be biased at the optimal point where the subthreshold leakage current and the BTBT leakage current are balanced to accomplish the minimum leakage power, by using the stack transistor by comparing op amp and the stack circuitry mostly subthreshold leakage power has been reduced from the stack circuitry only

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