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Hardware Implementation Of Hyperbolic Tan Using Cordic On FPGA

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ABSTRACT

There are many hardware efficient algorithms for digital signal processing. Among these algorithms there is a shift and add algorithm known as CORDIC algorithm used for implementing various functions including trigonometric,hyperbolic, logarithmic. Hyperbolic tan is a function used in many decoding algorithms like LDPC (low density parity check) codes. In this paper we have implemented hyperbolic tan function using CORDIC rotation method algorithm on FPGA .Coding of the algorithm is done in vhdl.

Keywords–**CORDIC, FPGA, hyperbolic tan, LDPC.**

1. INTRODUCTION

Many digital signal processing algorithms are implemented on microprocessors and microcontrollers. Though these processors are low cost and provide extreme flexibility ,they are not fast enough for truly demanding Digital signal processing tasks. With the advent of reconfigurable devices like CPLDs and FPGAs which work at higher speed , DSP algorithms could be easily implemented .There are many DSP algorithms out of which there is one hardware efficient algorithm based on iterative solution to calculate trigonometric and transcendental functions. This iterative algorithm uses only shift and add operation to calculate the values of the function. This algorithm is called CORDIC algorithm.

CORDIC stands for COordianteRotation Digital Computer . This algorithm was first proposed by Jack Volder in the year 1959 [1].In his thesis he proposed a method to calculate trigonometric values. Extensions to the CORDIC theory based on work by John Walther[2] and others provide solutions to a broader class of functions.

Hyperbolic functions are analogous to trigonometric circular functions.The basic hyperbolic functions are sinh cosh and tanh

Tanh function is defined as

$$\tanh(x) = \frac{\sinh(x)}{\cosh(x)}$$

Tanh is function widely used in many applications like digital neural network, image processing, filters, decoding algorithms etc.

This paper aims to implement hyperbolic tan on Field programmable gate array(FPGA).In the first part a brief description of the theory behind the algorithm is presented. Then the extended theory called unified CORDIC algorithms is explained. In the second part implementation of algorithm on FPGA is shown. The last part of the paper deals with the experimental results and future work.

2. CORDIC ALGORITHM

CORDIC is a special purpose digital computer for real time computations. This algorithm was specially developed for real time digital computers where the majority of computations involved trigonometric relationships. It contains special arithmetic unit consisting of shift registers,adder–subtractors and special interconnects.

CORDIC algorithm was first proposed by Jack Volder in 1959[1],[3]. This algorithm is derived from general rotation transform

$$x' = x * \cos(\emptyset) - y * \sin(\emptyset) \quad (1)$$
$$y' = y * \cos(\emptyset) + x * \sin(\emptyset) \quad (2)$$

which rotates a vector in Cartesian form. The above two equations can be modified as

$$x' = \cos(\emptyset)\,[x - y * \tan(\emptyset)] \quad (3)$$
$$y' = \cos(\emptyset)\,[y + x * \tan(\emptyset)] \quad (4)$$

If the rotation is restricted to $\tan(\varphi) = +/- 2^{(-i)}$,the multiplication in the above equation will be replaced by simple shift operation. The rotation can now be expressed as

$$X_{i+1} = K_i\left[X_i - Yi * d_i * 2^{(-i)}\right] \quad (5)$$
$$Y_{i+1} = K_i\left[Y_i + X_i * d_i * 2^{(-i)}\right] \quad (6)$$

Where i is the iteration count and

$$K_i = \cos\left(\tan^{-1}\left(2^{-i}\right)\right) \quad (7)$$

and $d_i = +/- 1$.

Removing the scaling factor the iteration equation is simple shift and add equation. The value of K approaches to 0.607 as the iteration count approaches infinity. The direction in which the vector should be rotated is given by the equation

$$Z_{i+1} = \left[Z_i - di * \tan^{-1}\left(2^{-i}\right)\right] \quad (8)$$

where

$$d_i = -1\ if\ Z_i < 0, +1\ otherwise.$$

The limitation of the equations proposed by Volder was only sin,cos and tan function values could be calculated .Volder did not propose method to

calculate hyperbolic and linear functions like division multiplication logarithmic values, sinh cosh tanh etc.

J.S.Walther [2] modified the equation given by Volder. His modification to the original CORDIC equations helped calculating hyperbolic and linear functions. He proposed generalized equation which can be used to calculate functions belonging to all three coordinate systems. He considered coordinate system parameterized by 'm'. The modified equations are as given

$$X_{i+1} = [X_i - m * Yi * d_i * 2^{(-i)}] \quad (9)$$

$$Y_{i+1} = [Y_i + X_i * d_i * 2^{(-i)}] \quad (10)$$

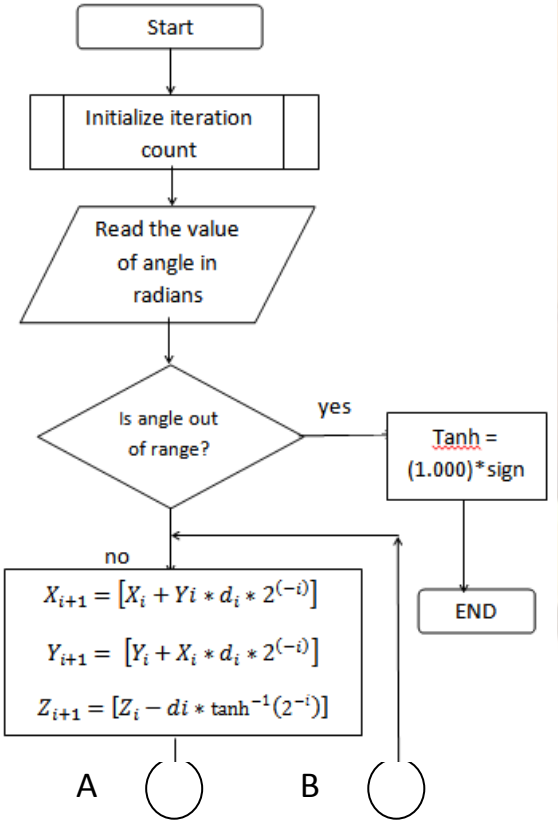
$$Z_{i+1} = [Z_i - di * Ei] \quad (11)$$

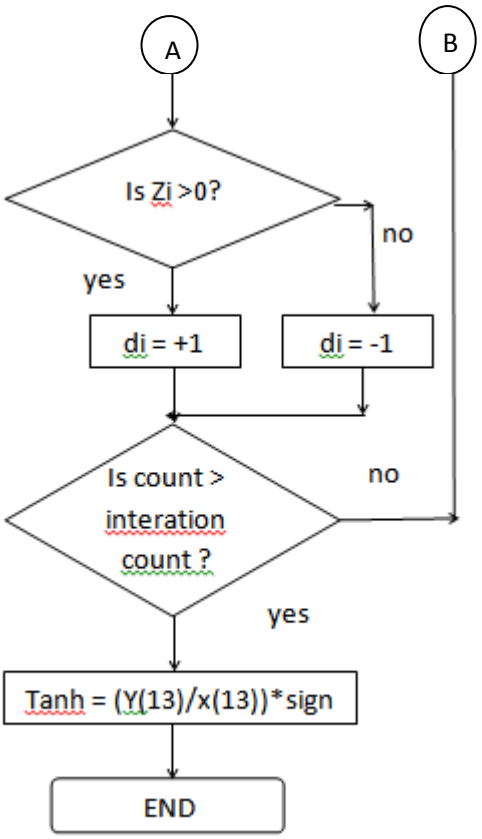
Where

$$d_i = -1 \; if \; Z_i < 0, +1 \; otherwise$$

Coordinate system	Value of m	Value of Ei
Circular	1	$\tan^{-1}(2^{-i})$
Hyperbolic	-1	$\tanh^{-1}(2^{-i})$
Linear	0	2^{-i}

3. FLOW CHART





Graph 2

4.DESIGN

Hyperbolic tan graph was simulated using MATLAB.[6] The graph is as shown

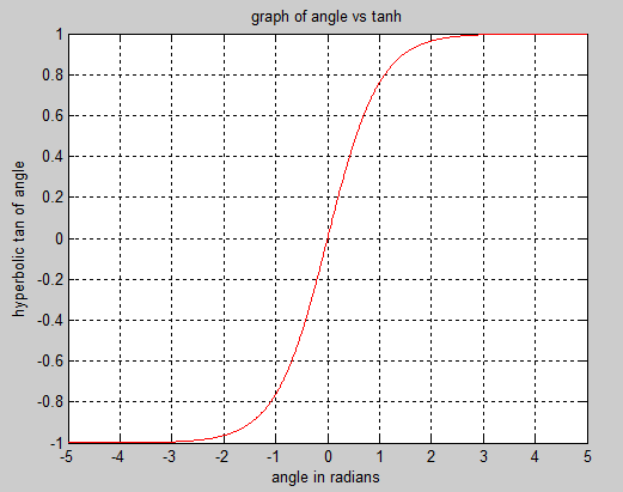


Figure 1

From the graph it is clear that value of hyperbolic tan remain constant (= 1) when the angle crosses the value approximately equal to 3.
From the graph it is also clear that

$$\tanh(-\emptyset) = -\tanh(\emptyset)$$

Hence the vhdl code first calculates the hyperbolic tan of the absolute value of the input angle. At the end of the code the sign of the entered angle is taken into consideration. Before calculating the tanh value of the entered angle system checks whether the entered angle isgreater than 3.5. If it is, then directly the output is generated (+/- 1 depending upon the sign of the entered angle).

As the CORDIC algorithm is an iterative shift and add algorithm to calculate the value of the function, iteration count plays an important role is the accuracy of the calculated value . [4] Hyperbolic functions do not converge with the sequence of angles $\tanh^{-1}(2^{-i})$ since

$$\sum_{j=i+1}^{\infty} \tanh^{-1}(2^{-j}) < \tanh^{-1}(2^{-i}) \quad (12)$$

Values of iteration count which leads to convergence of hyperbolic functions are 4,13,40,….k,(3k+1).

MATLAB code of CORDIC algorithm was executed for different values of iterations and the graph of error between calculated and observed value vs number of iterations was plotted .The graph is as below

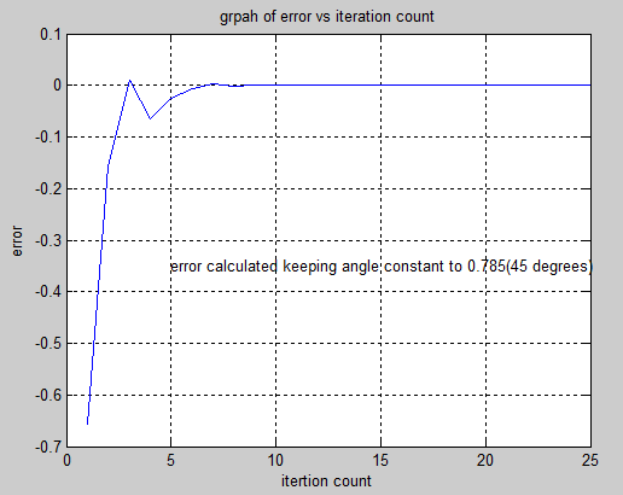


Figure 2

From the graph it is clear that when the iteration value crosses a count of 10 error is almost zero. Hence in the vhdl code iteration count is taken as 13

The data is represented by 16 bit fixed point data format.The format is as shown

SIGN	INTEGER(5)	FRACTION(10)

Sign bit is MSB . It indicates whether data is positive or negative(0 means positive and 1 means negative). 10 bit precision is used.This increases the accuracy of the system.

The block diagram of the circuit is as show.

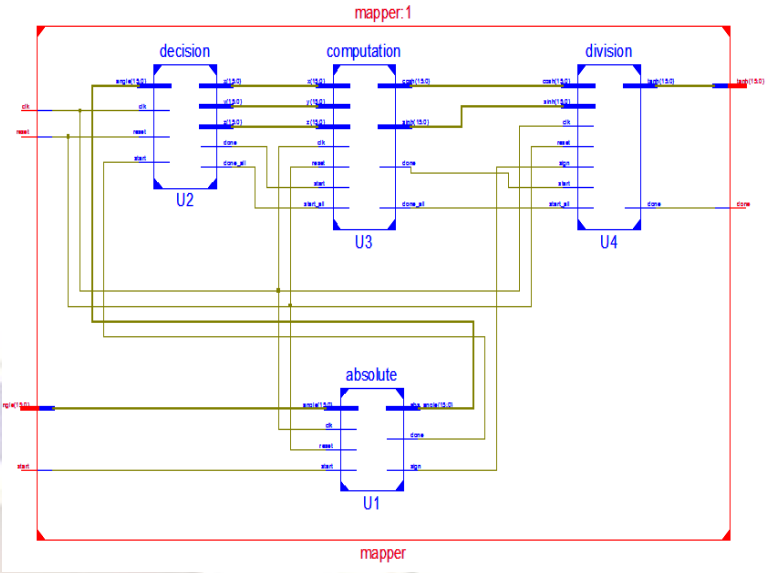


Figure 3

The absolute block separates the sign and the magnitude part of the angle entered. The magnitude part of the values is given to the decision block.

The decision block checks the range of the angle . If the value is out of range(greater than 3.5) then decision block generates a done_all control signal. If not then decision block initializes the valuesof X, Y and Z and generates a control signal done. These values are given to the computation block.

The computation block implements the hyperbolic CORDIC equation given in equation(9),(10) and (11).this block at the end of 13 iterations generates the values of hyperbolic sin and hyperbolic cos.These values are given to division block.To increase the speed barrel shifters are used.[5]

The division process used in this code is also implemented using CORDIC algorithm. It computes the value of tanh (tanh = sinh/cosh).After calculating the value of hyperbolic tan sign value is taken into consideration and final result is generated.

5. RESULTS

MATLAB code for hyperbolic tan function was written and was executed for various values of angle and was compared with the standard value. The graph for the same was plotted

From the graph it is clear that error percentage for angles less than 0.1 is approximately is 4.5% and for angles greater than 0.1 error is approximately 0.

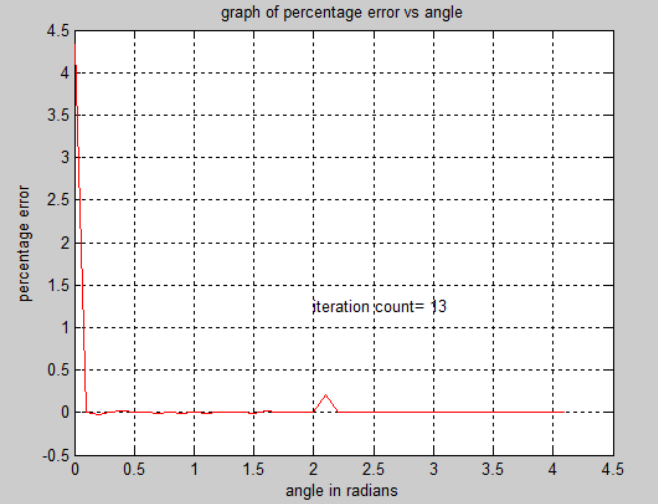


Figure 4

Xilinx ISE design suite 13.2 software was used to synthesize the VHDL code. The board selected was Virtex5 FPGA board[7]. The target device is xc5vlx110t-1ff1136. The synthesis report is as shown.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	211	69120	0%
Number of Slice LUTs	1153	69120	1%
Number of fully used LUT-FF pairs	149	1215	12%
Number of bonded IOBs	36	640	5%
Number of BUFG/BUFGCTRLs	1	32	3%

Figure 5

The maximum clock frequency at which the system can work is 130MHz.Total power consumption of the system is 1.04watts.

6. CONCLUSION

The advantage of the design proposed in this paper is that no DSP or multiplication blocks are used. As 10 bit precision is used, the accuracy of the design is high. The only disadvantage is that thenumber of iterations required are slightly more.This block can be used in few decoding algorithms in communication systems. The design will be used in LDPC decoder sum product algorithm.

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