

Designing Of Controller for Anti-Lock Braking System Using FPGA

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ABSTRACT

The antilock braking systems are designed to increase wheel traction by preventing the wheels from locking up during braking, while also maintaining adequate vehicle steerability; however, the performance is often degraded under harsh road conditions. Experimental results show that the proposed antilock brake control algorithm provides very good slip regulation in a braking event on low friction-coefficient surfaces when compared with that of a braking event without the proposed antilock-braking control. The proposed control scheme has been realized using XC3S50.

Keywords - Analog to digital converter (ADC), Antilock braking system (ABS), Brake system, Speed Sensors.

I. INTRODUCTION

In auto mobile industry, applications of the controlled technology have been widely used for controlling the speed of wheels of the car. Traditional methods like brakes and air pressure having their own disadvantage on dry and slippery surfaces. Among these traditional method brake are generally used in the wheels of the car but they are not completely safe because it is totally subjected to the surface of road. In recent years, the various developments in electronic technology have become key components in implementing high performance of auto mobile industry. A lots of research work has been carried out to improve the control technology of cars and auto mobiles area. With the help of available electronic technology it is possible to drive the devices with more sensitivity. These controls are more accurate and precise as compared to traditional method used in earlier stages of development of auto mobile industry. But the general perception is that the potential of electronic technology is not fully utilized in the area of auto mobile industry. Now researchers are trying to combine this two high potential area to implement high efficient hybrid model for controlling the speed of wheels of the car. Proliferation of braking system based on electronic circuit numbered days of traditional braking system. It is well accepted that the use of these advanced integrated circuits has significantly improve system performance.

The control of ground vehicle motion is very important for driving safety. A motor vehicle has large amount of kinetic energy as it is driven; when the brakes are applied, the kinetic energy of the vehicle is dissipated as heat energy in the brake disks, and between the wheel and the pavement.

The objective of an antilock braking system (ABS) is to maximize wheel traction by preventing the wheels from locking during braking, while maintaining adequate vehicle stability and steerability and reducing the vehicle stopping distance.

The ABS is a challenging problem because the vehicle braking dynamics are highly nonlinear with uncertain time-varying parameters. These parameter variations are due to factors such as changes in the braking coefficient of friction, changes in the road gradient, and variations in the friction characteristics of the wheel/road contact [1].

Digital Signal Processors (DSPs) and Microcontrollers are used for digital control applications. But DSPs and Microcontrollers can no longer keep pace with the new generation of applications that require not just higher performance also more flexible without increasing cost and resources. Further microprocessors, Microcontrollers and DSPs are sequential machines that mean tasks are executed sequentially which takes longer processing time to accomplish the same task. The efficient control of the motor drive systems involves fast computational units. Signal processors and microprocessors are frequently used in such applications. Using universal microprocessors or signal processors enables obtaining high computational efficiency but significantly increases the costs of a drive application. The 16 and 32 bit processors designed for electric drive applications have relatively low computational power. Furthermore, the sets of interfaces offered by such processors in some application have to be replaced by specialized ones. Alternatively the ASIC chips can be applied. Such an approach enables developing custom-built digital interface as well as digital data processing blocks and sometimes even integration of ADC converters into one integrated circuit. Developing an ASIC chip is however expensive and laborious, therefore on the design stage of algorithm and interface development, FPGA based solution can be used.

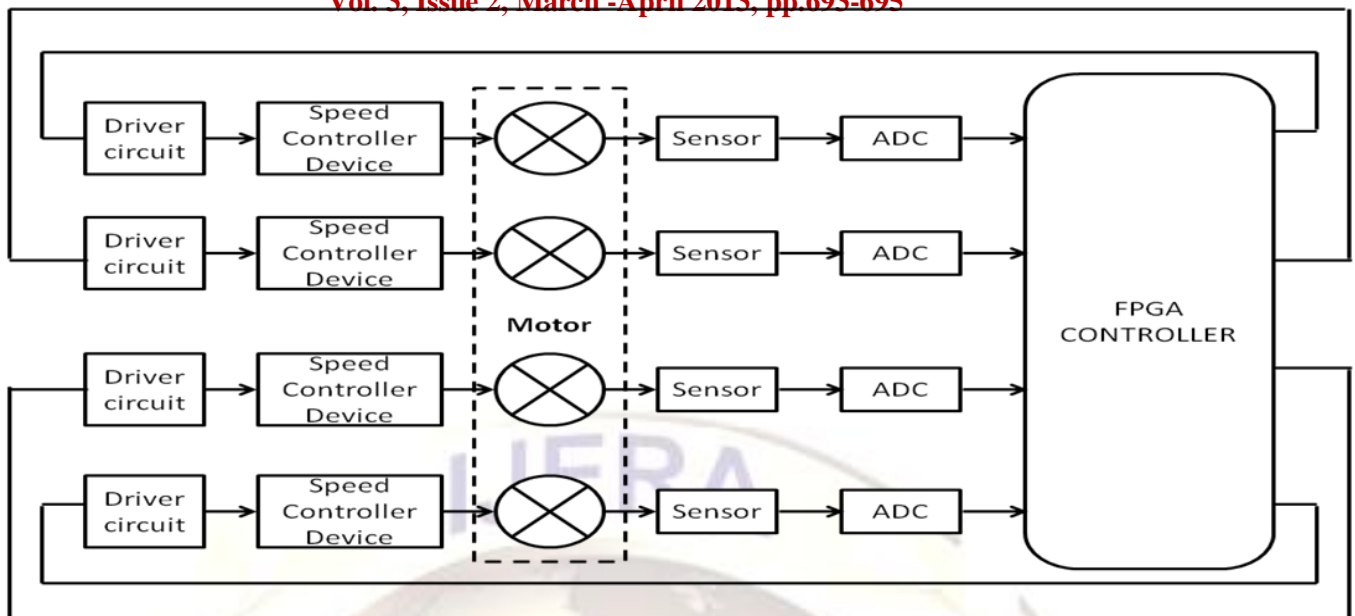


Fig. 1 System Block Diagram

II. FPGA BASED CONTROL SCHEME

Set-up will consist of FPGA Board, speed sensors, ADC, Driver circuit, speed controlling device. Integration of these modules will result in controlling technology with superior performance over other traditional braking methods.

2.1 Sensors

The anti-lock braking system needs some way of knowing when a wheel is about to lock up. The speed sensors, which are located at each wheel, or in some cases in the differential, provide this information.

2.2 FPGA Controller

FPGA Controller accepts input of the speed sensors through ADC. Depend on the speed of 4 wheels; the controller unit in FPGA calculates the required increment or decrement in the speed. Depend on this calculation FPGA controller provide the required controlling signal to the driver circuit for changing the amount of pressure of hydraulic pump. The changes in the output of speed sensor directly decide the speed of particular wheel. The FPGA controller is design by using the counter and latch. The FPGA controller is design by using the counter and latch. The coding is performing in VHDL. The flowchart is shown in Figure 2.

2.3 Driver Circuitry

I/O ports on FPGA board can source only 10 mill ampere of current on each pin. This current is not enough to fire the SCR directly. Sensitive gate switches those with gate trigger current is less than 200 microamperes can be fired directly but the problem of isolation will still be existing. Typically this problem is resolved using pulse transformers. As the goal of this proposed design is to provide a solution that is compact and fully isolated from mains, technique to drive the SCR/TRIAC by optocoupler seems good and economical in anyway. The triggering pulse is generated at the output pin of

FPGA board is 4.8V, this pulse is provided to the input of optocoupler which convert this small voltage and current into appropriate driving voltage and current and apply it to the gate of the thyristor as a result thyristor gets fired. With the variation in the sensor output delay is inserted in the generation of triggering pulse with respect to sinusoidal voltage which is known as firing angle. Hence when this pulse is provided to the optocoupler it triggers the thyristor. As we are using the bridge circuit we get the output for positive as well as negative half cycle.

2.4 ADC

An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a device that converts the input continuous physical quantity to a digital number that represents the quantity's amplitude. The conversion involves quantization of the input, so it introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have converted a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal [4].

An ADC may also provide an isolated measurement such as an electronic device that converts an input analog voltage or current to a digital number proportional to the magnitude of the voltage or current.

III. EXPERIMENTAL RESULTS

The controller was designed using VHDL, in a manner that facilitates control over the hardware implementation complexity, and is implemented into a Xilinx FPGA. A compact reliable low-complexity reusable digital controller design is achieved, allowing rapid prototyping of the drive via FPGA

controller implementation. This offers a cost effective solution for industrial applications that do not have high dynamic requirements. Experimental results confirmed the efficiency of the controller.

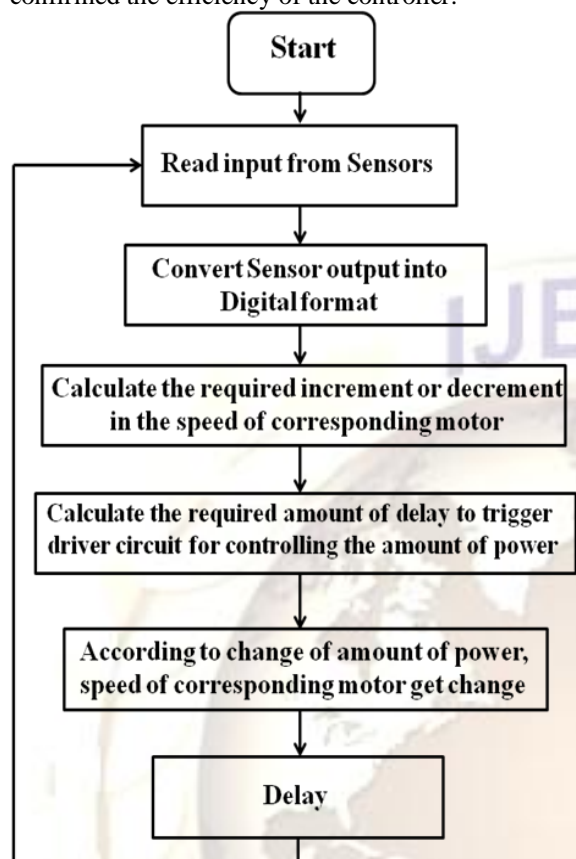


Fig. 2 Flow Chart

Table 1 Parameters of motor driver

Parameters	Value
Current controller sampling frequency	40 KHz
PWM switching frequency	40 KHz
Source voltage	40 V
Phase inductance	7.35 mH
Phase resistance	2 Ω
Encoder resolution	10000 position/revolution

Table 2 Timing summary

Resources	Quantity
Minimum period	37.468ns
Minimum input arrival time before clock	(26.689MHz)
Maximum output required time after clock	13.688ns
Maximum combinational path delay	10.794ns
	8.175ns

Table 3 Device utilization summary

Resources	Quantity
Selected Device	XC3S50
Number of Slices	12788 out of 46592 27%
Number of Slice Flip Flops	6721 out of 93184 7%
Number of 4 input LUTs	21682 out of 93184 23%
Number used as logic	21457
Number used as Shift registers	225
Number of IOs	176
Number of bonded IOBs	173 out of 824 20%
Number of MULT18X18s	64 out of 168 38%

IV. CONCLUSION

In this paper, an optimized FPGA controller is proposed for ABSs. The input variables to the controller are wheel speed and vehicle acceleration. All the parameters of FPGA system are optimized using genetic algorithms and an error-based optimization technique. The objective function is defined to maintain the wheel slip to a desired level so that maximum wheel traction force and maximum vehicle deceleration are obtained. In order to obtain the optimum value in a shorter time and in a much wider region, the error-based optimization approach is used. The method shows a much faster response in comparison with the genetic algorithm alone. The performance of the proposed controller is tested on the vehicle model considering the effect of dynamic load transfer from the rear to the front wheel, with the hydraulic brake system, for different road conditions. Simulation results show very good performance of the controller for different road conditions. It is shown that in the case of the optimal FPGA controller, the slip is kept a small value by tracking the maximum adhesion factor. In addition, the oscillations are much less than that of the fuzzy logic and PI controller, so the vehicle has adequate lateral stability and good steerability.

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