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Study of Three Phase Cascaded H-Bridge Multilevel Inverter For Asymmetrical Configuration

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ABSTRACT

We know that, the inverters are broadly classified as two level inverters and multilevel inverters. This conventional inverters have many limitations at high power and high voltage applications. However, the multilevel inverter becomes popular for high power and high voltage applications due to their increased number of levels at the output. As number of levels increases, the harmonics are reduced and output voltage tend to become more pure i.e., sinusoidal. There are three types of topologies used in multilevel inverter, 1) neutral-point-clamped (NCP), 2) flying capacitors, 3) cascaded H-bridge. Among this, Three phase cascaded H-bridge multilevel inverter is further divided in two configuration, 1) Symmetrical and 2) Asymmetrical.

This paper deals with, study of Asymmetrical configuration for seven level H-bridge multilevel inverter. We prepared the simulation for five level symmetrical, seven level symmetrical and Asymmetrical configurations in MATLAB.

Keywords - Multilevel Inverter, Symmetrical MLI, Asymmetrical MLI.

I. INTRODUCTION

If the output voltage or current of conventional voltage source inverter has levels such as +Vdc, 0 or -Vdc, where Vdc is the dc-link voltage, then it is termed as two-level inverter. To obtain a quality output voltage or a current waveform with a minimum amount of ripple content, they require high switching frequency along with various pulse-width modulation (PWM) strategies. These two level inverters have some limitations in high power and high voltage application. These are mainly due to switching losses and constraints of device ratings.

Where, as the multilevel inverter becomes popular in high voltage and high power application. Multilevel inverter is an effective and practical solution for increasing power demand and reducing harmonics of AC waveform. Function of multilevel inverter is to synthesize a desired voltage wave shape from several levels of DC voltages. As number of levels increases, the number of steps in staircase output waveform becomes more and more and tends to become more pure i.e, sinusoidal waveform.

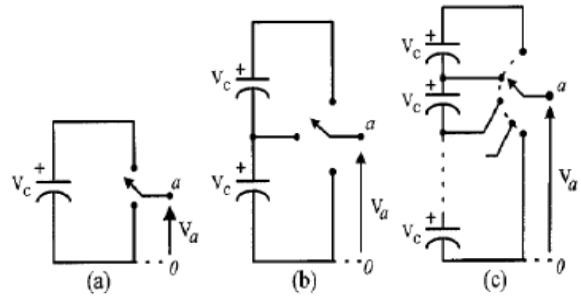


Fig.1 One leg of inverter with (a) two-levels (b) three-levels and (c) n-levels.

Fig. 1 shows a schematic diagram of one phase leg of inverters with different numbers of levels, for which the action of the power semiconductors is represented by an ideal switch with several positions. The multilevel inverter includes an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output, while the power semiconductors must withstand only reduced voltages. However, if the number of levels are increases, the number of components required are more this results into reduction of overall reliability and efficiency of power converter. On the other hand, solution with a low number of levels either need a rather large and expensive LC filter to limit the motor winding insulation stress or can only be used with motors that do withstand such stress.

II. CASCADED STRUCTURE AND ITS OPERATION

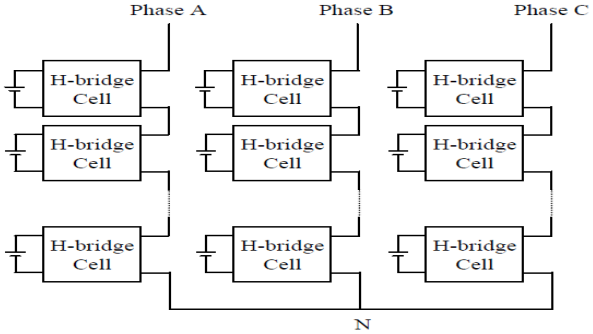


Fig.2 Structure of m-cells cascaded multilevel inverter.

The Fig.2 shows, structure of m-cells cascaded multilevel inverter. In which, each phase consists of H-bridge cell connected in series with other H-bridge cell. Same is true for all three phases. Such a structure is known as cascade ding. The structure of single H-bridge cell is shown in Fig.3.

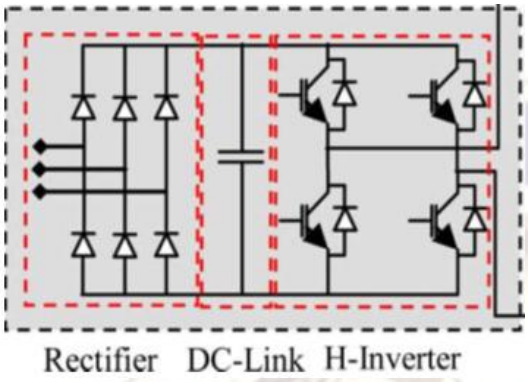


Fig.3 H-bridge cell structure.

As shown in fig., the four IGBT's are arranged in bridge fashion in order to form single phase H-bridge. Which is supplied by an isolated dc source on dc side, which can be obtained from batteries, fuel cell, or ultracapacitors. The advantage of this topology is that the modulation, control, and protection requirements of each bridge are modular. It should be pointed out that, unlike the diode-clamped and flying-capacitor topologies, isolated dc sources are required for each cell in each phase.

In symmetrical multilevel inverter, all H-bridge cells are fed by equal voltages, and hence all the arm cells produce similar output voltage steps. However, if all the cells are not fed by equal voltages, the inverter becomes an asymmetrical one. In this inverter, the arm cells have different effect on the output voltage. An output phase-voltage waveform is obtained by summing the bridges output voltages,

$vo\ (t) = vo,1\ (t) + vo,2\ (t) + \cdots + vo,N\ (t)$ (1)

where, N is the number of cascaded bridges.

The inverter output voltage $vo\ (t)$ may be determined from the individual cells switching states,

$vo\ (t) = \sum_{j=1}^{N} (\mu j - 1) Vdc, j,$ $\mu j = 0, 1, \ldots .$ (2)

If all dc-voltage sources in Fig. 1 are equal to Vdc, the inverter is then known as a symmetric multilevel one. The effective number of output voltage levels n in symmetric multilevel inverter is related to the cells number by,

$n = 1+2N$ (3)

The maximum output voltage Vo,Max is then

Vo,MAX = NVdc. (4)

To provide a large number of output levels without increasing the number of inverters, asymmetric multilevel inverters can be used. It is proposed to chose the dc-voltages sources according to a geometric progression with a factor of 2 or 3. For N of such cascade inverters, one can achieve the following distinct voltage levels,

$$\begin{cases} n = 2^{N+1} - 1, & if\ V_{dc,j} = 2^{j-1} V_{dc,} \quad j = 1,2,\ldots,N \\ n = 3^{N}, & if\ V_{dc,j} = 3^{j-1} V_{dc,} \quad j = 1,2,\ldots,N \end{cases}$$

Table 1. Comparison of Multilevel Inverter

	Symmetrical inverter	Asymmetrical inverter	
		Binary	Ternary
N	2N+1	$2^{N+1} - 1$	3^N
DC sources number	N	N	N
Switch number	4N	4N	4N
$V_{o,MAX}[pu]$	N	$2^N - 1$	$(3^N - 1)/2$

The maximum output voltage of these N cascaded multilevel inverters is,

Vo,MAX = $\sum_{j=1}^{N} Vdc, j,$ (6)

Equation (6) can be rewritten as,

$$\begin{cases} V_{o,MAX} = (2^N - 1) V_{dc,} \\ if\ V_{dc,j} = 2^{j-1} V_{dc,} \quad j = 1,2,\ldots,N \\ V_{o,MAX} = \left(\frac{3^N - 1}{2}\right) V_{dc,} \\ if\ V_{dc,j} = 3^{j-1} V_{dc,} \quad j = 1,2,\ldots,N \end{cases} \quad (7)$$

Comparing (3) to (7), it can be seen that asymmetrical multilevel inverters can generate more voltage levels and higher maximum output voltage with the same number of bridges.

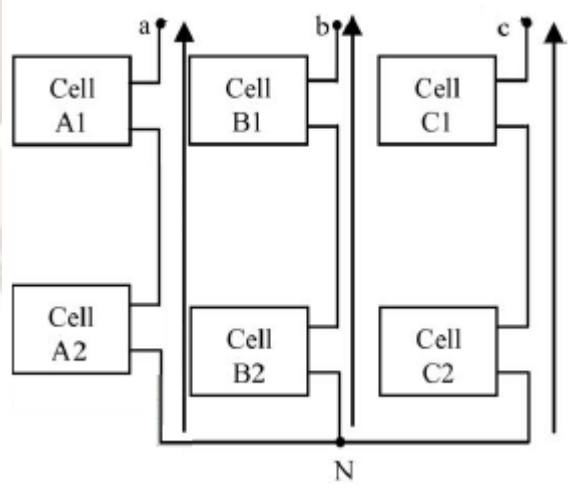
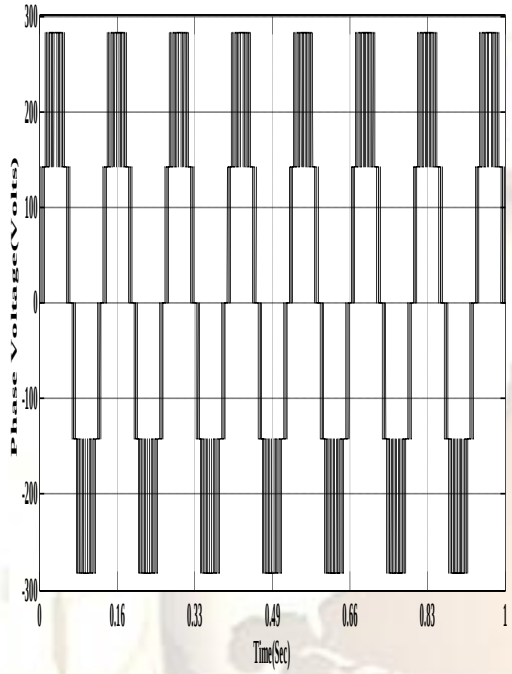


Fig.4 Block diagram of five level inverter.

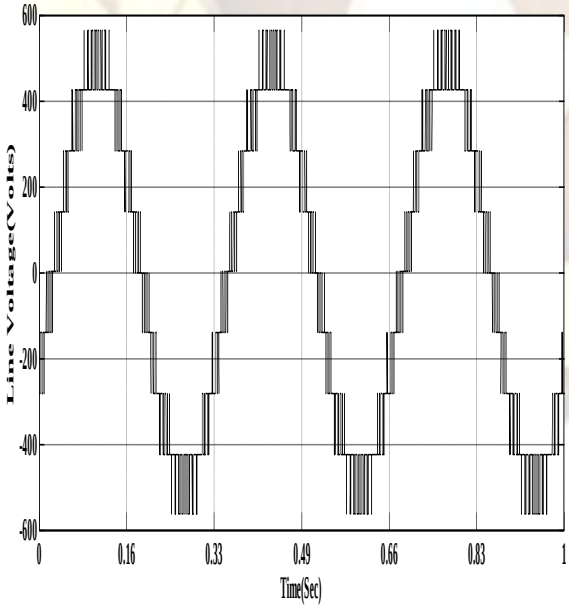
As shown in fig.4, if the each upper H-bridge cell in each phase is supplied by 2Vdc and if each lower H-bridge cell in each phase is supplied

by Vdc then we are able to obtained the same value of output voltage but with seven levels. Similarly, if the each upper H- bridge cell in each phase is supplied by 3Vdc and if each lower H-bridge cell in each phase is supplied by Vdc then we are able to obtained the same value of output voltage but with nine levels.

III. RESULTS

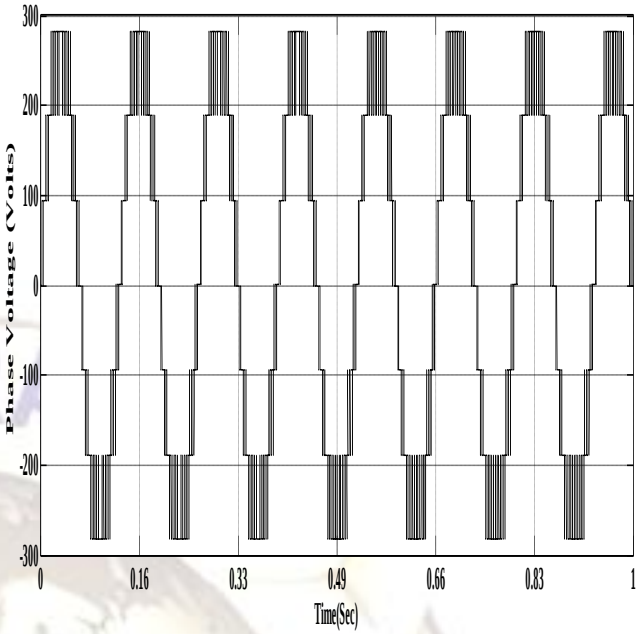


(A)

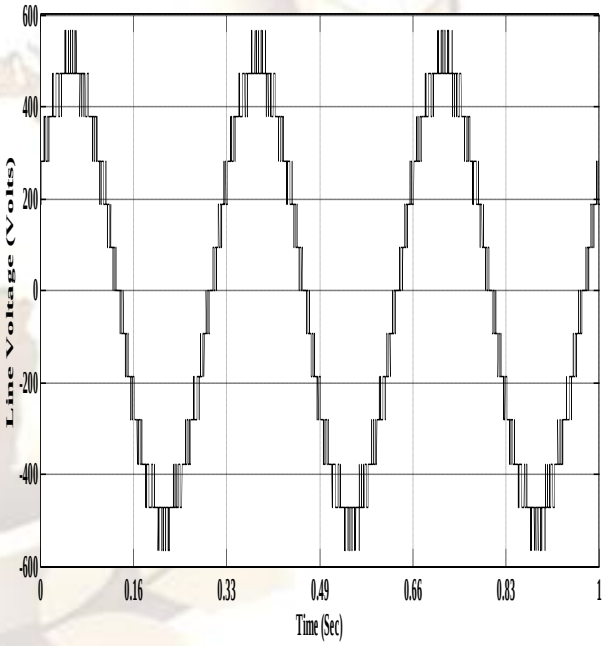


(B)

Fig.5 Simulation Results For 5- Level Symmetric Cascaded H-Bridge Multilevel Inverter, A) Phase Voltage; B) Line Voltage.

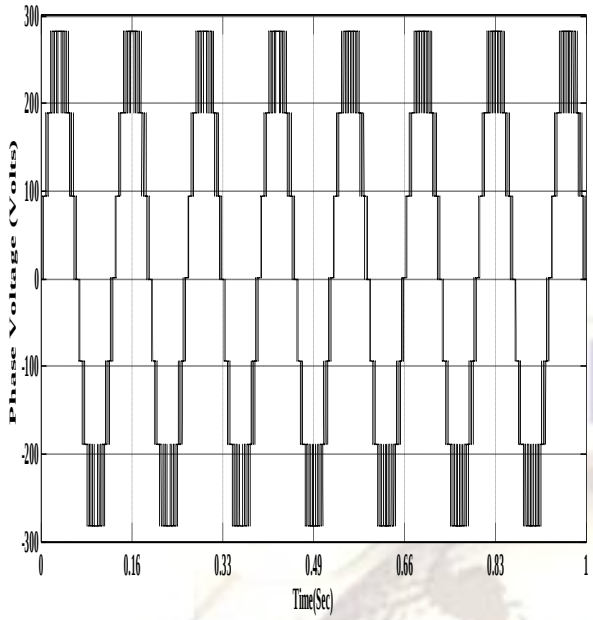


(A)

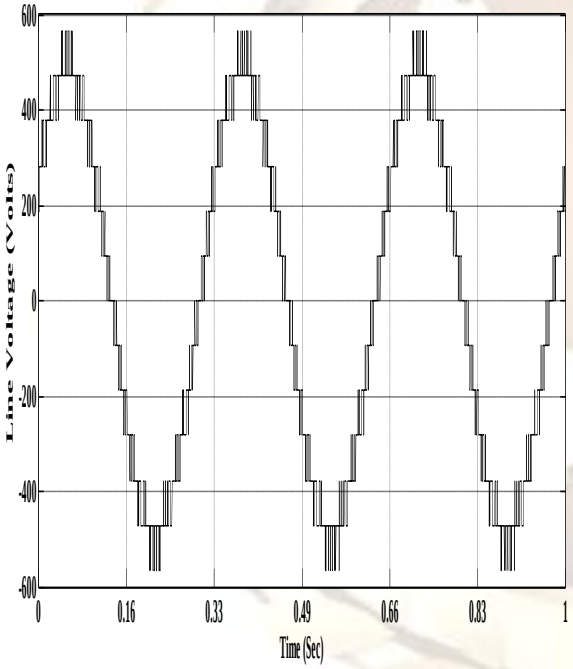


(B)

Fig.6 Simulation Results For 7- Level Symmetric Cascaded H-Bridge Multilevel Inverter, A) Phase Voltage; B) Line Voltage.



(A)



(B)

Fig.7 Simulation Results For 7- Level Asymmetric Cascaded H-Bridge Multilevel Inverter, A) Phase Voltage; B) Line Voltage.

IV. CONCLUSION

From above waveforms and table we concluded that, the Asymmetrical inverter is able to produce same value of output voltage but with more number of levels thus the output voltage has less harmonics and it is more pure than Symmetrical one. The number of bridges and DC sources, switching losses are also reduced in asymmetric MLI as compared to symmetrical.

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