Ujwal Shirode, Ajay Gadhe / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 3, Issue 1, January -February 2013, pp.876-879

Read stability and read failure analysis of low voltage Schmitt-Trigger based SRAM bitcell

Ujwal Shirode[*], Ajay Gadhe[**]
[*](Department of Electronics, North Maharashtra University, Jalgaon- 425001)
[**] (Department of Electronics, North Maharashtra University, Jalgaon- 425001)

ABSTRACT

We analyze Schmitt-Trigger (ST) based differential sensing static random access memory (SRAM) bitcells for ultralow voltage operation. The ST-based SRAM bitcells address the fundamental conflicting design requirement of the read versus write operation of a conventional 6T bitcell. The ST operation gives better read-stability as well as better read-failure probability compared to the standard 6T bitcell. The proposed ST based bitcells incorporate a built-in feedback mechanism. Balancing the trade-offs between small areas, low powers, fast reads/writes are an essential part of any SRAM design. That is, SRAM design requires balancing among various design criteria such as minimizing cell area using smaller transistor, maintaining read/write stability, minimizing power consumption by reducing power supply, minimizing read/write access time, minimizing leakage current, reducing bit-line swing to reduce power consumption. A detailed comparison of 6T bitcell shows that the ST based bitcell can operate at lower supply voltages. Measurement results in 130-nm CMOS technology show that the proposed ST based bitcell gives 1.6 higher read static noise margin and 180mV lower read Vmin compared to the 6T bitcell.

Keywords - **Low power SRAM, low voltage SRAM, Read stability, Schmitt trigger.**

1. INTRODUCTION

The power requirement for battery operated devices such as cell phones and medical devices is even more stringent with the scaling of the device dimensions. Reducing the supply voltage reduces the dynamic power quadratically and leakage power linearly [1]. Hence, supply voltage scaling has remained the major focus of low-power design. This has resulted in circuits operating at a supply voltage lower than the threshold voltage of a transistor [2]. However, the reduction in supply voltage may lead to increased memory failures such as read-failure, hold failure and write-failure [3], [4].

For a stable SRAM bitcell operating at lower supply voltages, the stability of the inverter pair should be improved. None of the aforementioned bitcells has a mechanism to improve the stability of the inverter pair under low voltage operation. The proposed Schmitt trigger based differential bitcell having built-in feedback mechanism for improve the stability of the inverter pair under low voltage operation [4].

2. SIX TRANSISTOR SRAM CELL

The 6-transistor (6T) cell which uses a cross-coupled inverter pair is the de facto memory bitcell used in the current SRAM designs. The conventional 6T SRAM cell design is as shown in Fig.1. 6T cell utilize differential read operation [5].

The memory cell in SRAM consists of two static inverters that feed into each other creating a latch. Access into the memory cell is controlled through access transistor logic connected between the read/write logic and the memory cell itself and the switching for the transistor logic is controlled by word lines [6].

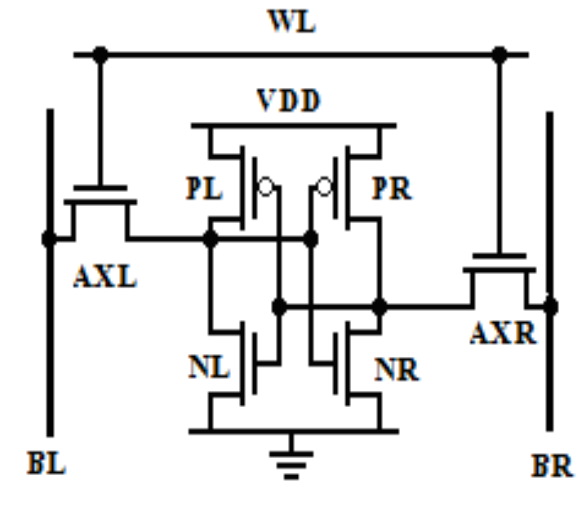

Figure 1: 6T SRAM cell

The proposed Schmitt trigger based differential 10-transistor SRAM bitcell have built-in feedback mechanism. It requires no architectural change compared to the 6T cell architecture. It can be used as a drop-in replacement for present 6T based designs. With respect to 6T cell, the proposed Schmitt trigger based bitcell gives better read stability, better write-ability, lower read failure probability, low-

voltage/low power operation, and improved data retention capability at ultralow voltage.

3. SCHMITT TRIGEER

The proposed ST based 10-transistor SRAM cell focuses on making the basic inverter pair of the memory cell robust. At very low voltages, the cross-coupled inverter pair stability is of concern. To improve the inverter characteristics, Schmitt trigger configuration is used. A Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction of the input transition [7]. This adaptation is achieved with the help of a feedback mechanism.

One possible implementation of a Schmitt trigger is shown in Fig. 2.This structure is used to form the inverter of our memory bitcell. The basic Schmitt trigger requires six transistors instead of two transistors to form an inverter. Thus, it would need 14 transistors in total to form an SRAM cell, which would result in large area penalty. Since PMOS transistors are used as weak pull-ups to hold the "1" state, a feedback mechanism in the PMOS pull-up branch is not used. Feedback mechanism is used only in the pull-down path. The modified Schmitt trigger schematic is shown in Fig. 2.

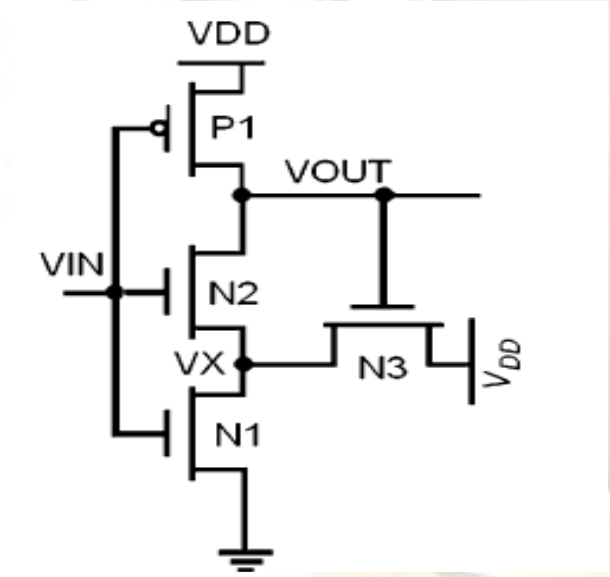

Figure 2: Modified Schmitt- trigger used to form the inverter of memory bitcell.

4. SCHMITT TRIGEER BASED SRAM BITCELL

The complete schematic for the proposed ST based SRAM bitcell is as shown in Fig. 3. Transistors PL-NL1-NL2-NFL forms one ST inverter while PR-NR1-NR2-NFR forms another ST inverter. AXL and AXR are the access transistors. The positive feedback from NFL/NFR adaptively changes the switching threshold of the inverter depending on the direction of input transition. During a read operation (with say VL="0" and VR= VDD), due to voltage divider action between the access transistor and the pull-down NMOS, the voltage of VL node rises. If this voltage is higher than the switching threshold (trip point) of the other inverter, the contents of the cell can be flipped, resulting in a read failure event [8].

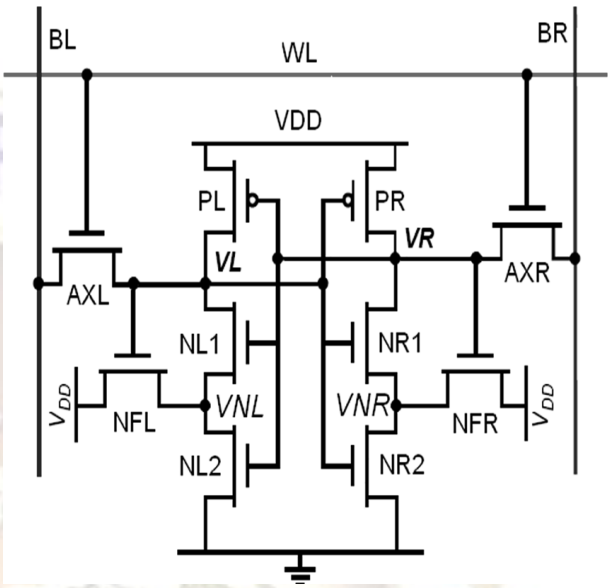

Figure 3: schematic for the ST based SRAM bitcell

In order to avoid a read failure, the feedback mechanism should increase the switching threshold of the inverter PR-NR1-NR2. Transistors NFR and NR2 raise the voltage at node VNR and increase the switching threshold of the inverter storing "1". Thus, Schmitt trigger action is used to preserve the logic "1" state of the memory cell [9].

The proposed ST based SRAM bitcell utilizes differential operation, giving better noise immunity [7]. It requires no architectural change compared to the conventional 6T cell architecture and hence can be used as a drop-in replacement for the present 6T based designs.

5. SIMULATION RESULTS

HSPICE simulations are done using 130nm logic process technology. Typical NMOS (PMOS) threshold voltage is 300 mV. The 6T and the proposed ST based bitcells are compared for various SRAM metrics. For the 6T SRAM bitcell, the transistor widths WPU/WAX/WPD are 160nm/240nm/320nm, respectively. For the ST based SRAM bitcell, extra transistors NFL/NL2 are of minimum width 160 nm while the other transistors have the same dimensions as those of the 6T cell.

5.1 Read Stability

For improving the cell stability, the proposed ST based SRAM bitcell focuses on making the inverter

pair robust. Feedback transistors NFL/NFR increase the inverter switching threshold whenever the node storing "1" is discharged to the "0" state. Thus, cell asymmetry changes based on the direction of the node voltage transition. When node VL is increased from "0" to VDD, the other node (VR) makes a transition from VDD to "0". During this time, the feedback mechanism due to NFR-NR2 raises the node voltage VNR and tries to maintain the logic "1" state of the VR node. This gives near-ideal inverter characteristics essential for robust memory cell operation. The static noise margin (SNM) is estimated graphically as the length of a side of the largest square that can be embedded inside the lobes of the butterfly curve [10].

The read static noise margin of 6T and ST based SRAM bitcell for different supply voltages is mentioned in Table 1. Simulation result shows that the read SNM is improved in ST based bitcell than 6T bitcell.

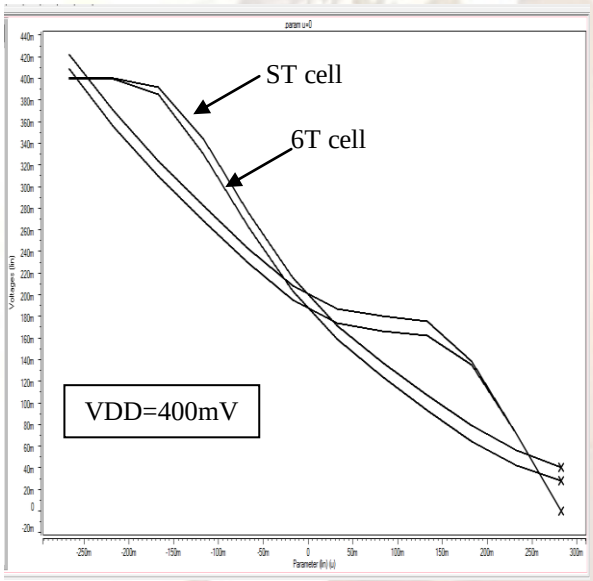

Figure 4: Read SNM curve for 6T and ST based bitcell at lower supply voltage (VDD=400mV)

The minimum sized ST based bitcell gives 1.52 percent larger (improved) in read SNM over the 6T cell (VDD=400 mV), shown in Fig. 4. This shows that for a stable SRAM cell operating at a lower supply voltage, a feedback mechanism can be more effective than simple transistor upsizing as in a conventional 6T cell.

..

Table 1: Read SNM for 6T and ST cell at different supply voltages

Supply voltage (V)	6T cell read SNM (mV)	ST cell read SNM (mV)
1.2	70	65
1	65	60
0.8	55	40
0.6	45	35
0.4	42	28
0.3	Read Failure	26
0.22	Read Failure	26

5.2 Read failure probability

Supply voltage is reduced gradually from the nominal value of 1.2V to the point where memory cell contents are about to flip or reach a metastable point. It is observed that, the ST based bitcell operates at a lower voltage than the conventional 6T cell. Due to reduced VDD, the ST based bitcell consumes lower leakage power compared to the 6T cell despite four extra transistors. As the access transistor size in the ST based bitcell is the same as the 6T cell, the bit-line diffusion capacitance and word-line gate capacitance is unchanged. This reduces read/write dynamic power dissipation quadratically ($CLV^2_{DD}f$) with reduced VDD. Note that the difference in minimum VDD increases as the read failure probability decreases. When butterfly curve is not valid, the read operation is failed. Simulation results show that the 6T bitcell and ST based bitcell fails in read operation below 400mV and 220mV respectively shown in Fig. 5.

It is observed that the proposed ST based bitcell operates at 180 mV lower supply voltage than the 6T cell at supply voltage VDD=400mV.As technology scales, with increased process variations, the memory cell failure probability would worsen at lower supply voltages. In such a scenario, the proposed ST based bitcell with built-in feedback mechanism could be useful for low VDD operation.

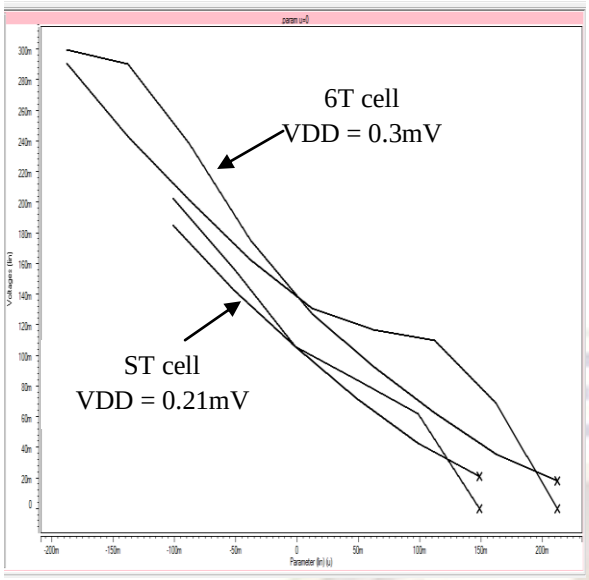

Figure 5: Read SNM failure comparison of 6T bitcell and ST based bitcell at lower supply voltage (VDD=400mV)

6. CONCLUSION

The proposed Schmitt trigger based differential, robust, 10-transistor SRAM bitcell suitable for subthreshold operation. The proposed ST based bitcell achieves higher read SNM (1.56% larger) compared to the conventional 6T cell (VDD=400mV). It incorporates differential operation and hence it does not require any architectural changes from the present 6T architecture. At iso area read-failure probability, the proposed ST based bitcell operates 180mV lower VDD than the 6T bitcell.

Simulation results shows that, the proposed ST based SRAM bitcell gives more stability in read operation with reduced power supply voltage and correspondingly the read failure probability also decreases as compare to conventional 6T SRAM bitcell.

Lowering the supply voltage is an effective way to achieve ultra-low-power operation. In this work, we evaluated ST based SRAM bitcells suitable for ultra-low voltage applications. The built-in feedback mechanism in the proposed ST based bitcell can be effective for process-tolerant, low-voltage SRAM operation in future nano scaled technologies. Simulation results show that the ST based bitcell can retain the data at low supply voltage (150 mV).

ACKNOLEDGMENT

The authors are highly thankful to Dr. D.K.Gautam, head of the department of electronics, North Maharashtra University, for their regular support. The authors are again grateful to the faculty of Department of Electronics for their moral support.

REFERENCES

[1] H. Soeleman and K. Roy, Ultra-low power digital subthreshold logic circuits, *Proc. Int. Symp. Low Power Electronics and Design (ISLPED'98)*, 1998, 94–96.

[2] K. Roy and S. Prasad, *Low Power CMOS VLSI Circuit Design* (New York: Wiley, 2000).

[3] N.Yoshinobu, H. Masahi, K. Takayuki and K. Itoh, Reviewand, future prospects of low-voltage RAM circuits, *IBM J. Res. Devel., vol. 47, no. 5/6*, 2003 525–552.

[4] A.Raychowdhury, S.Mukhopadhyay, and K. Roy, A feasibility study of subthreshold SRAM across technology generations, *in Proc. Int. Conf. Computer Design*, Oct. 2005, 417–422.

[5] J. Chen, L. Clark, and T. Chen, An ultra-low-power memory with a subthreshold power supply voltage, *IEEE J. Solid-State Circuits, vol. 41, no. 10*, Oct. 2006 2344–2353.

[6] A. Bhavnagarwala, X. Tang, and J. Meindl, The impact of intrinsic device fluctuations on CMOS SRAM cell stability, *IEEE J. Solid-State Circuits, vol. 36, no. 4*, Apr. 2000, 658–665.

[7] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Design Perspective* (2nd ed. Englewood Cliffs, NJ: Prentice Hall, 2002.)

[8] S. Mukhopadhyay, H. Mahmoodi, and K. Roy, Modeling of failure probability and statistical design of SRAM array for yield enhancement in nanoscaled CMOS, *IEEE Trans. Comput. Aided Des, vol. 24, no.12*, Dec. 2005 1859–1880.

[9] Jaydeep P. Kulkarn, Keejong Kim, and Kaushik Roy, A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM *IEEE Journal Of Solid-State Circuits, Vol. 42, No. 10*, October 2007

[10] E. Seevinck, F. List, and J. Lohstroh, Static noise margin analysis of MOS SRAM cells, *IEEE Solid-State Circuits, vol. SC-22, no. 5*, Oct. 1987, 748–754.