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Design and Analysis of 6T SRAM Cell with low Power Dissipation

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Abstract

In the current technology demand for SRAM is increasing drastically due to its usage in almost all embedded systems, forms a integral part of computer, System On Chip and high performance processors and VLSI circuits etc. The Power Consumption has become a major concern in Very Large Scale Integration circuit designs and reducing the power dissipation has become challenge to the Low power VLSI designers. As power dissipation increases with the scaling of the technologies. As the feature size shrinks ,static power has become a great challenge for current and future technologies. In this research work, we design 6T SRAM and some of the techniques to reduce the leakage power using like sleep approach, stack approach techniques which reduces the leakage power without changing the exact operation of SRAM. The proposed circuits were designed in 0.18um CMOS VLSI technology with a Microwind tool, and measure the power dissipation for the different design approach in Advanced BSIM4 level. Power reduction is achieved with associated area overhead. The total power dissipation is lower by 40% as compared to the 6T SRAM cell.

key words- Power dissipation, sleep, stack, leakage power.

I. INTRODUCTION

SRAM has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand held communication devices. Power dissipation consists of dynamic power and static power. Static power is the power dissipated in the design in the absence of any switching activity and is defined as the product of supply voltage and the leakage current.

The rising demand for multimedia rich applications in handheld devices continues to drive the need for large and high speed SRAM to enhance the system performance. The portable hand held devices need to reduce the dynamic and static power consumption in order to meet the battery life time. In this work an attempt has been made to reduce the leakage power by adding some transistors. Each technique provides an efficient way to reduce the leakage power, but disadvantage of each technology limit the application of each technique. In this paper SRAM cell was designed with different technology and analyze the power consumption in each technique.

II. CONVENTIONAL 6T SRAM CELL

In a 6T cell, it consists of 6 Transistors and each bit in SRAM is stored on four transistors that form two cross- coupled inverters. This storage cell has two stable states which is used to denote 0 and 1. Two nMOS transistors serves as the access transistors to control the access to storage cell during read and write operation. Access to the cell is enabled by the word line which controls the two access transistors M5 and M6 which in turn control whether the cell to be connected to BL and BLB. They are used to transfer data for both read and write operations. Both BL and BLB are used to improve the Noise Margins.

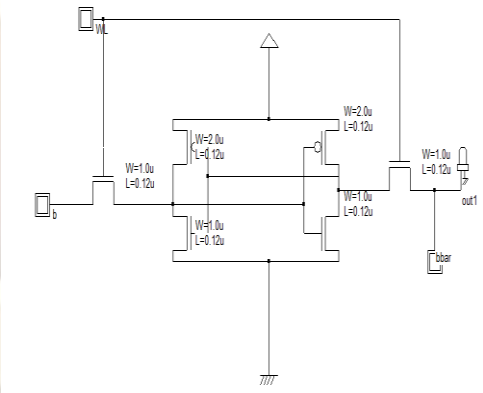

Fig1a: Schematic for basic 6T SRAM Cell

III. LEAKAGE POWER REDUCTION CIRCUITS

A. SRAM Cell with Sleep Transistor

In present deep-sub micrometer devices with low threshold voltages, sub threshold and gate leakage are dominant sources of leakage and are expected to increase with the technology scaling. Solutions for leakage reduction is required at the both process technology and circuit levels [3]. One of the methods is to have an nMOS connected to virtual ground terminal as shown in Fig.2 . Effect of sleep transistor is negligible as far as error is concerned.

The sleep transistor is required to completely discharge virtual ground to real ground prior to turning on the write line (WL) of cell.

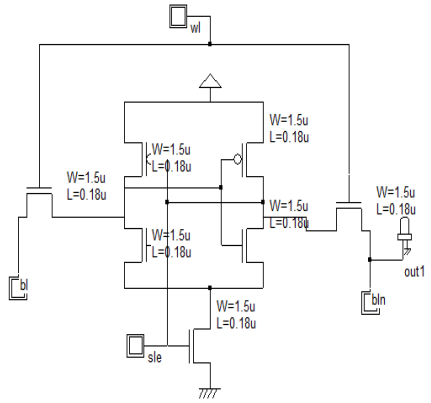

Fig 2a: schematic of SRAM Cell with Sleep transistor

Sleep signal is high in normal operation and present as small resistance as possible. Proper selection of sleep transistor is required as it affect the trade off. It should be wide to minimize supply fluctuation. At the same time higher threshold result in better leakage suppression [6]. This 6T SRAM contain two cross coupled inverters suitable for low power design. The sizing of inverters in SRAM cell does not correspond to electron hole mobility ratio, also the access transistors must be sized such that stored bits are not flipped during a read operation . Thus driver nMOS transistors must be stronger (larger W/L) than access transistors.

B. Ultra Low-power 8T SRAM Cell

The 8T SRAM cell consists of two cross-coupled inverters made up of transistors M1, M3 and M2, M4. The transistors M5, M6 are access transistors. The two additional NMOS transistors M7 and M8, one each in pull down path of cross coupled inverters are used to achieve leakage power reduction. The access transistors are connected to the word line at their respective gate terminals, and the bit-lines at their drain terminals. The word line is used to select the cell while the bit lines are used to perform write and read operations on the cell. The node Q holds the stored value while other node QN holds its complement. The two complementary bit lines are used to improve speed of write and read operations. The 8T SRAM cell is shown in Fig. 2. The SRAM cell is symmetric and hence M1=M2, M3=M4, M5=M6, M7=M8 [1].

During write operation, word line (WL) is made '1' and data to be written and its complement are imposed on the two complementary bit lines, BIT and BITN. The data on the bit lines gets stored onto the SRAM cell nodes 'Q' and 'QN' through access transistors, M5 and M6.[7]

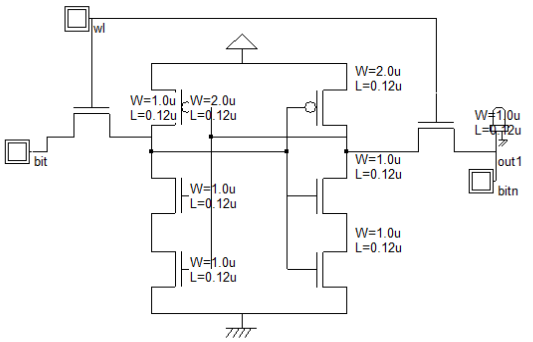

Fig 3a: Schematic of Ultra Low-power 8T SRAM Cell

The information written in the SRAM cell gets reinforced by the action of pMOS and nMOS transistors in either inverter, as long as the power is there. During inactive state, WL=0, but due to the cross coupled inverters and low power stack transistors, M7 and M8, in the pull-down path, data stored remains uncorrupted, at reduced power.

C. 6T SRAM Cell using stacking Technique

In the 6T SRAM cell, is shown in Fig.4a the transistors M8, M4, M10 and M6 form cross coupled inverters. The basic idea behind our approach for reduction of leakage power is the effective stacking of transistors in the path from supply voltage to ground. This is based on the observation made in [4] that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path." In our method, we introduce two leakage control transistors in each inverter pair such that one of the leakage control transistor is near its cutoff region of operation. Two leakage control transistors (PMOS) and (NMOS) are introduced between the nodes and of the pull-up and pull-down logic of the inverter. The drain nodes of the transistors and are connected together to form the output node of the Inverter. The source nodes of the transistors are connected to nodes of pull-up and pull-down logic, respectively. The switching of transistors is controlled by the voltage potentials at nodes respectively. This wiring configuration ensures that one of the leakage control transistor is always near its cutoff region, irrespective of the input. Hence the resistance of will be lesser than it's OFF resistance, allowing conduction. Even though the resistance of is not as high as it's OFF state resistance, it increases the resistance of to ground path, controlling the flow of leakage currents, resulting in leakage power reduction. Thus, the introduction of leakage control transistors increases the resistance of the path from supply voltage to ground[5].

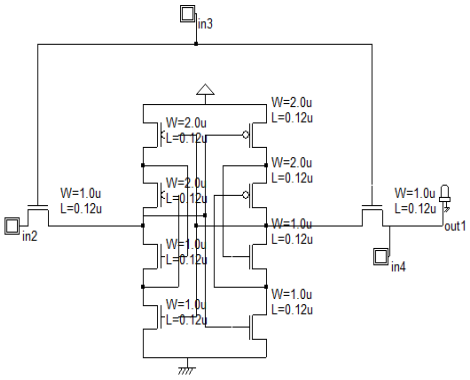

Fig4a: Schematic of 6TSRAM Cell using stacking Technique

IV. MOTIVATION

In the past few years a remarkable rise in VLSI fabrication has led to increase the densities of integrated circuits by decreasing the device geometries. Such high density circuits support high design complexities and very high speed but susceptible to power consumption. Circuits with excessive power dissipation are more susceptible to run time failures and give rise to reliability problems. The other factors behind the low power design is growing class of hand held devices, e.g., as portable desktops, digital pens, audio and video based multimedia products and wireless communications such as PDA's and smartcards, etc.[2]

These devices and systems demand high speed and complex design functionalities. The performance of these devices is limited by the size, weight and lifetime of portable batteries. Memory design is an integral part in these devices and so reducing the power dissipation in these can improve the system power efficiency, performance, reliability. In this paper provides the some possible solutions for low power dissipation which in turn provides Low power SRAM Cell required for designing memory systems.

V. SIMULATION RESULTS

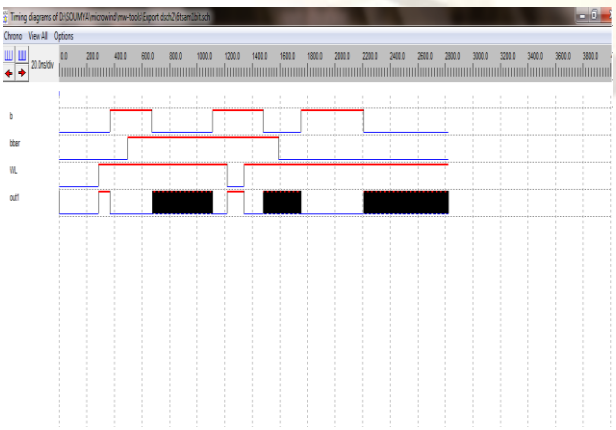

Fig1b: Simulation results for basic 6T SRAM Cell

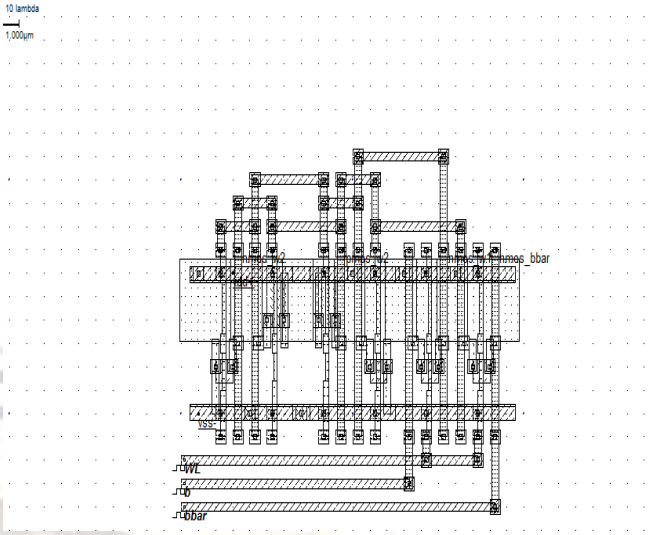

Fig 1c: Layout for basic 6T SRAM cell

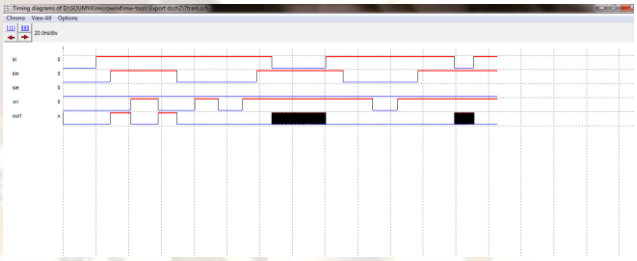

Fig2b: Simulation results of SRAM Cell with Sleep transistor

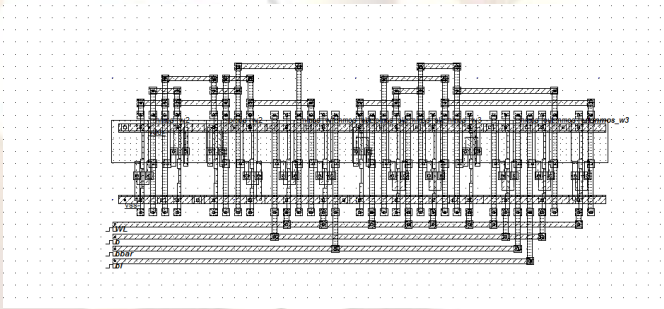

Fig2c: Layout of SRAM Cell with Sleep transistor

Fig3b: Simulation results of *Ultra Low-power 8T SRAM Cell*

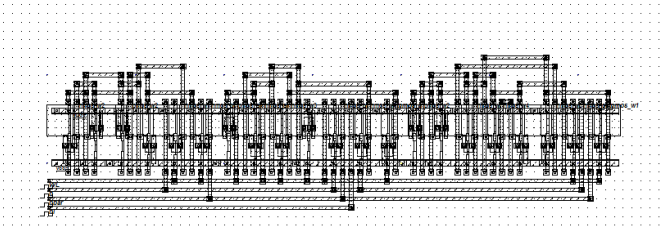

Fig 3c: Layout of Ultra Low-power 8T SRAM Cell

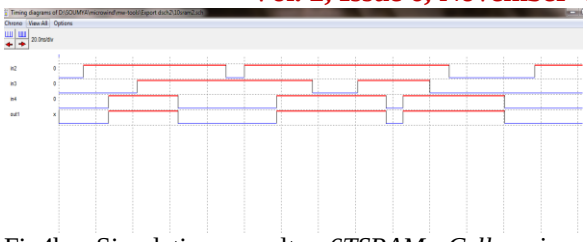

Fig4b: Simulation results *6TSRAM Cell using stacking Technique*

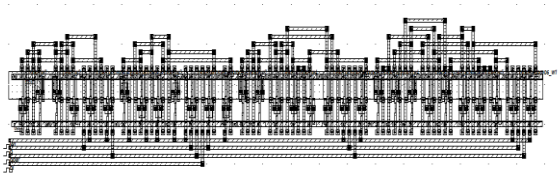

Fig4c:Layout of 6TSRAM Cell using stacking Technique

Power dissipation Analysis between Basic SRAM and SRAM using leakage power reduction technique

Technology	Basic SRAM	SRAM with sleep transistor(7T)	SRAM with sleep transistor(8T)	SRAM with stack approach
180um	0.190mW	0.126mW	0.101nW	0.453mW
120um	0.111mW	0.318mW	0.231nW	0.11mW
90nm	70.367uW	2.545uW	0.162nW	8.839uW
70nm	5.939uW	0.446uW	1.620uW	18.238uW
50nm	3.445uW	0.136uW	0.448uW	2.459uW

VI.CONCLUSION

In this paper we designed SRAM cell using leakage power reduction techniques, to reduce power dissipation. The anticipated circuits were designed in 0.18um technology and analyzed for power dissipation. Here we observed that in order to achieve low power consumption we compromised with area and delay compared to the basic 6T SRAM .based on the simulation results of SRAM, there is 40% reduction in power dissipation. Hence we conclude the proposed SRAM circuits used for low power designs and these designed techniques are used to improve the performance and can be used for low power applications.

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