C-V Investigation in Optically Illuminated MOSFET

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ABSTRACT

A thorough investigation of N-channel multifinger MOSFET capacitances in dark and under optical illumination is presented in this paper. The intrinsic and extrinsic capacitances are modelled and analysed considering the scaling effects for sub-micron scale MOSFET. Bias dependence is taken into account and capacitances essential for small signal model for RF frequency operation are evaluated. The MOSFET under illumination indicates reduction in capacitance *Cgs* indicating its potential in analog and mixed signal applications at RF.

Keywords - Capacitance, Modelling, MOSFET, Opto-electronics, Photo-detector, RF

I. INTRODUCTION

Advances and maturation in CMOS technology has resulted in feasibility of MOS circuits operating at RF. Transit frequency, Maximum frequency of oscillation and Noise Fig. are major considerations for operation at RF [1]. MOSFET channel length reduction is one of the most conventional and powerful method to improve device performance. The aggressive scaling in spite of several advantages, has trade-offs associated with it. This makes it essential to use alternative methods rather than scaling, to improve device characteristics. One way is optoelectronic integration by illuminating the device with intensity modulated wave with energy greater than bandgap energy. Optoelectronic and RF CMOS integration offers all the benefits like immunity to electromagnetic interference, better reliability etc [2].It also gives an additional independent control port along with all the advantages of optoelectronics This renders control over operating region of the device which is crucial in submicron dimension especially when device is operating at high frequency.

When the device operates at RF, device modelling is one of the major issues and plays a dominant role. The exploration and modelling of capacitances at high-frequency in MOSFET is vitally important because capacitances play an important role in deciding operating frequency of the device and hence performance at RF. [3]. Investigation of intrinsic capacitances at medium frequency for a small signal model of optically controlled MOSFETS has been

done in [4]. To our knowledge, the effect of light illumination on the MOSFET capacitances at RF has received no attention. In this paper detailed analysis of extrinsic and intrinsic capacitances has been made at DC and RF, and the device structure is also modified to multifinger MOSFET accordingly. Analysis has been done with bias dependence for the total capacitance in dark condition and with varying optical power.

Content organization in the paper is as follows. Section-II deals with calculation of photo voltage for MOSFET under illumination, section-III presents theory for MOSFET capacitances, and the relevant calculations. Section IV covers the results and discussions that arise out of the simulation and section-V deals with the major conclusions drawn from the investigation and finally the references. Device is expected to emerge as the prospective device for RF applications with better control and can be integrated as optically controlled MMIC, OEICs, ASIC design etc.

II. MOSFET UNDER ILLUMINATION

Investigations have been done on an MIS device which can be modified to optically gated MISFET (OG-MISFET). One of the key device structures is $Si\text{-}SiO_2$, and the device is referred to as optically gated OG-MOSFET (OG-MOSFET)[4].The device is modelled at higher range of frequency where consideration to extrinsic components has to be given, as against in low and medium frequency range.

The structure under consideration is an optically illuminated N – MOSFET as shown in Fig. 1. It is essential for a large device to reduce the gate resistance, while reducing gate length, and hence MOSFET with multi-finger gates with small finger widths is used. The device in Fig. -1 represents a single finger of the device. Optical radiation is perpendicular to the surface and the wavelength of radiation is higher than that of silicon bandgap energy and is considered to be of 830 nm for simulation purpose. Optical radiation is assumed to be incident in the non- metallic gate region which will be absorbed in the depletion region.

In N-MOSFET, the ion implanted channel profile in the active region of the device is represented by

$$N(y) = \frac{Q}{\sigma\sqrt{2\pi}}\exp\left(-\left(\frac{y - Rp}{\sigma\sqrt{2}}\right)^2\right) \quad (1)$$

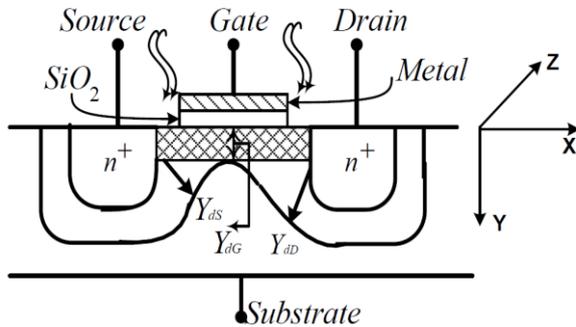Where Q is implanted dose, σ straggle parameter Rp projected range.

Fig. 1 Schematic of MOSGET under illumination

Illumination with source $h\nu \gg E_g$, causes the effective potential of gate to change as photo voltage develops at the MOS junction. This also causes change in channel conductivity and hence in total charge in channel. The total charge Q_G for the MOSFET includes the charge in inversion and depletion charges for as given in [5].

$$Q_G = -Q_I - Q_B \qquad (2)$$

Where Q_G is charge on gate, Q_I is the charge in channel, Q_B charge in the bulk.

$$Q_D = W.\int_0^L \frac{y}{L} Q'_I(y).dy \qquad (3)$$

The source charge is further obtained as

$$Q_s = Q_I - Q_D \qquad (4)$$

Under optical illumination the total charge changes

$$Q_{total} = Q_G + Q_{illumination} \qquad (5)$$

Q_G is charge under dark condition in the MOSFET,

$Q_{illumination}$ is induced charge due to illumination and can be calculated as in [7]. The external photovoltage across the junction is obtained using the relation [8]

$$Vop = \frac{KT}{q}\ln\left(\frac{Jp}{Js}\right) = \frac{KT}{q}\ln\left(\frac{qv_y p(0)}{Js_1}\right) \qquad (6)$$

Where Js is the reverse saturation current, v_y is the carrier along vertical direction perpendicular to the device surface,

$p(0)$ is number of holes crossing junction at $y=0$, given by

$$p(0) = \frac{\Pi}{4}Z(p_1 YdS^2 + p_2 YdD^2) \qquad (7)$$

Where p_1 and p_2 are the constants dependant on carrier lifetime under ac conditions.

Y_{dD} and Y_{dS} is depletion width at drain and source end.

Z is the device width.

The calculation of photovoltage is important as it modifies the depletion width Y_{dG} (depletion width at gate).Using abrupt junction approximation the Y_{dG}(under dark condition) and Y'_{dG} under illumination are calculated as given below[7],[8]

$$Y_{dG}(x) = \left(\frac{2\varepsilon}{qN_{dr}}(\varphi_B - \Delta + V(x) - V_{GS})\right)^{1/2} \qquad (8)$$

$$Y'_{dG}(x) = \left(\frac{2\varepsilon}{qN_{dr}}(\varphi_B - \Delta + V(x) - V_{GS} - V_{op})\right)^{1/2} \qquad (9)$$

Where $V(x)$ is channel voltage, φ_B built in potential, Δ is the position of Fermi-level below conduction band. Due to the photo voltage developed the effective bias across gate changes to $(V_{GS} + V_{OP})$ from V_{GS}.

III. CAPACITANCE MODELLING IN MOSFET

Small signal models of device are required for analog and RF circuit design and consist of resistances, conductances and capacitances. At low frequencies, the impedance of the junction capacitance is large that the substrate impedance can be neglected. In RF MOSFETs, the distributed R–C network effects have to be given a thought and hence a four terminal MOSFET model along with depletion capacitances and the substrate resistances should be considered.

A four terminal MOSFET is under consideration as shown in Fig.-2[9].The schematic represents only the intrinsic components of the MOSFET. The intrinsic part is the core of the device and is caused by the gate induced charges in the channel region.
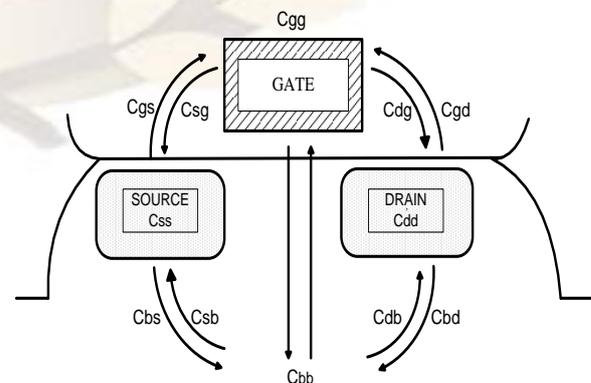

Fig. 2 Intrinsic Capacitances in MOSFET

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In a four terminal MOSFET the terminal charge Qx (in general is a function of terminal voltages Vy (x,y = G, S, D, B)

$$Cxyi = -\frac{\partial Qx}{\partial Vy} , x \neq y \; x, y = G, S, D, B$$

$$= \frac{\partial Qx}{\partial Vy} , x = y \qquad (10)$$

To calculate MOSFET intrinsic capacitances the charge, Q_I is calculated and hence Q_G, Q_D, Q_S and Q_B, are calculated as independent variables and as function of node voltages, so that charge conservation is assured as per [9]. The capacitances are calculated by evaluating the terminal charges using the following relation in(10)under dark and illuminated condition by calculating the corresponding charges under different illuminated condition as given in(5)

$$Cxyi = \frac{dQx}{dQy}\Big|other\, voltages\, const\Big|$$

$$= \frac{Qx(i+1)-Qx(i-1)}{Vy(i+1)-Vy(i-1)}\Big|other\, voltages\, const \qquad (11)$$

Thus, a four terminal device will have 16 capacitances, including 4 self capacitances corresponding to its 4 terminals. Though there are sixteen intrinsic capacitive elements only nine capacitances *Cggi, Cgdi, Cgsi, Cddi, Cdgi, Cdsi, Cssi, Csgi,* and *Csdi* are independent and other can be evaluated by application of charge conservation. It should be noted that capacitive elements *Csdi* and *cdsi* are exceptions for sign consideration.[9]. The terminal charge calculations in dark condition are done using equations of the charge based model as given in [10] capacitances are evaluated. The effect of optical illumination is modelled by calculating the charges with effective change in charges and bias voltage.

Fig. 3 indicates small signal model of MOSFET which is valid at low and medium frequency The capacitances indicated are intrinsic capacitances which can be evaluated by using expressions (10,11)
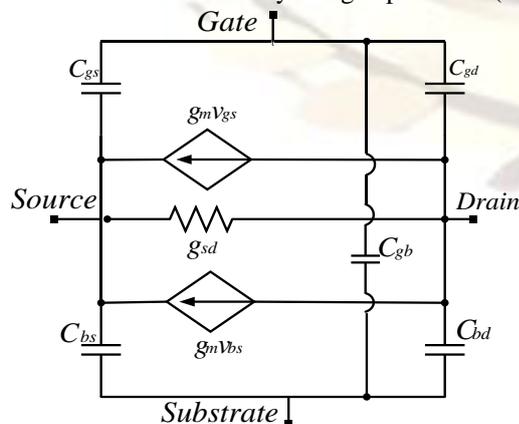

Fig. 3 Small Signal model for low and medium frequency

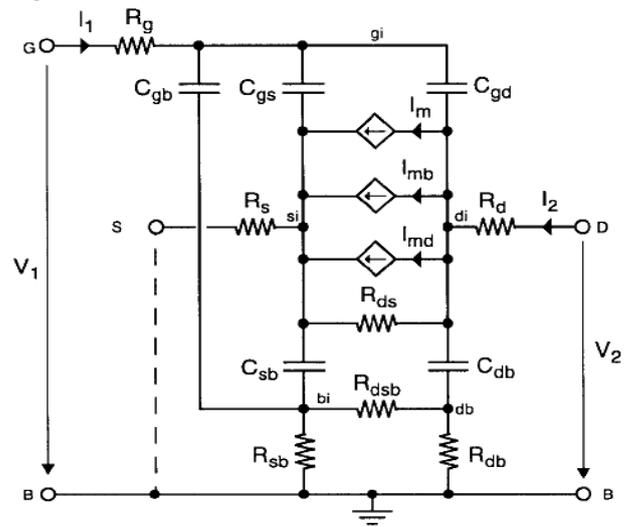For the MOSFET operated at RF, the model shown in Fig.-4 has to be considered.

Fig.4 Small Signal model valid at RF.

A complete small signal model, valid in all regions of operations of MOSFET valid upto 10 GHz frequency is shown in Fig. 4 is considered, as [5]. The RF model in Fig. 4 consists of additional capacitances as compared to model shown in Fig. 3. The capacitances indicated in the model at RF are combination of intrinsic capacitances and extrinsic capacitances. The intrinsic part of the device capacitances are related is evaluated in (10, 11).The extrinsic capacitance components primarily consist of source to bulk and drain to bulk reverse bias components, overlap and fringe capacitances. The dynamic behaviour of a MOSFET is due to the device capacitive effects, which in turn are the results of the charges stored in the device.

It is of prime importance to calculate the MOSFET capacitances and their dependence on externally applied voltages considering, charge non-conservation and reciprocity which are mutually exclusive. In order to simplify the circuit representation, the overlap capacitances and the junction capacitances are merged with corresponding intrinsic capacitances in Fig.-4. For a multifinger device L_G and W_G represent length and width of single finger. For the modelling of the device at RF the total capacitances under consideration are evaluated as in (12)

$$C_{gst} = C_{gsi} + C_{gso} \qquad (12a)$$
$$C_{gdt} = C_{gdi} + C_{gdo} \qquad (12b)$$
$$C_{gbt} = C_{gbi} + C_{gbo} \qquad (12c)$$
$$C_{bst} = C_{bsi} + C_{jbs} \qquad (12d)$$
$$C_{bdt} = C_{bdi} + C_{jbd} \qquad (12e)$$
$$C_{gg} = C_{gst} + C_{gbt} + C_{gdt} \qquad (12f)$$

The overlap capacitances can be calculated from length of gate-to-source, gate-to-drain) overlap area,

the length of heavily doped diffusion from contact to lightly doped region, by appropriate consideration of N_F i.e. the number of fingers, N_S the number of source diffusions, and $N_D = N_F + 1 - N_D$ is the number of drain diffusions as in[5]. The model also consists of transcapacitances Cm and Cms which are very important for accurate modelling at RF to calculate Y parameters.

$$C_m = C_{dgt} - C_{gdt} \qquad (13a)$$
$$C_{md} = C_{dbt} - C_{bdt} \qquad (13b)$$
$$C_{ms} = C_{gbt} - C_{bgt} \qquad (13c)$$

IV. RESULTS AND DISCUSSIONS

Simulations has been carried out for an N-MOSFET device with $N_F = 10$, $W_F = 12\mu m$ and $L_F = 0.36\mu m$. W_F and L_F are effective width and length of single finger. N_F is the number of fingers. The parameters used for simulation are for 0.25μm CMOS process. Numerical calculations have been performed to evaluate the photovoltage generated due to optical illumination. The ion implanted channel profile in the active region of the device is assumed to be non-uniformly doped with Gaussian profile. The intrinsic and extrinsic capacitances are calculated considering bias dependence. The capacitances are calculated giving due thought to mobility effects due to vertical and lateral fields, velocity saturation, short-channel effects as channel-length modulation (CLM), source and drain charge-sharing and , reverse short channel effect (RSCE) as modelled in [10].The effect on substrate current due to impact ionization also has been accounted for. The capacitance investigation has been done for quiescent condition of V_{GS} varying from -0.5V to 3V, ensuring that it covers all the regions of MOSFET operation. The voltage V_{SB} is fixed at 0V and V_{DS} is at 0V and 1V under dark and optical illumination. The photon flux varies from 1x 10^{14} to 1x 10^{18} indicating change of optical power from 0.25mW onwards.

The direct illumination of the gate results in generation of excess electron hole pairs due to absorption of radiation in depletion region. The excess carriers generated cause change in gate voltage due to photo voltage, VOP as reported in [12].

Fig. 5 shows all the 16 intrinsic capacitance in dark condition for $V_{DS}=0V$, $V_{SB}=0$ and V_{GS} varying from -0.5 to 3V. The magnitude of the capacitances can be related with the corresponding charges and the terminal voltage associated .It can be seen that capacitances associated with substrate (bulk) terminal are significant in the region of V_{GS} from -0.5 to 0 which is essentially the accumulation of MOSFET, where Q_I is zero and Q_G is equal to Q_B. On other hand as the MOSFET begins to enter the inversion region, typically with $V_{GS} > 0.5V$, the charges associated with drain and source become dominant and this can be seen with drain and source

capacitance becoming important. These capacitances represent the effect on terminal charge due to applied external terminal voltages and hence cannot be interpreted simply as parallel plate capacitances. It can be seen that magnitude of *Cgdi, Cgsi ,Cgdi* and *Cdgi* is same. The numerical value of *Cbsi, Csbi, Cbdi* and *Cdbi* are identical. *Cdsi* is also equal to *Csdi* . Since at $V_{DS}=0$ and $V_{SB}=0V$, the drain, source and substrate voltages do not show nonreciprocal influence, and the transcapacitances are equal.
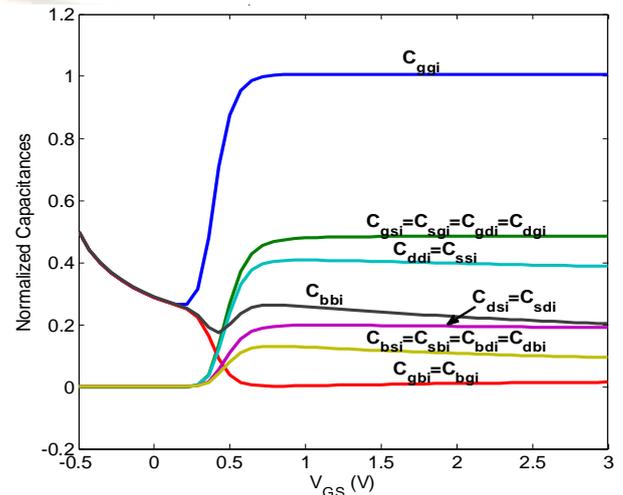

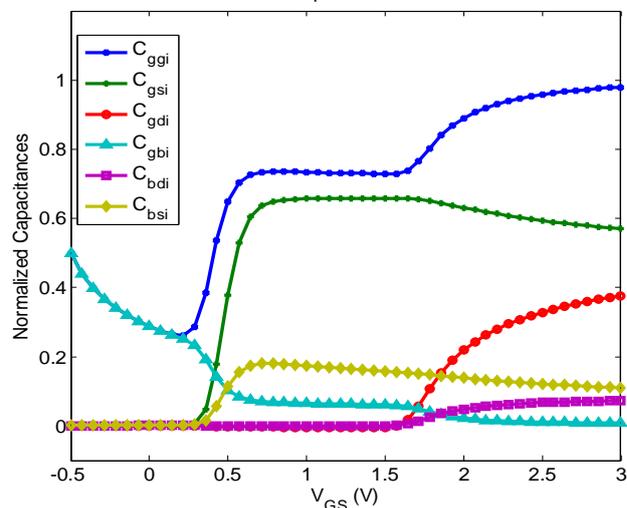Fig 5 Intrinsic Capacitances under dark condition at $V_{DS}=0V$ and varying V_{GS}.

Fig 6 Significant Intrinsic Capacitances with $V_{DS}=1V$ and varying V_{GS} under dark condition.

Fig. 6 indicates intrinsic capacitances at VDS=1V, VSB=0 V and VGS varying from -0.5 to 3V. The capacitances indicated are *Cgsi, Cgdi, Cgbi,Cbdi and Cbsi* are intrinsic capacitances which are associated with small signal model valid at low and medium frequency. The influence of applied voltage V_{DS} can be easily seen as it is the

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voltage which decides whether the MOSFET will be in saturation or non-saturation. In this view, the voltage V_{DS} has no effect on charges in accumulation and depletion region and hence the capacitances in those regions show no change as compared with $V_{DS}=0$. The capacitance *Cgsi, Cgdi* and *Cgbi* represent the effect of gate on source, drain and substrate terminal, but it is essential not to associate these capacitance parameters with any physical capacitor like structures. With applied voltage V_{DS}, the capacitance *Cgsi* is not same as *Cgdi* over the range of VGS. This is due to the fact that as MOSFET enters strong inversion region, the inversion layer ceases to be uniform and the source and drain depletion widths also become asymmetric. The source and drain charges are also influenced and charge partitioning has to be considered for accurate modelling. It can also be seen that capacitances *Cbdi* and *Cbsi* which are associated with the substrate region have no influence of gate voltage till V_{GS} exceeds 1.6V in spite of applied V_{DS}. This is because in presence of uniform inversion layer, the gate is protected from influence of substrate
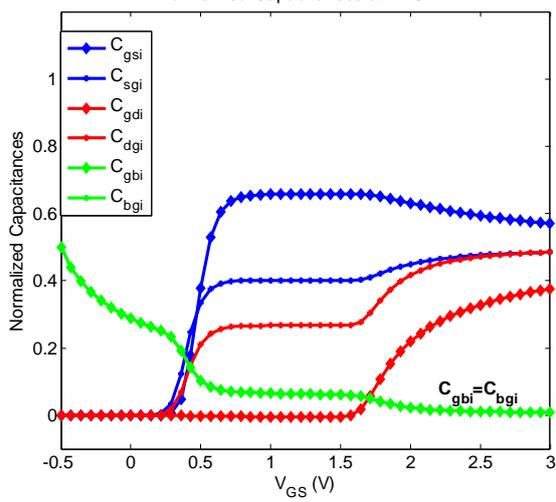
small value and the difference is almost zero, since effect on substrate charges is seen under varying bias which is essentially constant for MOSFET operation.
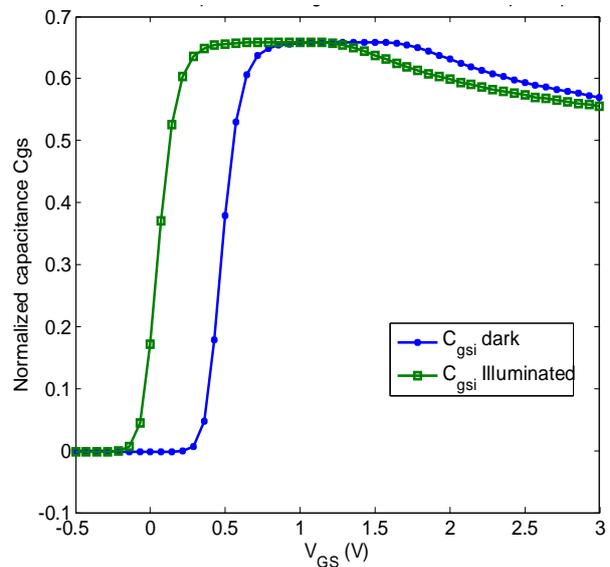

Fig 8 Intrinsic Capacitance *Cgsi* with V_{DS}=1V , varying V_{GS} under dark and with optical flux of 1x 10^{14}.

Fig 8 is the plot of capacitance Cgsi under dark condition and with optical illumination with optical flux of 1x 10^{14}. The capacitance *Cgsi* is the most important capacitance component of the small signal model as it is the one which affects transition frequency f_t. The transition frequency f_t determines the maximum limit at which the device operates satisfactorily. It is obvious from the plot that capacitance *Cgsi* with optical radiation has constant or lower magnitude for the region of operation. This is due to generated optical voltage which modifies the effective gate bias and hence the capacitance. This characteristic can be used to improve transition frequency f_t and also to control the device by an independent port.

Fig. 9 is the plot of the normalized transcapacitances under similar operating conditions and with optical flux of 1 x 10^{14}.It is important to note the scale of normalized transcapacitances, indicating that the transcapacitances are of lower magnitude than intrinsic capacitances. This is natural as the transcapacitances are the difference between intrinsic reciprocal capacitances. The transcapacitances under optical illumination have lower magnitude indicating better device performance at RF.

Fig. 10 shows total capacitance *Cgg* for a multifinger MOSFET device which that can be satisfactorily operated till frequency of 10 GHz. For the device model to work at RF, it is important to

Fig 7 Additional Intrinsic Capacitances Components with V_{DS}=1V and varying V_{GS} under dark condition.

The small signal model for RF frequency till 10 GHz consists of capacitive components indicated in Fig. 6 and the additional components in Fig. 7. As shown the capacitance *Cgsi* is not the same as *Cgdi* over the range of V_{GS}. The capacitance *Cgsi* represents the capacitive effect of source on gate and *Csgi* represents capacitive effect of gate on source. This is applicable to *Cgdi* and *Cdgi* also. This is as the capacitances *Cdgi* and *Csgi* have additional conductive components and differential capacitive components associated with them in the small signal model which is valid at high or RF frequency. These differential components are known as transcapacitances and have relationship as indicated in (13). The *Cgbi* and *Cbgi* have a very

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include intrinsic and then extrinsic component. The capacitance Cgg is the sum of extrinsic and intrinsic components of $Cgst$, $Cgdt$, and $Cgbt$. The magnitude of Cgg is almost equal to the oxide capacitance at $V_{DS}=0V$, but reduces when $V_{DS}=1V$. Under optical illumination, the nature of the curve remains the same, and these characteristics can be used to control the region of device operation.
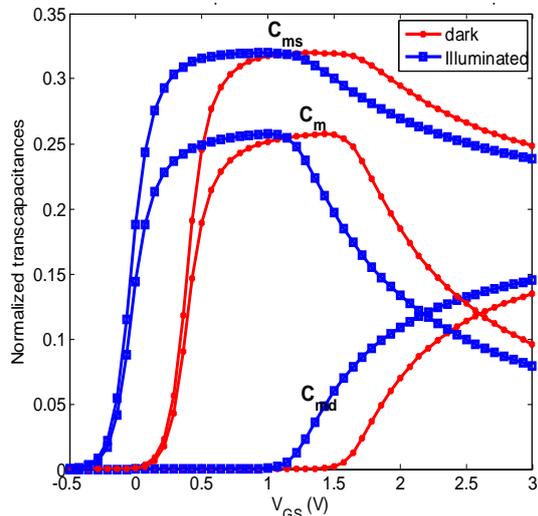

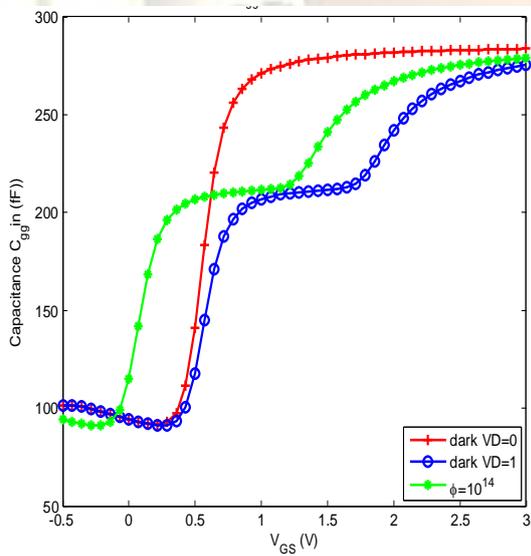Fig 9 Normalized transcapacitances with $V_{DS}=1V$, varying V_{GS} under dark and with optical flux of 1 x 10^{14}

Fig 10 Total Capacitance Cgg with varying V_{GS} and V_{DS} under dark and with optical flux of 1 x 10^{14}.

Fig. 11 shows the distribution of capacitive components of capacitance $Cgst$ under dark condition at $V_{DS}=0V$, $V_{DS}=1V$ in dark and with optical flux of $1x10^{14}$. The plot indicates total capacitance $Cgst$ and $Cgsi$, the intrinsic component.. The graph indicates that extrinsic component of capacitance plays a major role when

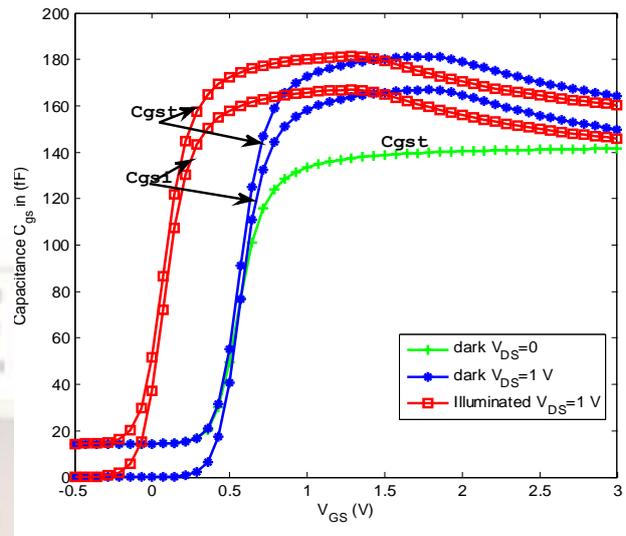the device is in depletion or inversion region with applied nonzero V_{DS}.

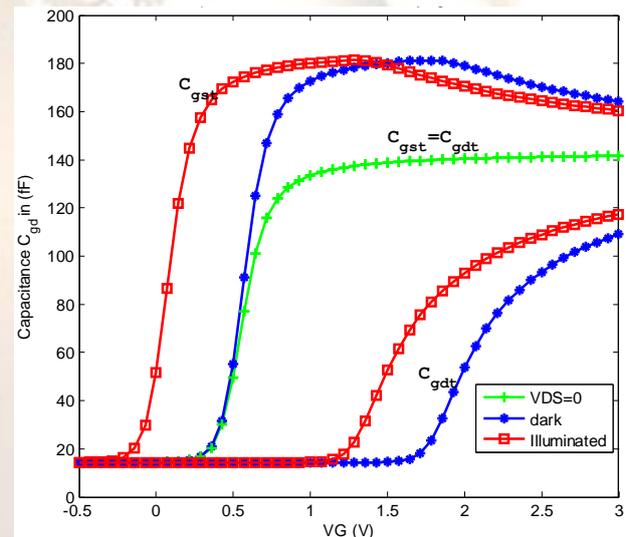Fig 11 Capacitance $Cgst$ and $Cgsi$ under dark and Illumination.

Fig 12 Total capacitances $Cgst$ and $Cgdt$ under dark and illumination.

Fig. 12 displays analysis of total capacitances $Cgst$ and $Cgdt$ which are major components for the small signal model. The plot confirms with the previous results indicating that capacitance $Cgst$ is equal to $Cgdt$ at $V_{DS}=0V$. The capacitance $Cgdt$ drops significantly in non-saturation region, where the drain overlap capacitance becomes dominant. Under optical illumination, the capacitance $Cgdt$ increases, which is undesirable, but since overall $Cgdt$ reduces to a small value, hence effect on the performance of OG-MOSFET can be neglected. The capacitance $Cgst$ is seen to fall under optical illumination which aids in improving frequency range of operation.

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Fig. 13 shows variation of total capacitance *Cgst* with varying optical flux of 1×10^{14} to 1×10^{18} at quiescent condition of V_{GS}=1.5V, V_{DS}= 1V and V_{SB}=0V . The capacitance *Cgst* is found to reduce under influence of increasing optical power. This is due to increase in channel conductivity and hence increase in inversion charge with bias V_{GS} remaining constant. This reduces the capacitance *Cgst* which is likely to enhance device performance and offer better control.
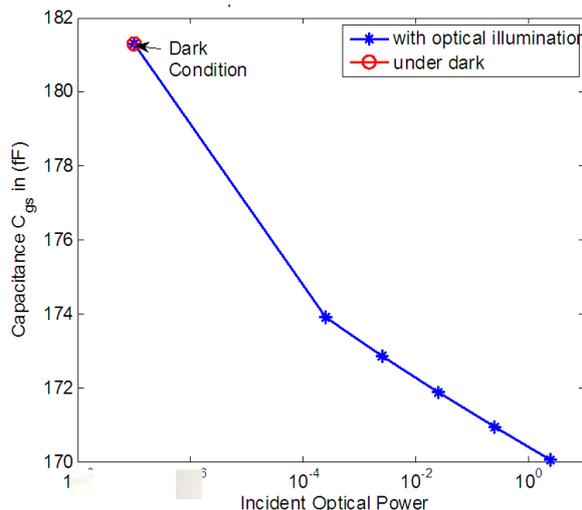

Fig 13 Capacitance *Cgst* under dark and with varying optical flux of 1×10^{14} to 1×10^{18}

V. CONCLUSION

Theoretical investigations have been done on extrinsic and intrinsic capacitances of the MOSFET considering the bias variations. A detailed analysis for the capacitances which are vital for the small signal model has been done on an MIS device, modified to optically gated MOSFET. The frequency range extended from DC to RF. The increase in the photon flux density results in reduction in potential differences between the channel potential minimum and the source potential. The reduction in total capacitance *Cgs* indicates improvement in performance at RF. This ensures the device application for optoelectronic applications like photo-detection,optical switching and imaging. Modification in device composition, structure and materials may find more areas of application.

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