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High Speed & Dynamic Swtiching Type Signal Generation For FPGA for Emulating Test Signal for Navigation Receiver

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Abstract

playing an important role in navigation test, radio navigation generator widely used in the people/military plane. But traditional equipment composed of analog circuit present low accuracy and poor reliability. A new kind of digital navigation signal generator is designed in this paper. It receives data and communication from PC by Micro Blaze embedded soft processor of Xilinx company and demodulated information to control FPGA load different software to generate various navigation signals, which fully meets general radio navigation system test technical requirement by giving full play to the system hardware and software advantages and fulfilling design targets such as the accuracy, flexibility and expansibility. Therefore, providing a new idea for radio navigation system design and test, this generator can be widely applied to debugging use on people/military plane radio navigation.

Keywords—Micro blaze, FPGA Navigation, DDS Signal Generator

I. INTRODUCTION

In modem aviation, navigation is an important technology. So far, equipped in almost all the military and civil airports, radio navigation system is the most widely used navigation devices in aviation. At present, radio navigation still has priority in short-range navigation of civilian and military aviation in our country. Also, due to the imperfect landing system device in the existing aircraft, radio navigation system is of vital importance in ensuring safety in plane's homing and approaching.

In the actual navigation test, to simulate the RF signal of combined antenna in radio navigation, various signal generators are often designed to satisfy performance of navigation system and meet technical requirements. Meanwhile, the signal generator must adjust signal types, parameters and work modes timely according to the navigation system requirements. Therefore, signal generator must have the feature that signal can be generated flexibly, parameters change quickly, signal spectrum stay stabilized, and the system is reliable, etc. The proposed system adopts Micro Blaze soft processor as the control core of generator to communicating command with PC. which can satisfy each requirement in actual application of testing and debugging on navigation.The important role in navigation test, radio navigation generator is widely used in the people/military plane. But traditional equipment composed of analog circuit Presents low accuracy and poor reliability. A new kind of digital navigation signal generator is designed. It receives data and commands from PC by MicroBlaze embedded soft processor of Xilinx company and demodulates information to control FPGA load different software to generate various navigation signals, which fully meets general radio navigation system test technical requirements by giving full play to the system hardware and software advantages and fulfilling design targets such as the accuracy, flexibility and expansibility. Therefore, providing a new idea for radio navigation system. this generator can be widely applied to debugging use on people/military plane radio navigation.

The reference paper implements only AM modulation type for testing the navigational receivers.

1. But today's communication systems use variety of latest digital modulation techniques, hence we have developed two architectures one for analog and other for digital modulations in this project.
2. For realizing the digital modulation we have used Universal digital modulator for generating all type of digital modulated signals.
3. Signal generator will be designed that contains feature that signal can be generating flexibly, parameters change quickly, signal spectrum stay stability, and the system is reliable, etc.
4. Fundamentally, characteristics of signal patterns and real-time variability are mainly embodied in signal generation technology.
5. This system adopts MicroBlaze soft processor as the control core for generating communicating command with PC and controlling FPGA load different

II BLOCK DAIGRAM

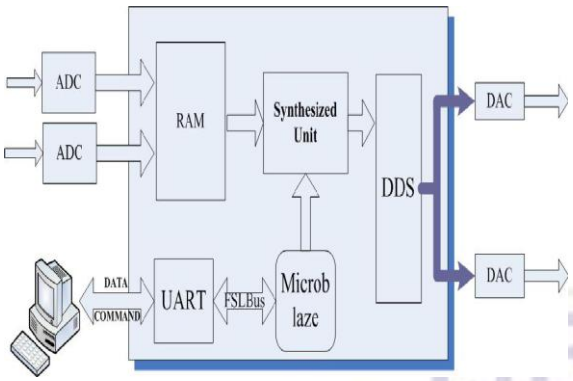


Figure 1 processing module for FPGA

The figure1 block diagram consist of sub module as

1. ADC: For converting analog signal to digital signal
2. RAM: For storing digital values
3. UART: serial cable interface for communication purpose
4. Micro blaze: It is a processor used for giving the commands
5. Synthesized Unit: it is used for selecting modulation technique
6. DDS: it is used to generate carrier signal
7. DAC: to convert the digital signal to analog signal

III DESIGN SCHEME OF DIGITAL SIGNAL GENERATOR OF RADIO NAVIGATION:

According to different technical requirements of navigation, the generated signal is basically formed by the carrier signal, low frequency modulated signal and audio modulated signal. Therefore, in this scheme, the signal generator adopts direct digital frequency synthesizer (DDS) technology to design precise clock reference source, word length of frequency and phase accumulator and sine function table to generate the modulated sine signal whose frequency variation scope, step length change and precision meet the acquirements in overall design. Large-scaled FPGA is used in this system to realize accurate DDS , ADC converter is used to convert the external signal to be modulated by carrier signal, and the soft embedded processor MicroBlaze communicates with PC by RS422/232 as the control core, figure 1 is the overall scheme of digital signal generator of radio navigation. The control software of PC wrote in VC6.0 communicates with the generator through RS422/232 is in charge of transmitting control command to set frequency, azimuth angle, channel, working mode and other parameters of navigation signal and receiving status and data of the generator after every change. In this system, as a master unit MicroBlaze sends parameters to FPGA after demodulating data from PC while FPGA generates accurate navigation signal to high-speed DAC converter as the ground floor synthesis unit. Meanwhile, multiple clock signals used in the system are generated in phase lock logic part of FPGA from external oscillator.

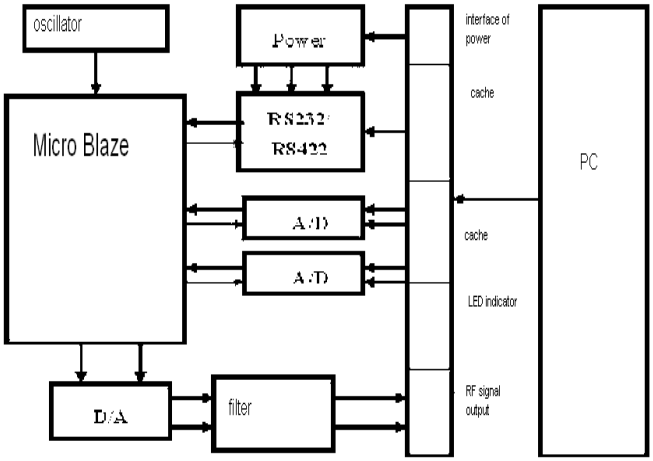


Figure 2 Block Diagram of FPGA

Direct Digital Synthesizer*:*

A Direct Digital frequency Synthesizer (DDS) design and prototype suitable for space-borne applications is presented. The design is targeted for use in the uplink section of the RF subsystem of the New Horizons Pluto spacecraft currently under design at APL. Design and analysis of the digital portion of the DDS is presented along with experimental data from the prototype system, which was implemented using an FPGA and a discrete digital to analog converter.

Direct Digital frequency Synthesizers (DDS) are a common component in a variety of communication systems, especially those requiring fast frequency hopping, low power dissipation, and small form factor.

A DDS at its simplest is a clock-dividing counter, termed the phase accumulator, which generates a digitized ramp waveform. This ramp is converted to a sine-wave representation and subsequently translated to the analog domain by a digital to analog converter (DAC). Subsequent filtering of the DAC output can be used to remove the high frequency components that arise from the data conversion process. Fig. 1 illustrates the conceptual system with a j-bit accumulator output truncated to a k-bit ROM address space and a m-bit DAC.DDS performance is measured in a number of ways. Some are fairly generic, including power dissipation and maximum nput clock rate and output frequency. Others are more specific, relating to minimum frequency step size and to the spectral purity of the DDS output. The DDS output spectrum reflects the fact that a DDS effectively samples a sine wave output. As a result, inaccuracies due to

finite word length effects as well as Nyquist sampling considerations cause the output spectrum to contain energy at frequencies other than the fundamental. These peaks, termed spurs, determine the signal to noise level of the DDS, which is defined as the Spurious Free Dynamic Range (SFDR). Non-idealities in the DAC can further degrade the SFDR as well. In general, peaks which are closer in frequency to the fundamental present more problems than peaks further out, simply because they are more difficult to attenuate with an output lowpass filter.

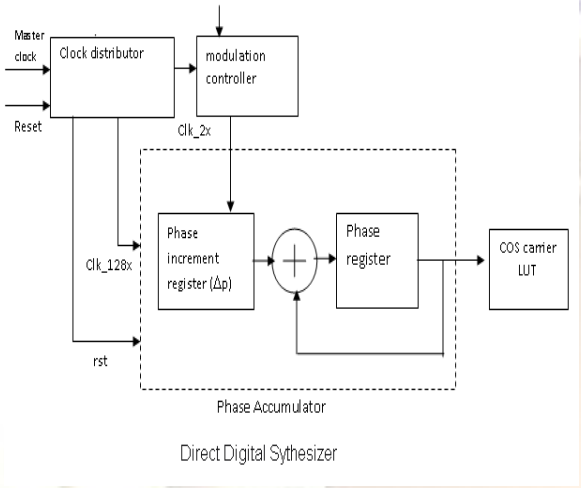


Figure 3 Direct Digital Sythesizer

Implementation of DDS

In this figure 3we are using Direct Digital Synthesizer for generation of the carrier signal. All we know about that by using DDS we can generate a carrier signal in the form of sine or cosine or sine cosine. Xilinx itself generate the core for DDS that is ip core generation. In that we should select options about the carrier or signal frequency in MHZ and phase off set and data width and the phase increment register data width depends on the data width or we can have a option like programmable then we can give the phase of set and frequency levels through the program. And we are taking the carrier signal from the DDS and we do the modulation like AM, FM, QPSK, BPSK. And in FM technique we are taking DDS signal as the message signal and we are generating the carrier by using the Hardware Description Language.

ADC

The Analog to Digital Module Converter Board (the AD1™) converts signals at a maximum sampling rate of one million samples per second, fast enough for the most demanding audio applications. The AD1 uses a 6-pin header connector, and at less than one square inch is small enough to be located at the signal source.

1.Features include:

- Two ADCS7476MSPS 12-bit A/D converter chips
- a 6-pin header connector
- a 6-pin connector
- two 2-pole Sallen-Key anti-alias filters
- two simultaneous A/D conversion channels at up to one MSa per channel
- very low power consumption
- small form factor (0.95" x 0.80").

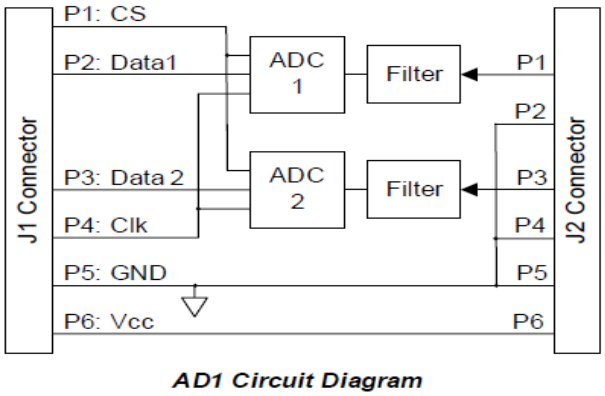


Figure 4 ADC block diagram

2. Functional Description

The figure 4 AD1 converts an analog input signal ranging from 0-3.3 volts to a 12-bit digital value in the range 0 to 4095. The AD1 has two simultaneous A/D conversion channels, each with a 12-bit converter and filter. Each channel can sample a separate stream of analog signals. The AD1 can also convert a single stream of analog signals using only one channel. Each channel has two 2-pole Sallen-Key antialias filters with poles set to 500 KHz. The filters limit the analog signal bandwidth to a frequency range suitable to the sample rate of the converter. The AD1 uses the SPI/MICROWIRE™ serial bus standard to send converted data to the host system. The serial bus can run at up to 20 MHz. The AD1 has a 6-pin header and a 6-pin connector for easy connection to a Digilent system board or other Digilent products. Some system boards, like the Digilent Pegasus board, have a 6-pin header that can connect to the AD1 with a 6-pin cable. To connect the AD1 to other Digilent system boards, a Digilent Modular Interface Board (MIB) and a 6-pin cable may be needed. The MIB plugs into the system board, and the cable connects the MIB to the AD1. The AD1 can be powered by voltage from either a Digilent system board or an outside device. Damage can result if power is supplied from both sources or if the outside device supplies more than 3V.

DAC

The Digilent PmodDA2 Digital to Analog Module Converter, converts signals from digital values to analog voltages on two channels

simultaneously with twelve bits of resolution. The PmodDA2 uses a 6 pin header connector and, at less than one square inch, is small enough to be located where the reconstructed signal is required.

1.Features include:

- Two National Semiconductor DAC121S101, 12-bit D/A converters
- a 6-pin header and 6-pin connector
- Two simultaneous D/A conversion channels
- very low power consumption
- small form factor (0.80" x 0.80").

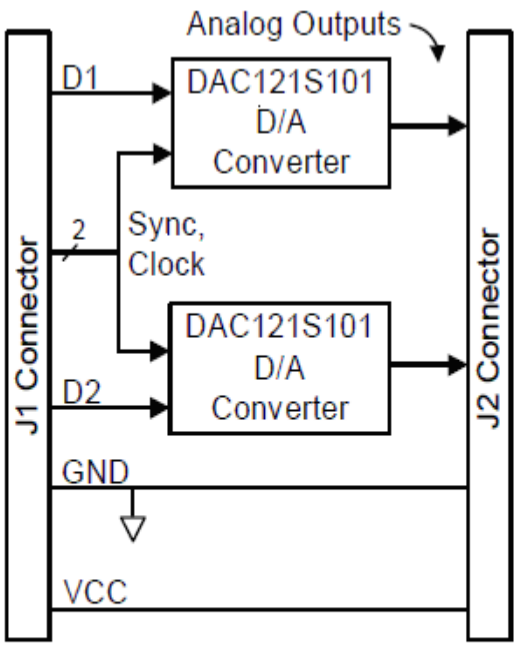


Figure 7
Block Diagram

Figure 5 DAC Block diagram

The PmodDA2 can produce an analog output ranging from 0-3.3 volts when operated with a 3.3V power supply. It has two simultaneous D/A conversion channels, each with a 12-bit converter that can process separate digital signals. The PmodDA2 is equipped with two DAC121S101 digital to analog converters. Sending commands via the SPI/MICROWIRE™ serial bus to the D/A converters produces outputs. The two converters are connected in parallel so that commands are sent to both converters simultaneously. The PmodDA2 is designed to work with either Digilent programmable logic system boards or embedded control system boards. Most Digilent system boards, such as the Nexys, Basys, or Cerebot, have 6-pin connectors that allow the PmodDA2 to plug directly into the system board or to connect via a Digilent six-wire cable Some older Digilent boards may need a Digilent Module Interface Board (MIB) and a 6- pin cable to connect to the PmodDA2. The MIB plugs into the system board and the cable connects the MIB to the PmodDA2.

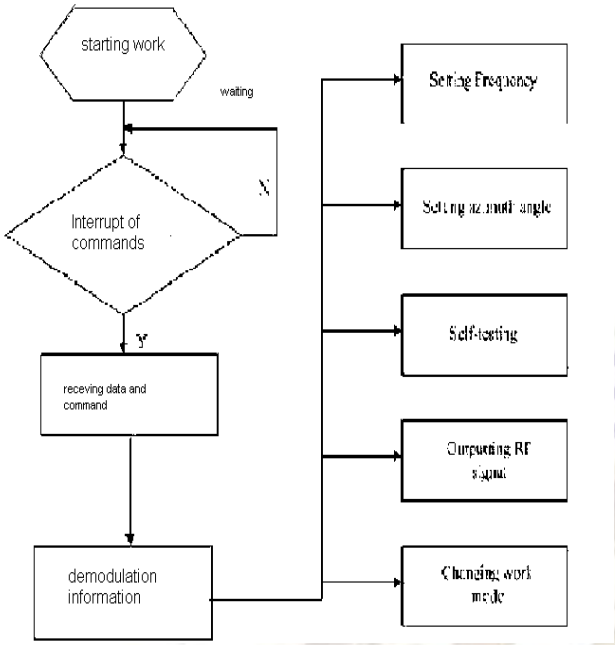
See Table 1 for a description of the signals on the interface connectors J1 and J2.

Table 1: Interface Connector Signal Descriptions

Digital Interface – J1	
1	SYNC (common)
2	DINA (converter IC1)
3	DINB (converter IC2)
4	SCLK (common)
5	GND
6	VCC
Analog Interface – J2	
1	VOUTA (converter IC1)
2	N/C
3	VOUTB (converter IC2)
4	N/C
5	GND
6	VCC

The PmodDA2 is usually powered from the Digilent system board connected to it. The power and ground connections are on pins five and six of the digital interface connector J1. Alternatively, the PmodDA2 can be powered from an external power supply provided through pins five and six of the analog interface connector J2. In this case the power select jumper on the system board should be set to disconnect power from the system board to J1. Damage may result if two power supplies are connected at the same time. The Digilent convention is to provide 3.3V to power Pmod modules. The PmodDA2 can be operated at any power supply voltage between 2.7V and 5.5V, however caution should be exercised if using any voltage greater than 3.3V, as damage to the Digilent system board could result.

MicroBlaze



This MicroBlaze part is used for giving the command to PC and selecting the modulation technique.

Implementation of Microblaze:

In our project the Microblaze place a main important role. It is a soft core processor. and we know about the two type processors, those are Micrblaze and the Power Pc. The main difference between the microblaze and power pc is ,microblaze is a soft core processor and the power pc is a hard core processor.

Microblaze: Which is a soft core processor, the some part of the fpga will acts as a microblaze processor by implementing the hardware description language means by the vhdl code we are making act of some part of fpga as microblaze. So it is called as soft core processor. No need of any external hardware circuitry.

Power Pc: It is hard core processor, means it is different than microblaze. In this we should require the external hardware by connecting this external hardware of the power pc to the fpga we can use the processor. Then the circuit complexity may increase.

So in this project we are implementing Microblaze soft core processor only. And this processor will take the information from the Pc by using UART. So from the we receive the commands in hexa,ascii format. By using these commands only we can change our parameters of modulation techniques like setting frequency ,setting azimuth angle, changing work mode, self testing and output RF signal. This function we will implementing by coding. According to these commands the modulation techniques are select in the synthesized unit.

IV SIMULATION RESULTS

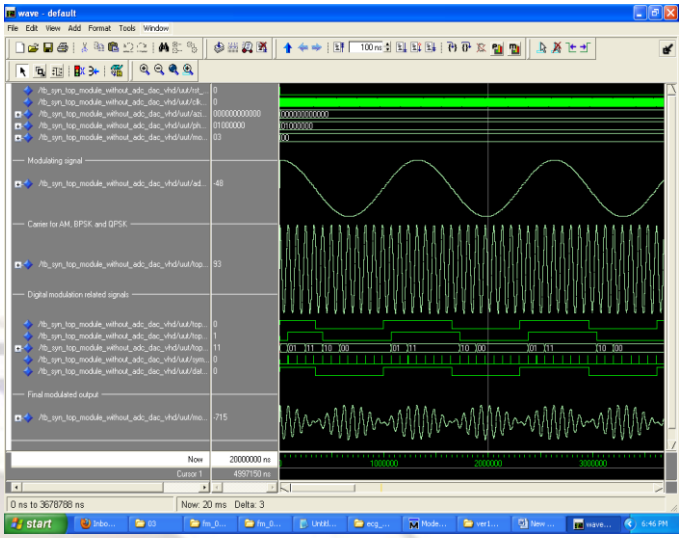


Figure 6 simulation of AM

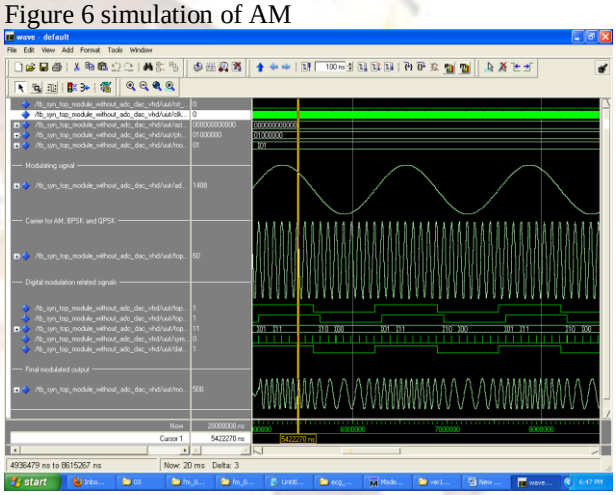


Figure 7 simulation of Fm

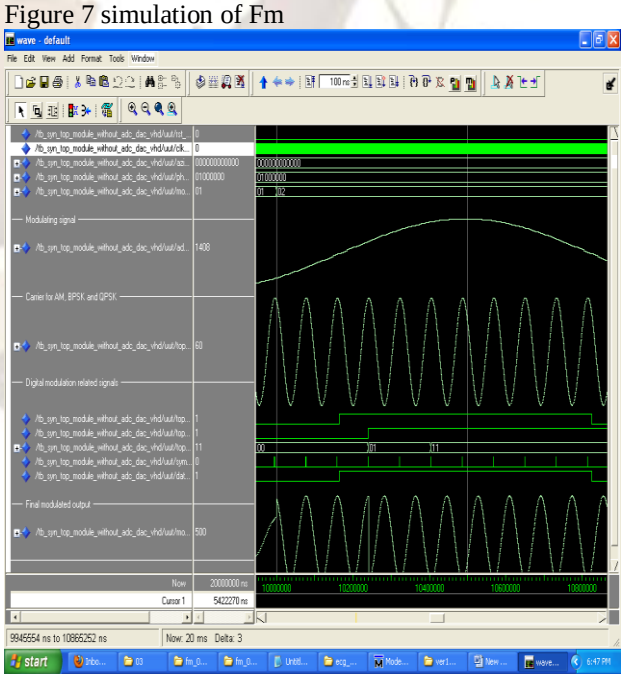


Figure 8 simulation of BPSK

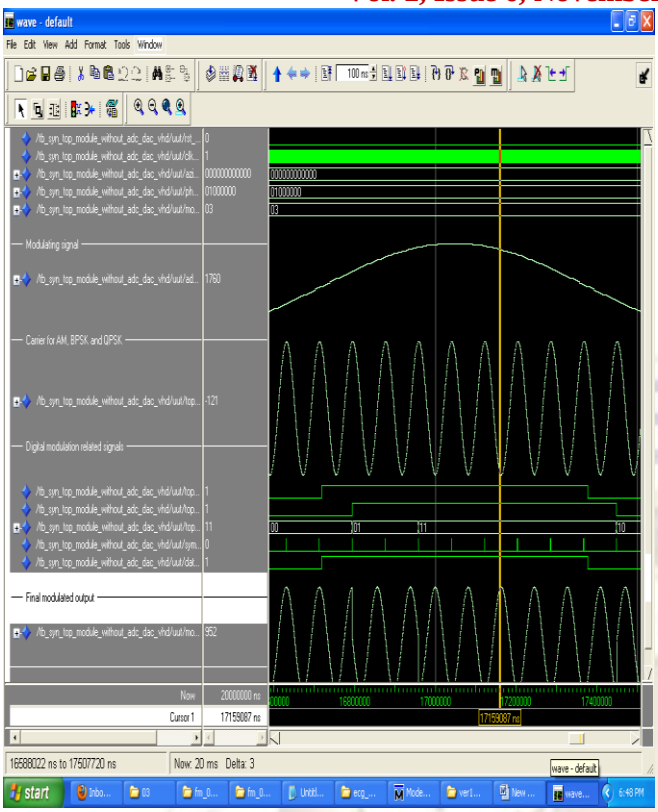


Figure 9 simulation of QPSK

IV CONCLUSIONS

In this paper, the digital signal generator of radio navigation is implemented by soft processor MicroBlaze whose key portion is achieved in a single FPGA chip, which overcomes the disadvantage of low accuracy and flat tuning in traditional methods. Simultaneously, various kinds of signals can be loaded in this system, obtaining more flexibility and better expandability. AM,FM,BPSK,QPSK modulation technique has being done . Through the numerical test and simulation results, the veracity and precision is confirmed. Favorable result has been acquired in practical application.

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