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Low Power- HTSCR and CMOS Structure for On-chip ESD Protection and Performance Comparison

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Abstract

Low power ESD protection circuits are implemented in 0.13µm technology [2,7]. This is confirmed by transient ESD simulation under varying condition of temperature and case sensitivity; the results converge to a low power on chip ESD protection based on the comparison of performance.

Index terms: Electrostatic discharge (ESD), Human Body Model (HBM), High triggered SCR (HTSCR), Total power dissipation (TPD), Salicide diffusion.

1. Introduction

Different technology have been introduced to implement ESD protection circuits on chip or off chip with a progression of advancement in performance over the previous ones [1,2,4]. These are not area specific that's why it is always beneficial to protect IC or chip with such technologies. Ironically, high performance computing system characterized by large power dissipation also drives the low power needs. Another major demand for low power chips and systems comes from environmental concerns. Here, different types of ESD protection circuits are shown with power down mode and their performance comparison in case of HBM [3,6].

HBM: According to the industry standards, ESD robustness requires the protection device to be able to block a minimum HBM ESD event of 2KV with a typical decay time of 150ns [2].

2. Types of ESD protection circuits:-

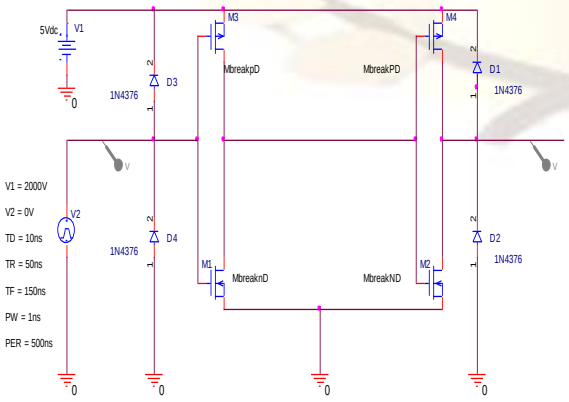


Fig.1 (a) ESD diode protection circuit.

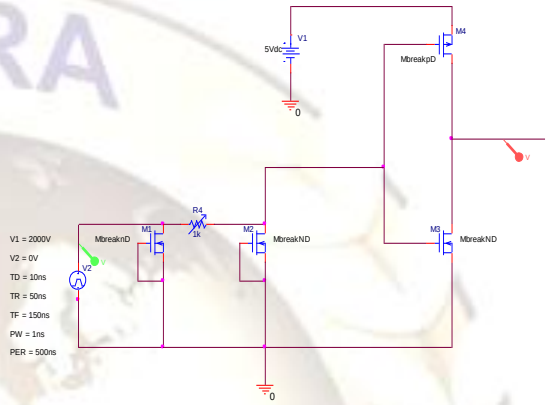


Fig.1 (b) Combination Resistor/ Transistor rotection.

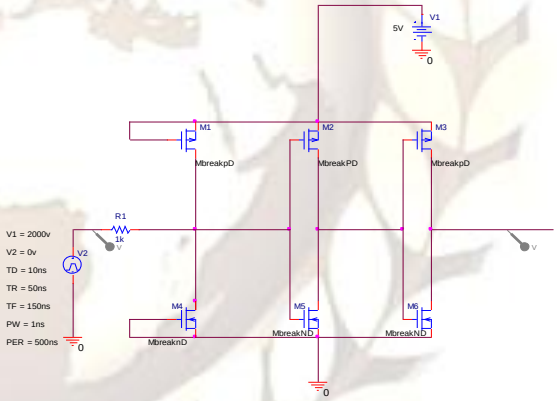


Fig.1 (c) CMOS ESD protection circuit.

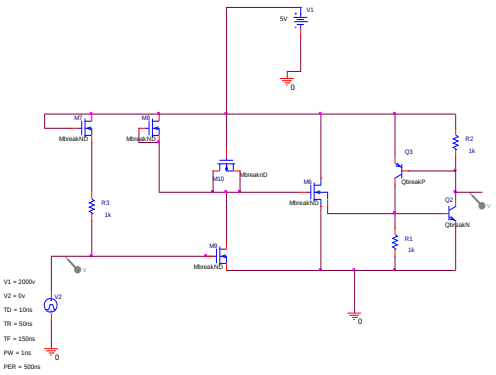


Fig.1 (d) ESD protection circuit using HTSCR.

3. Input ESD pulse for above circuits in HBM case: (Input ESD pulse Parametersare according to the industrial specifications) [2].

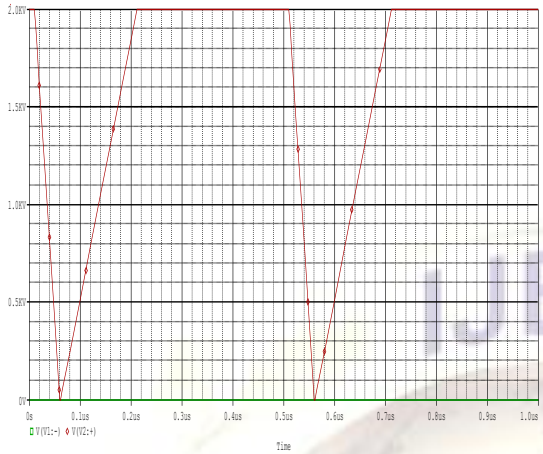


Fig.2. Input ESD waveform.

4. Transient Analysis with Case Sensitivity/ Worst Case at Temperature (Sweep): 27^{0}C, 45^{0}C, 70^{0}C, 100^{0}C, 250^{0}C.

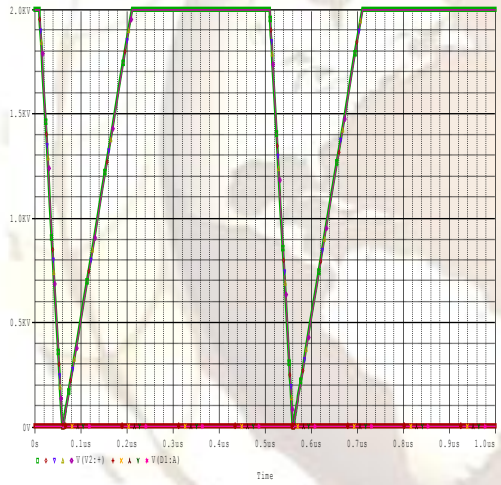


Fig. 3 (a) Simulation result for Fig. 1 (a).

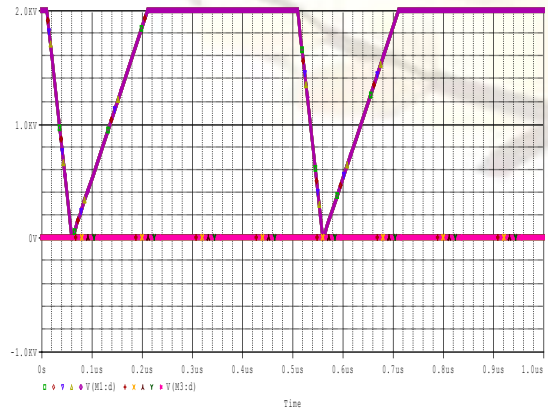


Fig. 3 (b) Simulation result for Fig.1 (b).

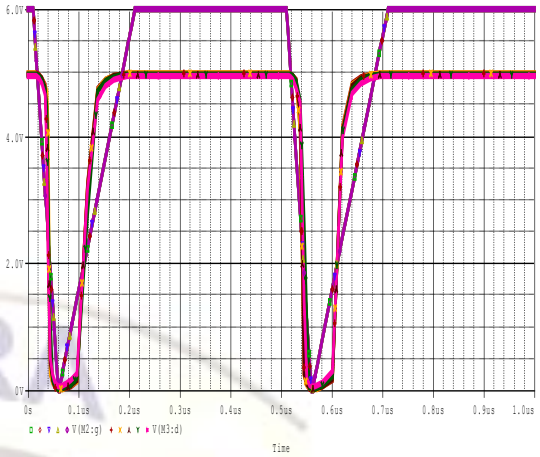


Fig. 3 (c) Simulation result for Fig. 1 (c)

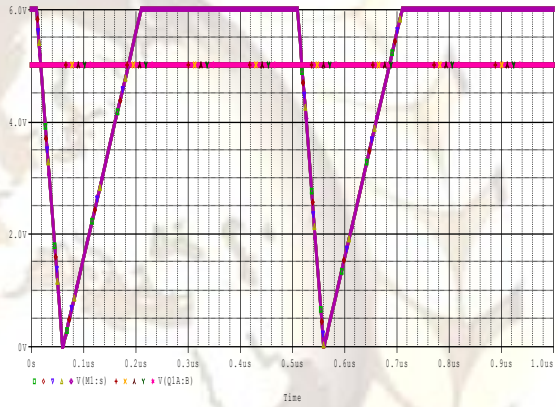
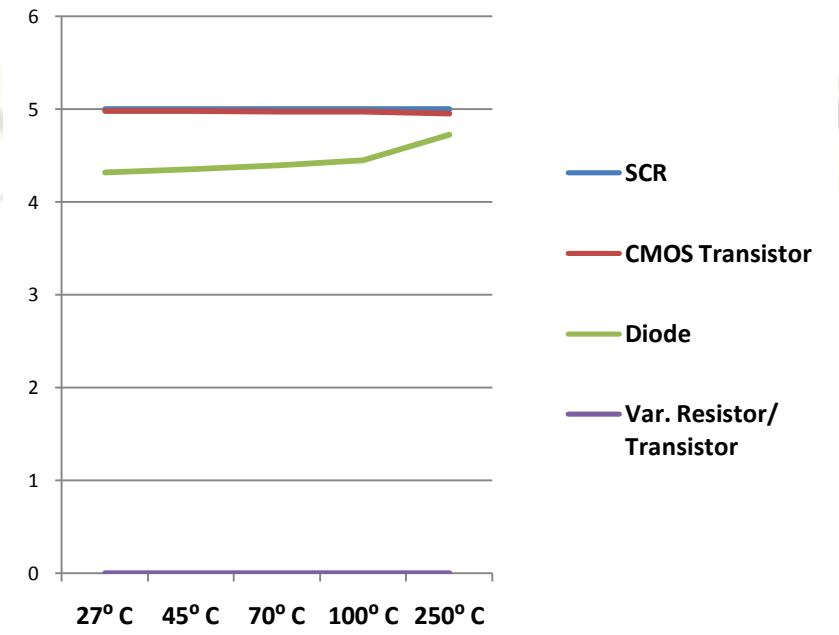


Fig. 3 (d) Simulation result for Fig. 1 (d)

Circuit Type	At 27° Celsius	At 45° Celsius	At 70° Celsius	At 100° Celsius	At 250° Celsius	TPD (W)	Impact due to increase in temp.
Diode	4.9809V/2 KV	4.9790 V/2KV	4.9762 V /2KV	4.9726V/ 2KV	4.9326V/2 KV	1.20E-01	O/P Voltage Decrease
Var. resistor & Tr an- - sistor	(1.223E-9)/ 2KV	(1.36E-09)/ 2KV	(2.488 E-09)/ 2KV	(31.70E-09)/ 2KV	0.0026 / 2KV	2.89E+03	O/P Voltage Decrease
CMOS	4-9809V /2KV	4-9791V /2KV	4-9763V / 2KV	4-9728V / 2KV	4-9485V / 2KV	2.08E+04	O/P Voltage Decrease
SCR	5.0V / 2KV	5.0V / 2KV	5.0V / 2KV	5.0V / 2KV	5.0V /2KV	2.08E+04	O/P Voltage Constant

5. Table I. Comparison of ESD performance among HTSCR, CMOS, Var. resistor/ Transistor, Diode protection circuits:

6. Graph I. on the basis of above table:



7. Conclusion:

Graph I. shows that ESD protection circuit using SCR gives better output stability over others by increasing the sustainability of the Integrated Circuits (ICs) on higher temperature.

From above it is clear that ESD protection circuit using CMOS, clamps higher voltage than a SCR but is not so fast to detect ESD transient pulse, this is owing to lower ON resistance of SCR and a more uniform distribution of electric field of the device [7]. The SCR also works with salicided diffusions [6]. In terms of stability, CMOS does not bestow stable o/p as temperature increases gradually.

8. Low Power ESD protection circuits (CMOS and HTSCR):

8. (a) Power consumption for circuit shown in Fig.1 (c):

Fig.4 (a)

8.(b) Power consumption for circuit shown in Fig.1 (d):

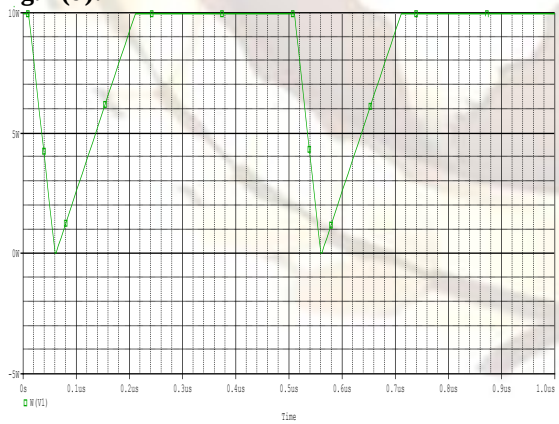


Fig.4 (b)

From the equation of power dissipation:

$P = C_L V^2 f$ ……. (I)

i. The capacitance C_L is constant.
ii. The voltage V is constant.
iii. Clock frequency f.

Assuming that in the above power equation the operating frequency for both the circuits is same and also the size of the ESD Clamp protection circuit is same, then the parasitic capacitance of the metal layer is 1fF/μm^2 [5]**.** To, turn these circuits with power down mode, supply Voltage. 1.2V is the optimum voltage at which these circuits may operate satisfactorily.

8.(c) CMOS ESD protection circuit at supply voltage 1.2V

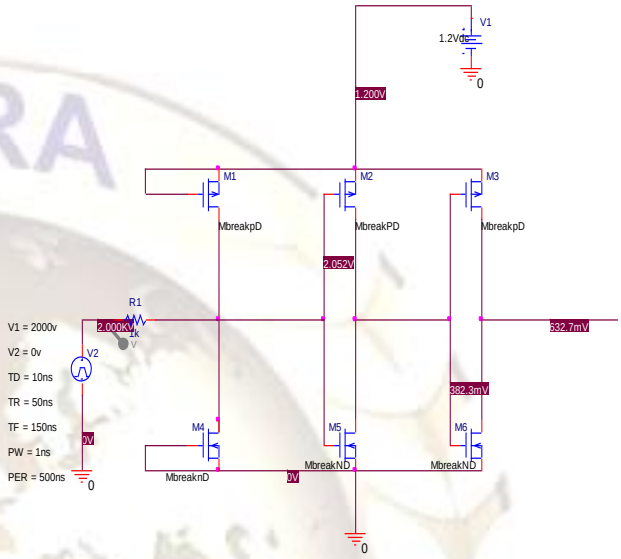


Fig.5 (a)

Power Consumption at 1.2V:

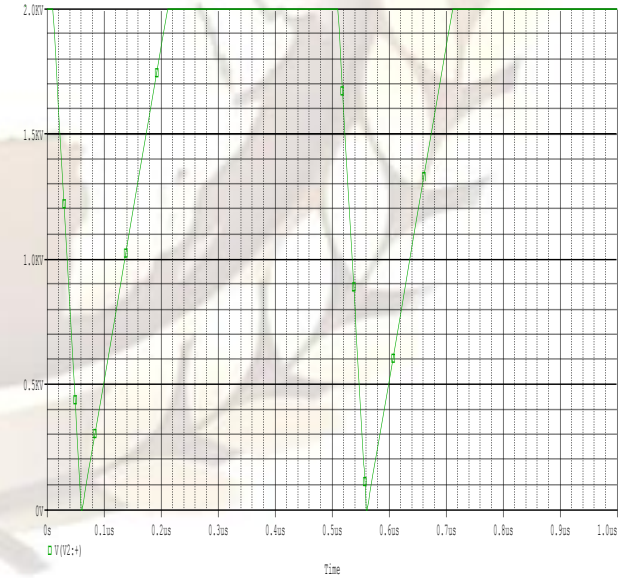
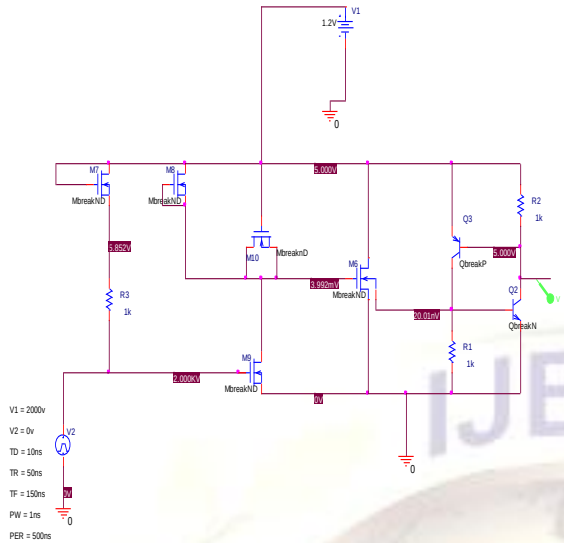


Fig.5 (b)

8.(d) SCR ESD protection circuit at supply voltage 1.2V



ig.5 (c)

Power consumption at 1.2V:

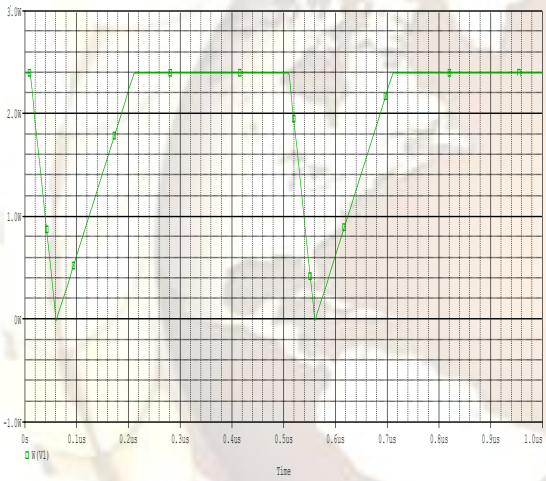


Fig.5 (d)

9. Table II. Power consumption

Circuit Type	At 5V	At 1.2V	
		At low trigger edge	At high trigger edge
CMOS	9.969 W	16.309 mW	2.3973 W
HTSCR	9.969 W	6.4970 mW	2.3973 W

Conclusion

This paper has described the methodology for low power CMOS and HTSCR ESD protection circuit and their performance comparison. Spice simulation was used to verify the results. From the above we have deduced 75.95% reduction in power consumption for the SCR circuit by reducing the voltage from 5V to 1.2V. Similarly, if we compare the above with CMOS, we have 60.16% reduction in power consumption at the lower trigger edge of the pulse. Low power ESD protection circuits simulation with analysis has been demonstrated in this work.

Reference:

[1] G. Langguth, C. Russ, W. Soldner, B.Stein, H. Gossner, "ESD Challenge in Advanced CMOS Systems on Chip" 978-1-4244-5775-0/2010IEEE.

[2] Ming-Dou Ker, Wan-Yen Lin, Cheng-Cheng Yen, Che-Ming Yang, Tung-yang Chen, Shih-Fan Chen, "On-Chip ESD Detection Circuits for System-Level ESD Protection Design" 978-1-4244- 5798-4/10/2010IEEE.

[3] Rafael Fried, Yaron Blecher and Shimon. Friedman "CMOS ESD Protection Structures... Characteristics and Performance comparison"0-7803-2647- 4/951/1995 IEEE.

[4] Stephen G. Beebe "CHARACTERIZATION, MODELING, AND DESIGN OF ESD PROTECTION CIRCUITS."

[5] Yang Chen and Ming-Dou Ker "Design on ESD Protection Circuit with Very Low and Constant Input Capacitance" Tung- 0-7695-1025-6/ 2001 IEEE.

[6] H. Feng, R. Zhan, Q. Wu, G. Chen and A.Z. Wang "RC-SCR: verv-low-voltage ESD protection circuit in plain CMOS" *ELECTRONICS LETTERS* 12th *September* 2002 Vol. 38 No. 79.

[7] ***F***. Ma, Y. Han, S. Dong, B. Song, M.Miao and K. Zhu "Investigation of boundary-MOS-triggered SCR structures for on-chip ESD protection" ELECTRONICS LETTERS 17th February 2011 Vol. 47 No. 4.