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An Algorithm for FPGA based Implementation of Variable Precision MAC unit for High Performance Digital FIR Filters

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ABSTRACT

The MAC Unit plays an important role in DSP applications. When implemented on FPGA, many MAC Units can be implemented on a single FPGA flexible to different design architectures. Hence the need of efficient MAC Units arises for filter applications. This paper discusses about variable precision based MAC Unit implemented on FPGA at algorithmic level. The proposed algorithm for FIR Filters is high performance and area efficient than the conventional MAC Unit. The delay for VP MAC Unit is reduced nearly by 60% than the conventional MAC Unit.

Keywords – ASIC, FIR Filter, FPGA, MAC Unit, Variable Precision.

I. INTRODUCTION

The design of High Performance Digital Filtering algorithms with is a typical challenge for most of the designers [1]. As it requires high sampling rate, implemented with less cost, which is flexible to adopt for different designs or structures and is fabricated for different technologies using same or similar process. The variable precision can be used for implementing MAC Unit.

The Common approaches to the implementation of digital filtering algorithms are general purpose Digital Signal Processing Chips for audio applications, special purpose Digital Filtering chips, Application Specific Integrated Circuits (ASICs) for higher rates and Field Programmable Gate Arrays (FPGAs).

The Several widely used general purpose digital processing chips for audio applications are Digital signal processors (ASICs) such as the Texas Instruments TMS320, Motorola 56000 and Analog Devices ADSP-2100 families designed to efficiently implement filtering operations at audio rates. These have a disadvantage of limited performance. To overcome this, use High performance designs for filtering at sampling rates above 100 MHz for specific application domain using CMOS and BiCMOS technologies, using approaches ranging from full custom to traditional factory-configured gate arrays.

The custom based designs are often well suited only for use in a particular application, and cannot be easily reconfigured for other operations even within that same domain. So the lack of flexibility or adaptability in the custom approach but it does promise the best performance and efficiency for the specific application for which a particular design is intended. Also these do not allow the function of a device to be modified within the system, for purposes such as correcting faults. And these increase cost of evaluation of exotic algorithms in a high performance real-time environment. To overcome these problems, use sufficient forethought, the costs in performance to reduce implementation complexity and additional design time to often preclude flexible solutions. Hence only high volume applications or extremely critical low volume applications can justify the expense of developing a full custom solution.

The FPGA based designs are programmable logic devices which bear a significant resemblance to traditional custom gate arrays. The more popular series consist of an array of arbitrarily programmable function blocks, with configurable routing resources which are used to interconnect these blocks. These are in-system programmable, which allows the modification of the operation of the device through simple reprogramming. The configuration of the device may be changed to implement alternate filtering operations, such as lattice filters and gradient-based adaptive filters, or entirely different functionality. Like other devices, FPGAs also have limitations like due to the overhead imposed by programmability. In particular, the density of the devices is only now reaching the level necessary to implement complete modules of reasonable complexity. Other difficulties associated with the devices result from the constraints imposed by the architecture, such as limitations on the logic functions which may be implemented in each logic block, and routing delays in the array. Hence the design has to focus on efficient structures which possess low complexity. The advantages offered by FPGAs are the additional flexibility provided by FPGA reconfigurability, the design and test cycle can be completed rapidly due to the elimination of the integrated circuit fabrication delays, high-performance systems can be implemented relatively inexpensively and this device allows adapting the functions to account for unforeseen requirements.

The MAC Unit forms a important unit or structure in the design of filters. Instead of using directly if multiple multipliers are used to implement the same then it is called as variable precision MAC. This paper discusses about the MAC Unit designed to implement FIR filters [1][2] on FPGA based on variable precision.

2. MAC UNIT

Due to ever-increasing IC i.e., integrated circuit fabrication capabilities, the future of FPGA technology promises both higher densities and higher speeds. Many FPGA families are based on memory technology, so the improvements in those areas should correlate with FPGA evolution.

FPGAs are well suited to datapath designs encountered in digital filtering applications which require to perform a nontrivial number of arithmetic operations on a single device. In particular, multiple multiply-accumulate (MAC) units [3] [4] may be implemented on a single FPGA, which provides comparable performance to general-purpose architectures which have a single MAC unit.

This work focuses on using variable precision multiplication approach with adder applicable to FPGAs. The word sizes can be chosen to balance the size of the implementation, which is limited by the FPGA density, against the numerical precision. Larger word sizes are possible if the number of MAC units [4] per chips is reduced. The increase in density of FPGAs in the future will certainly expand the design space available to the designer, and make such constraints less severe [7].

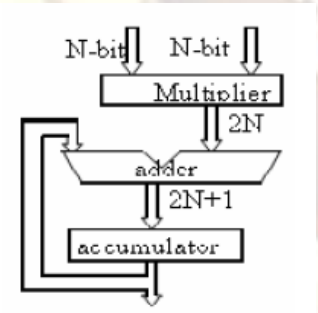

Fig.1: Basic Structure of MAC Unit

The basic structure of MAC Unit [3] is shown in fig.1. it has two N-bit inputs given to multiplier which produces 2N bits as output then an adder is used to add the present and previous bits output of multiplier [1] and accumulator. So the Output bits are usually 2N+1 bits. For floating point numbers based MAC [7] where rounding is required at least once or twice is referred to as fused multiply–add (FMA) or fused multiply–accumulate (FMAC).

3. Digital FIR Filters

The simplest form of realizing an FIR Filter [7] is as shown in fig.2. here the input bit sequence is shown as 'X' and the corresponding coefficients value as 'a'. Since the FIR filter [8] is realized as a MAC Unit, a multiplier, adder and delay element as accumulator are used.

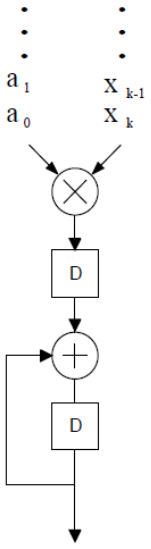

Fig.2: Basic Structure of FIR Filter MAC Unit

4. Variable Precision based MAC Unit

The MAC Units can be implemented using variable precision as discussed in fig.3. Operands A, B and the result R are split into m-bits words that correspond to the size of both the multiplier[1] and the memory cells used in this method, i.e., each of A_0, B_0, and R_0 has m-bits each contained in it.

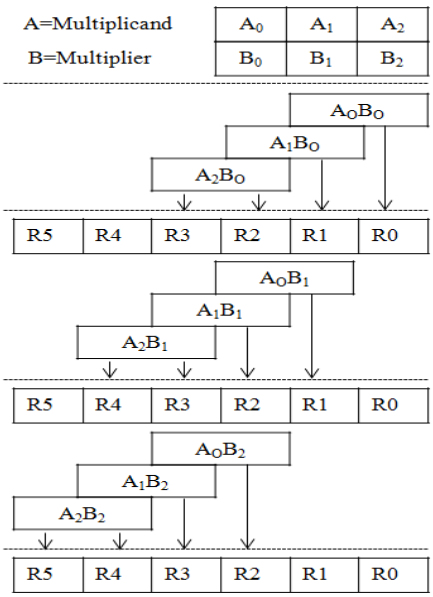

Fig.3: variable precision based multiplication

As the bits are multiplied separately and are finally added to obtain the result, this method is referred to as Variable precision based multiplication [5][6].

The same concept can be utilized for MAC Unit [3] also. Hence the name Variable Precision based MAC (VP MAC) Unit. Fig.4 shows the sample FIR Filter Realization using the VP MAC[5][6]. Since eight bit inputs are considered two sets of four two bit multipliers are used instead of a single multiplier waiting for the sequence to appear as input.

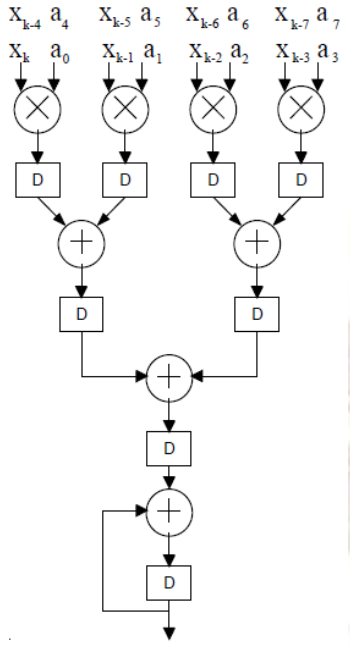

Fig.4: FIR Filter Realization Using VP MAC Unit with Four Multipliers

The design is implemented at algorithm level for FIR Filter [2][7] which is shown in fig.5.

```
Inputs a, x
Input m
Output r=a*x
For  j = 0 to m do
For  i = 0 to m do
Wait for 1delay
Temp = {a2(i),a1(i)}*{x2[j],x1[j]}
Wait for 1 delay
r=r+temp
End for
End for
wait for 1delay
r=r+temp
end
Return r=(r0,r1,….,r2m+1)
```

Fig.5: Algorithm for FIR Filter using VP MAC Unit

In this algorithm ‘a’ and ‘X’ are treated as coefficients and input bit sequence respectively. To implement the same for the VP MAC based FIR Filter, each of ‘a’ and ‘X’ are made into m bits each. a1, a2, x1 and x2 represent the m-bit sequence considered for VP MAC Unit [5].

5. Results and Discussion

The designs for conventional MAC based FIR Filter [2][3] and VP MAC [5][6] based FIR Filters are coded in Verilog HDL and are implemented in Xilinx ISE10.1i for Spartan 3E FPGA Family, for the device XC3S500E, for package FG320 with a speed of -5.

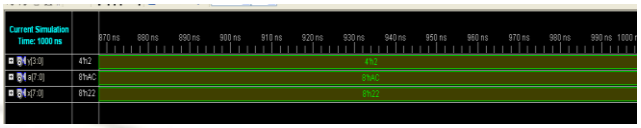

Fig.6: Simulation Results of the filters

The simulation results are shown in fig.6 where ‘a’ is taken to be 10101100 and the input bit sequence as 00100010 resulting in the output sequence as 10.

Table.1: Comparison Table for FIR Filters

Device Details	Using MAC	Using VP MAC
No. of Slices	84 out of 4656	51 out of 4656
No. of 4-Input LUTs	135 out of 9312	96 out of 9312
No. of Bonded IOBs	20 out of 232	20 out of 232
Combinational Path Delay	53.420ns	21.913ns

Table.1 shows the comparison results for the two methods based on algorithms and from this table it is clear that the the VP MAC utilizes less area and operates with more speed when compared to conventional MAC unit.

6. Conclusion

In this paper we have proposed a new algorithm to design MAC unit for implementation of FIR Filters on an FPGA using the concept of variable precision multiplication, which can be used for high performance filters than the conventional MAC unit. Hence the use of variable precision can serve the high sampling rates of filters and can be implemented on the FPGAs which promise flexible and efficient designs for the DSP Applications as the density of FPGAs increases in future, for more accurate and efficient filtering.

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