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Existing Full Adders and Their Comparison on The Basis of Simulation Result And to design a improved LPFA (Low Power Full Adder)

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Abstract

The main objectives is to compare the existing full adders circuits and there performances and to design a Low Power Full Adder having improved result as compared to existing full adders. The various full adders are described namely BBL-PT (branch based logic and pass transistor logic based), conventional CMOS full adder and hybrid full adder. Finally comparisons between the various full adders have been done to show the better performance of LPFA in terms of power consumption, area (number of transistors) and delay.

The LPFA and all other various full adders are designed and simulated using mentor graphics tool in 0.18 µm technology. The frequency used is 100 MHz. the voltage and all the various full adders and others designs are simulated at a voltage supply of 1.8V at same frequency.

1. Introduction

ADDITION is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. In addition to its main task, which is adding binary numbers, it is the nucleus of many other useful operations such as subtraction, Multiplication, division, addresses calculation, etc. In most of these systems the adder is part of the critical path that determines the overall performance of the system. That is why enhancing the performance of the 1-bit full-adder cell (the building block of the binary adder) is a significant goal.

The choice of logic style to design digital circuits strongly influences the circuit performance. The delay time depends on the size of transistors, the number of transistors per stack, the parasitic capacitance including intrinsic capacitance and capacitance due to intracell and intercell routing, and the logic depth (i.e., number of logic gates in the critical path). The dynamic power consumption depends on the switching activity and the number and size of transistors. Among other things, the die area depends on the number and size of transistors and routing complexity.

At the system level, in many synchronous implementations of microprocessors, the adder lies in the critical path because it is a key element in a wide range of arithmetic units such as ALUs and multipliers.

Extensive variants of full adders have been investigated by the academic and industrial research communities. The usual performance evaluations are speed, power consumption, and area. However, since mobile and embedded applications have prioritized the power consumption to stand at the top of circuit and system performance evaluations, the goal of many of these full-adder variants has traditionally been the reduction of transistor count. However, Chang *et al.* have shown in that although some of these full adders feature good behavior when implementing a 1-bit cell, they may show performance degradation when used to implement more complex structures.

Recently, building low-power VLSI systems has emerged as highly in demand because of the fast growing technologies in mobile communication and computation. The battery technology doesn't advance at the same rate as the microelectronics technology. There is a limited amount of power

Available for the mobile systems. So designers are faced with more constraints: high speed, high throughput, small silicon area, and at the same time, low-power consumption. So building low-power, high-performance adder cells is of great interest.

2. Existing full adder circuits

There are standard implementations for the full-adder cell that are used from last few years some of them among these adders there are the following:-

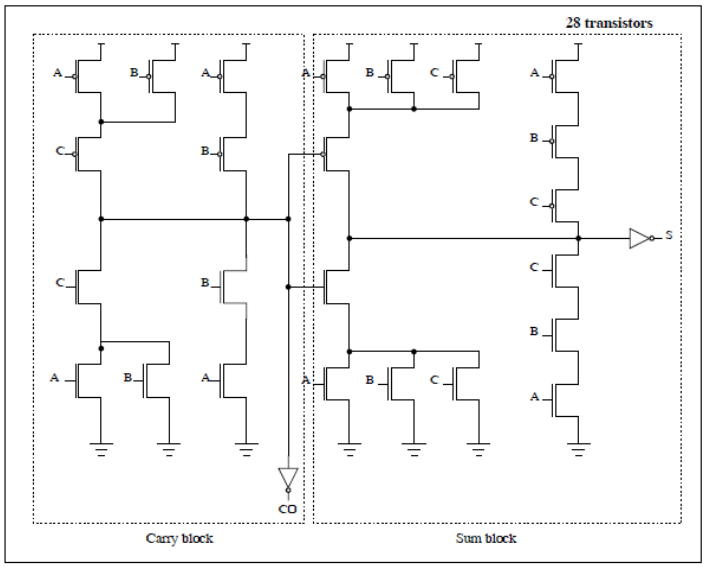


Figure.1- The Conventional CMOS full-adder

The CMOS full adder (CMOS)[1] has 28 transistors and is based on the regular CMOS structure
The Mirror logic [6] style based full adder has 28 transistors

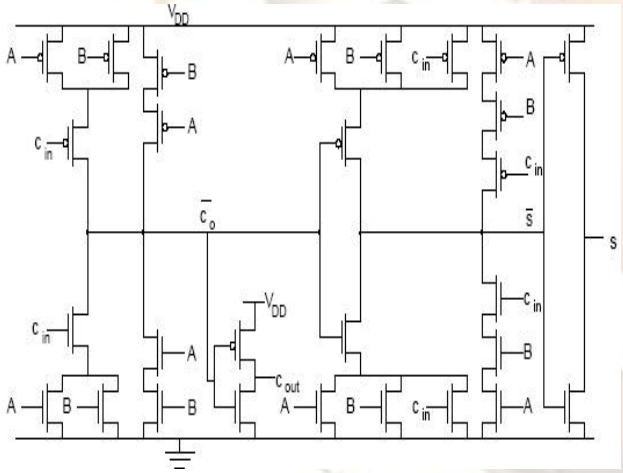


Figure-2: Mirror logic style based full adder

The DPL logic [3] style based full adder has 28 transistors

A Transmission gate full adder [4] using 18 transistors
A full adder cell using 14 transistors
A full adder cell using 10 transistors

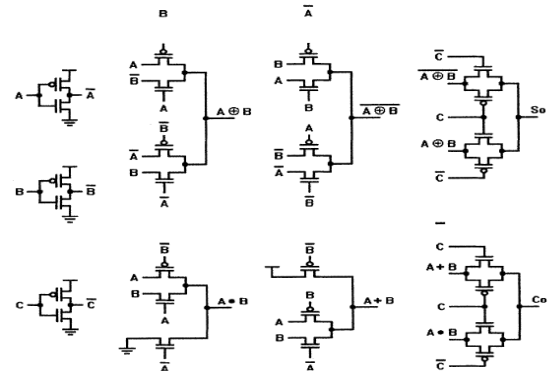


Figure: 3-DPL logic style based full adder

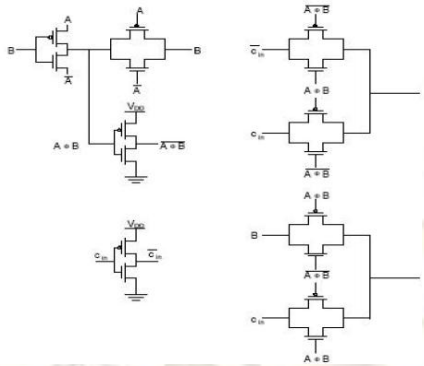
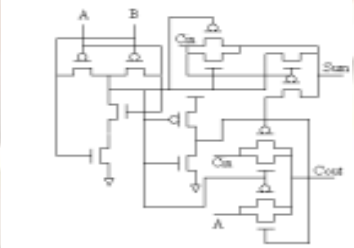


Figure-4: Transmission gate full adder

The DPL provides a saving power of about 2% over the conventional CMOS based full adder. But they generally do not provide good advantage over the delay. So the main advantage in PDP (power delay product) is only due to lesser power consuming Logic style. The TG-FA provides a power saving of 1% and delay reduction of about 2% over the conventional CMOS Based full adder.



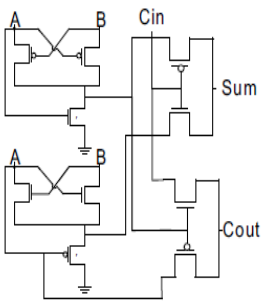


Fig-5:14-T full adder cell Figure-6:10-T full adder cell

3. Simulation result and comparison

These different full adder circuits were compared by the simulation using TSMC 180nm based mentor graphics technology.

(a). Conventional CMOS based Full adder simulation:-

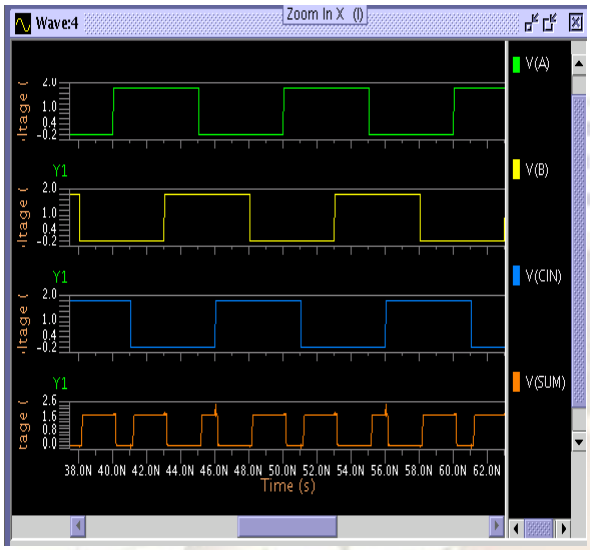


Figure 38:- Sum output of CMOS full adder

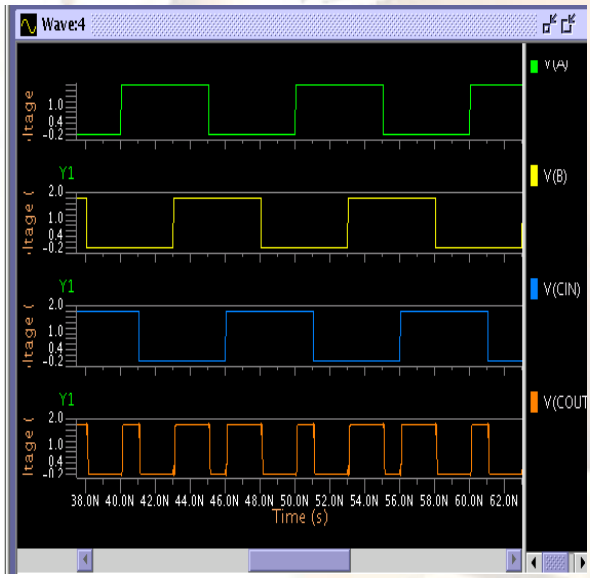


Figure 39:- Carry output of CMOS full adder

Now we will check the dynamic power dissipation of the conventional CMOS full adder by using the waveform for average current

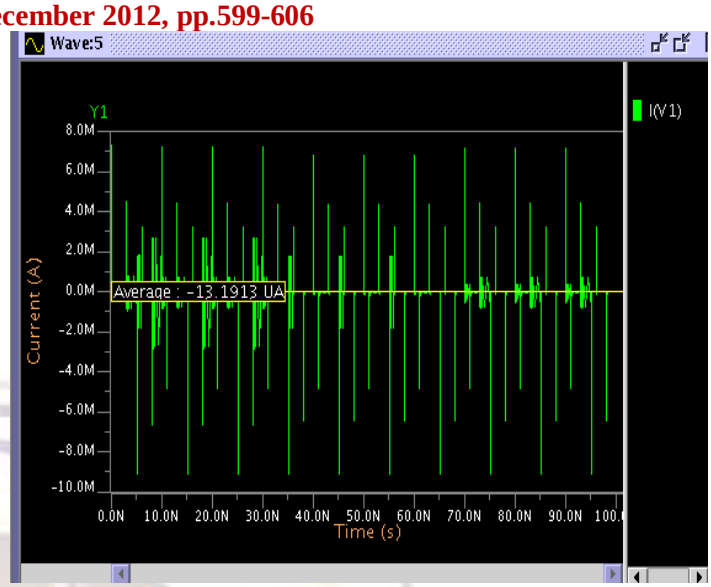


Figure 40:- Average current output of CMOS full adder

Dynamic power dissipation= (average current) x (voltage supply (V_{dd}))

So P= (13.1913μA) x (1.8v) =23.7443 μW

This value will be used further in table 5 for comparison among various full adder designs

(b). BBL-PT based Full adder simulation work:-

Next we will discuss about the BBT-PT full adder schematic and output waveforms:-

Figure 41 gives the schematic for BBL-PT full adder block. Now next we will see the output waveforms for the BBL-PT full adder in 180nm mentor graphics at a voltage of 1.8V.

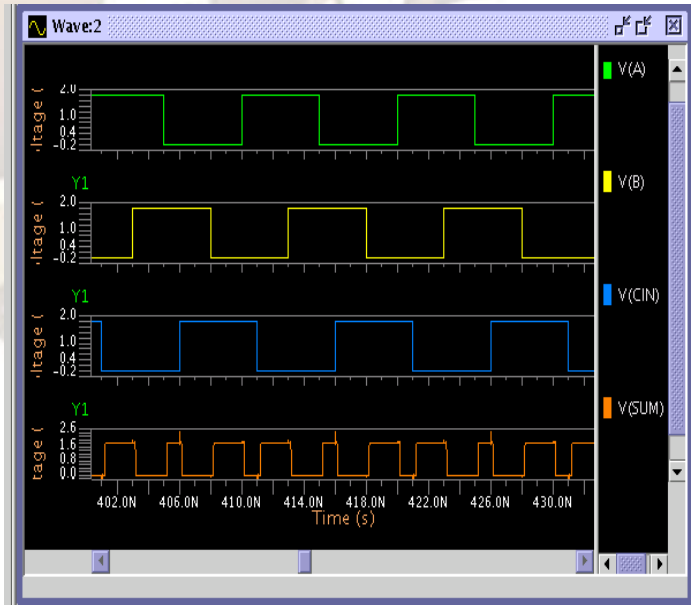


Figure 42:- Sum output of BBL-PT based full adder

Figure 42 gives the sum output of the three inputs A,B,Cin.also to be noted that we are doing the simulation at a frequency of 100 MHz and a voltage supply of 1.8V is used.

Figure 43 shows carry output of the three inputs A,B,Cin of BB-PT the spikes in the output of sum and Carry output is due to switching of inputs from "0" to "1" and vice versa.

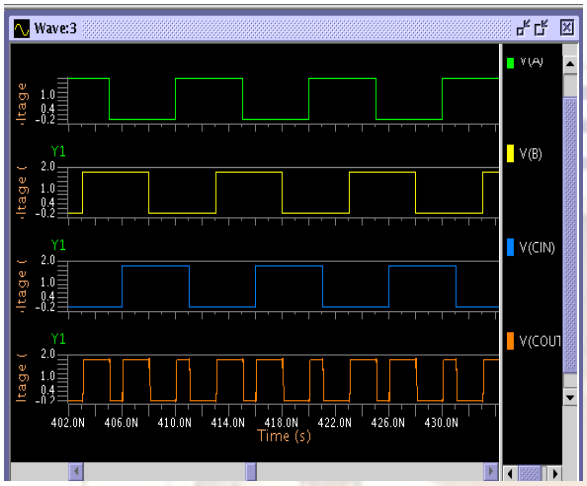


Figure 43:- Carry output of BBL-PT based full adder

Figure 44 shows the average current waveform for the BBL-PT full adder cell. We will use this output to find the dynamic power dissipation. Finally we will compare this output with the conventional CMOS full adder and HYBRID FULL ADDER.

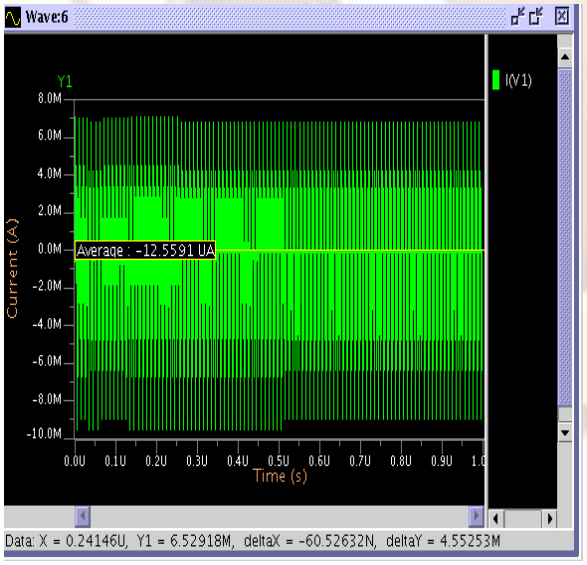


Figure 44:- Average current for the BBL-PT full adder

Now we will find the dynamic power dissipation for BBL-PT full adder

Dynamic power dissipation P=(average current) x (voltage supply (V_{dd}))

Sop= (12.5591 µA) x (1.8V) =22.60638 µW

(c) .Hybrid full adder simulation work:-

Now we will discussed about the Hybrid full adder and related waveforms. The schematic for the Hybrid full adder is shown in Figure 45.Figue 46 will show the zoomed view of Hybrid full adder.

Further we will see the sum and carry output for the HYBRID FULL ADDER Figure 47 shows the sum output of the HYBRID FULL ADDER. The spikes here are also due to simultaneous switching of inputs A, B, Cin.

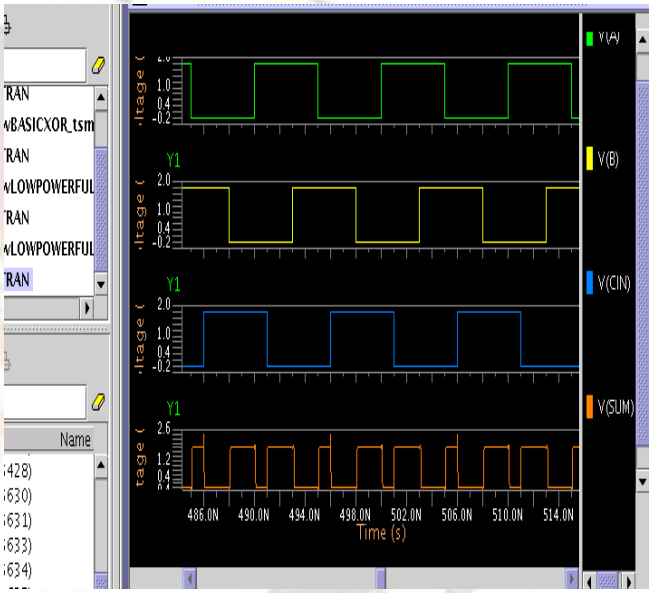


Figure 47:- Sum output of Hybrid full adder

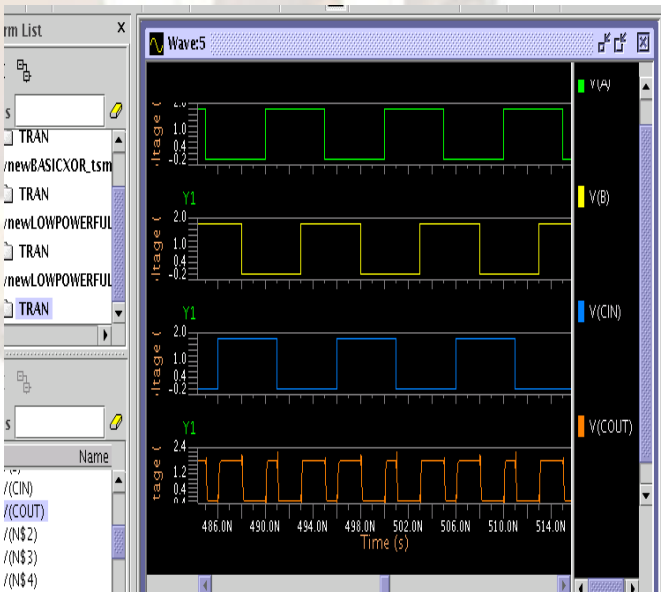


Figure 48:- Carry output of Hybrid full adder

Carry output of HYBRID FULL ADDER is shown in Figure 48.now finally on next page we will see the average current for the HYBRID FULL ADDER. That will be used to find dynamic power dissipation as discussed earlier.

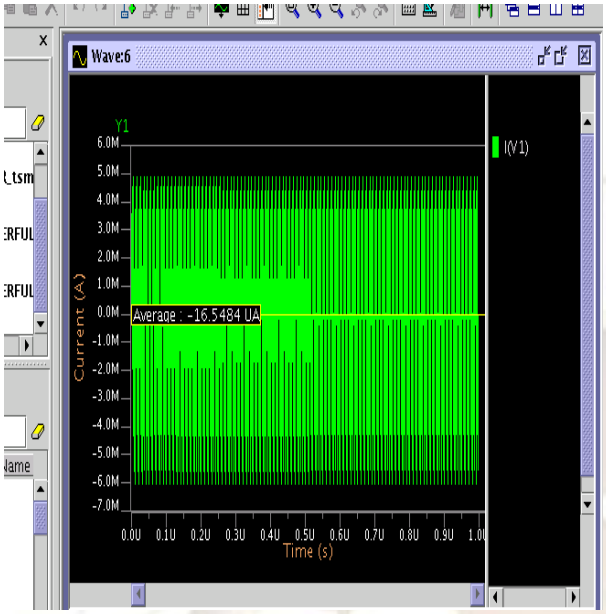


Figure 49:- Average current for the Hybrid full adder

Now we will use this average current waveform to find the dynamic power dissipation.

Dynamic power dissipation P=(average current) x **(voltage supply (V_{dd}))**

SoP= (16.5484 µA) x (1.8V) =29.7871µW

4. Design of Low Power XOR and Low Power XNOR

The improved versions are illustrated in Fig. 11 and Fig.12.In the improved versions both designs use 4transistors to achieve the same functions of XOR and XNOR.

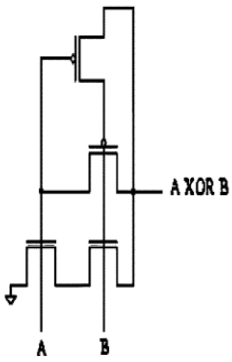


Fig:-11: LP XOR gate

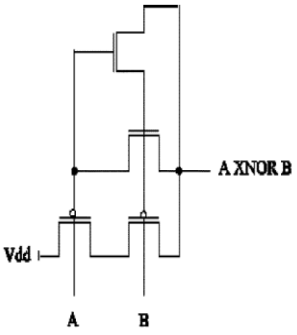


Fig 12:-: LP XNOR gate

Analysis on XOR structure, the output signals in the cases of input signal AB = 01, 10, 11 will be complete. When AB = 00, each PMOS will be on and will pass a poor "LO' signal level to the output end. That is, if *AB* = 00, the output end will display a voltage, threshold voltage ~V_{pth}, a little higher than "LO". For the XNOR function, the output signal in the case of *AB* = 00, 01, 10 will be complete. While *AB* = 11, each NMOS will be on and pass the poor "HI" signal level to the output end. The analysis of driving capability is the same as XOR structure. The structures stated above are the versions of 4 transistors without a driving output.

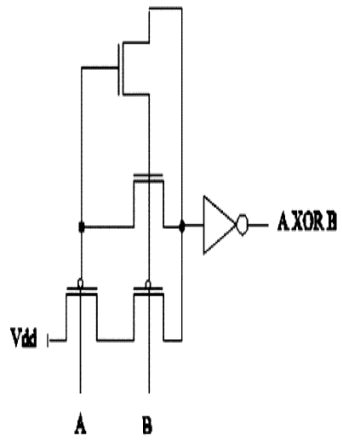


Fig:-13: LP XOR gate With driving outputs

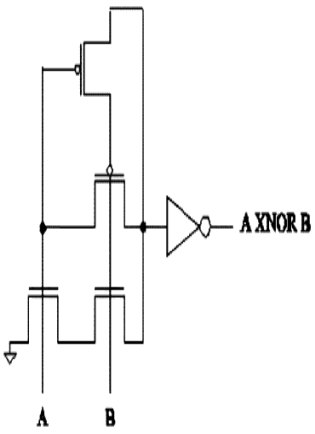


Fig 14:-: LP XNOR gate with driving outputs

By cascading a standard inverter to the LP XNOR circuit, a new type of XOR, as shown in Fig. 13 and Fig 14, will have a driving output, and the signal level at the output end will be perfect in all cases. The same property is present in the XNOR structure.

The output waveforms for XOR and XNOR for are given inputs A and B are shown in Fig 15, 16 and Fig 17.

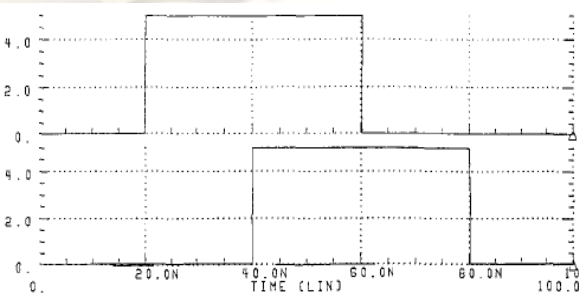


Fig-15:-showing the input signals A and *B*.

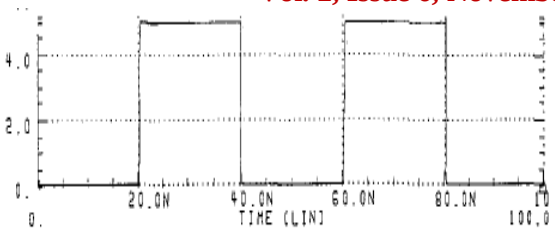


Fig:-16:- Showing the output of 6-transistor XOR.

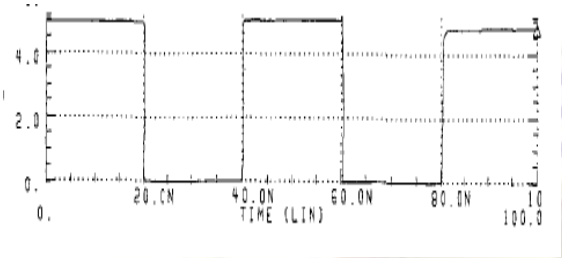


Fig:-17:- Showing the output of 6-transistor XNOR

5. Design of Low Power Adder Using LP XOR and XNOR:-

The Low power full adder which takes lesser number of transistors than the all other previously discussed configurations. The major drawback of this method is that although it utilizes lesser number of transistors but it does not provide full swing at the output which is needed to drive any external load. So to avoid this type of problem we will form the XOR by using XNOR followed by an inverter. Figure:-50 shown below is the schematic for the LOW POWER FULL ADDER (LPFA).

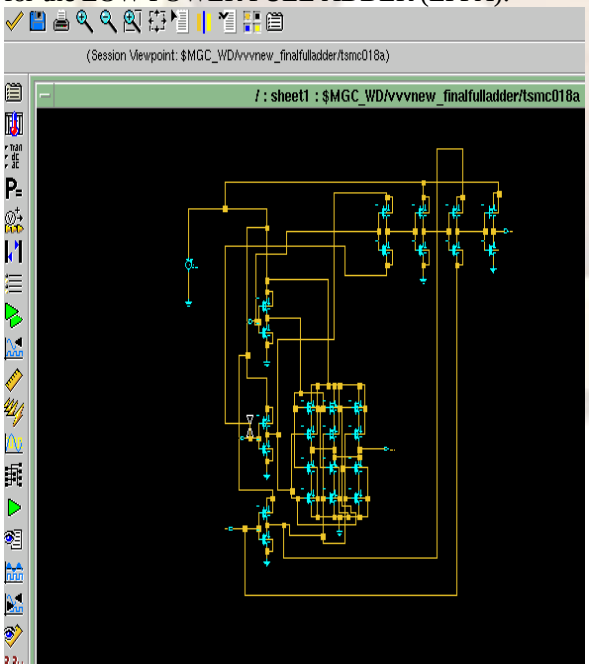


Figure 50:- LPFA (Low Power Full Adder) schematic

Now next we will show the sum and carry output waveform of LPFA (Low Power Full Adder).

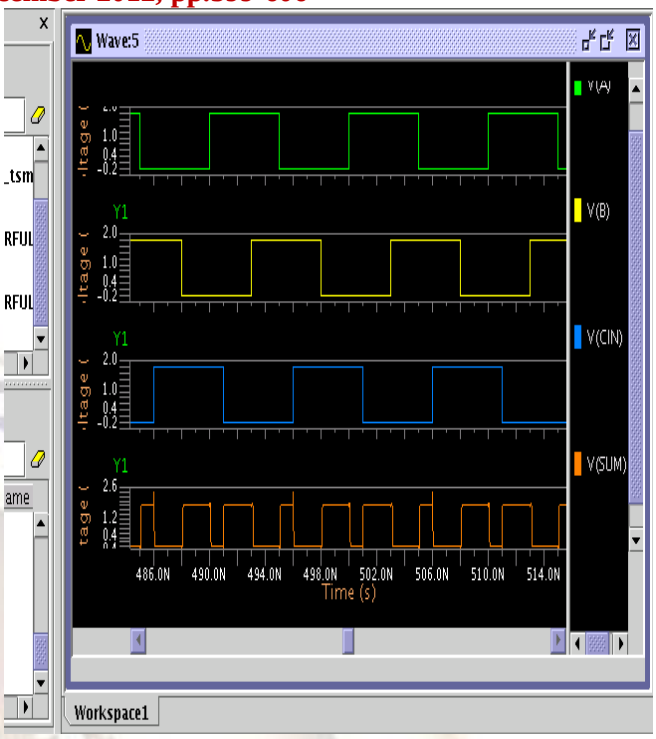


Figure 51:-Input and Sum output waveform of LPFA

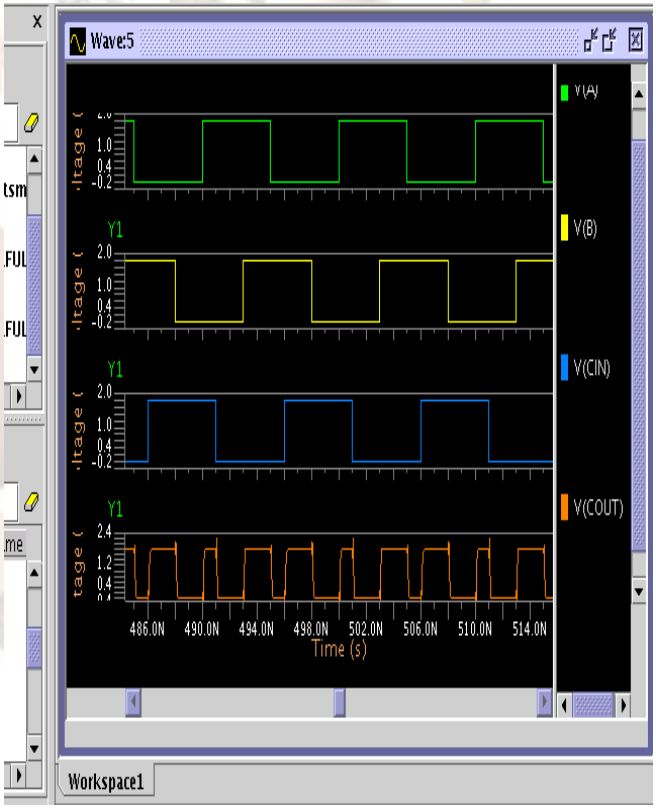


Figure 52:- Input and Carry output waveform of LPFA

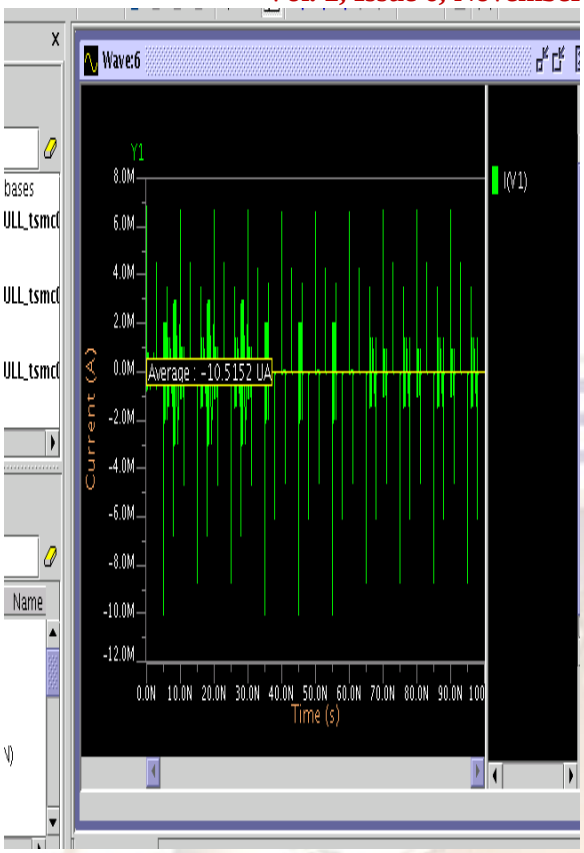


Figure 53:-Showing average current of LPFA

Now we will use this average current waveform to find the dynamic power dissipation.

Dynamic power dissipation P= (average current) x (voltage supply (V_{dd}))
SoP=(10.5152µA) x (1.8V) =18.92736 µW

6. Conclusion and Future work

As observed from the discussion about the full adder that various designs have their own advantage and disadvantage in terms of area, delay and power consumption. So reducing any of these parameters will leads to a high performance design of full adder design.

Hence we can see that LPFA (Low Power Full Adder) is better than all the other full adder designs in terms of Power consumption, Area (Number of Transistor), Delay, PDP (Power Delay Product.

Future work will be focused on the reduction of any of the parameter shown above i.e. **Area, Delay and Power**. There is also another term i.e.**PDP** (power delay product) this is generally used for to make a trade-off between power consumption and delay.

Table 5:- Showing the comparison of performance Conventional CMOS full Adder, BBL-PT based full adder, HYBRID FULL ADDER and LPFA

Design	Delay(ps)	Static Power Dissipation(pW)	Dynamic Power Dissipation(µW)	Total Power(µW)	Transistor Count
Conventional CMOS full adder	124	143.592	23.7443	23.74443	28
BBL-PT logic based full adder	110.3	126.308	22.60638	22.606506	27
Hybrid full adder	142	158.674	29.7871	29.787258	30
Low Power full adder (LPFA)	**101.2**	**113.869**	**18.92736**	**18.927473**	**26**

Figure-5

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