DYNAMIC POWER REDUCTION IN SRAM

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ABSTRACT

To reduce the dynamic power consumption in SRAM a new design technique is proposed here. The proposed technique is compared with 8T SRAM cell design technique using 0.18 micron technology. Simulation results indicates that the proposed technique provides an improvement of 64% in bitline leakage ,22.64% in write '0' power, 30.68% in write '1' power over 8T SRAM cell design technique.

Keywords - Dynamic power, scaling, leakage power, SRAM, process variation.

I. INTRODUCTION

Due to the rapid advancement in VLSI technology over the last two decades , aggressive scaling of MOS transistor dimensions is becoming a trend in order to achieve high packaging density chips and improved performance . Supply voltage and threshold voltage are also scaled in order to maintain the reliable operation of the transistors. Scaling results in increased active power dissipation and this problem becomes more severe in deep submicron region. The major part of the total power dissipation comes from the leakage power and this component is expected to rise for next generation techniques. Leakage current increases exponentially with the scaling of the device dimensions and this poses a threat for battery operated devices. Optimizing the device sizing voltage scaling & switching activity reduction are some common practices that are followed for reducing the power consumption. Since the dynamic power (Pd) in CMOS based circuits is directly proportional to the square of the supply voltage, reducing supply voltage will definitely lead to considerable saving in dynamic power, however leakage power reduces linearly to the first order[1]. The performance of SRAM cell is severely affected at low supply voltage and the effect of process variation make the situation even more worse. In this paper we propose a design of 10-T SRAM that reduces the dynamic power consumption without compromising much on other important design metrics . To prove the effectiveness of the proposed technique , it is compared with 8-T SRAM cell. This paper is organized as follows :

In section II conventional 6T SRAM cell is discussed . Section III presents on overview of 8T SRAM cell along with its read and write operation

mechanism. Proposed technique is described in section IV. Section V shows the simulation results and finally in section VI conclusions are drawn.

II. CONVENTIONAL 6T SRAM

6T SRAM cell is most widely used in embedded memory because of its fast access time and relatively small area. 6T cell design involves complex tradeoffs between various factors namely minimizing cell area, good soft error immunity, high cell read current, low leakage current, good cell stability with minimum voltage & minimum word line pulse. The full CMOS 6T SRAM bit cell configuration is shown in Fig.1. Full CMOS SRAM configuration provides superior noise margin, low static power dissipation, high switching speeds & suitability for high density SRAM arrays [2]. Each 6T cell has a capability of storing one bit of data.
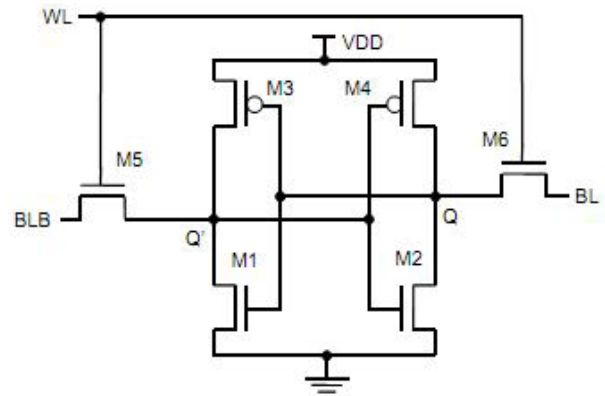

Fig. 1 Traditional 6T SRAM cell

6T SRAM cell consists of two inverters connected back to back. M5 & M6 are access transistors which are controlled by the word line (WL) signal. The cell preserves one of its two possible states denoted as '0' and '1' as long as power is available to the bit cell. Static power dissipation is very small due the use of CMOS inverters [3].

There are three operations in SRAM memory cell namely write, read and hold operations. Read and write operations are initiated by asserting the word-line (WL) signal. During write operation the value to be written is applied to the bit lines and for read operation both BL and BLB is precharged to VDD. During the read operation the '0' storing node is perturbed & this might flip the stored data, however the successful write operation requires that

data should be flipped very easily. Traditionally device sizing has been adopted to balance the read versus write design requirements [1].

III. 8T SRAM CELL

Fig.2 shows the schematic diagram of 8T SRAM cell. Due to the stability limitations of 6T SRAM cell at low supply voltages, 8T SRAM is suitable for multimedia applications [4].
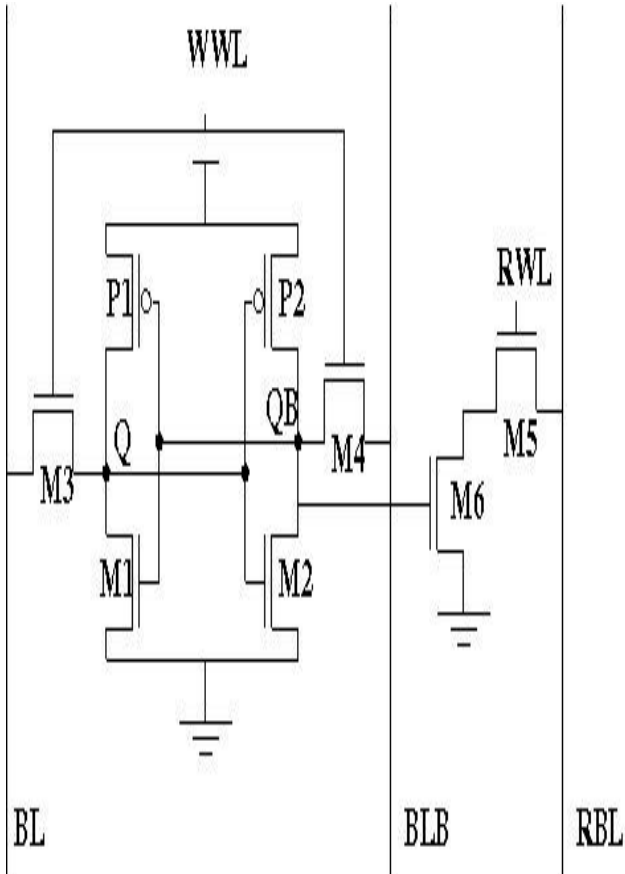

Fig. 2 Schematic diagram of 8T SRAM cell

8T SRAM cell has the normal 6T SRAM design with a read decoupled path consisting of two NMOS transistors M5 & M6. Read operation of 8T SRAM is initiated by pre-charging the read bit line to full swing voltage. After pre-charging read bit line, RWL is asserted that drives access transistor M5 on. If Q=0 then M6 is on & RBL discharges through transistors M5 & M6 to ground. This decrease in the voltage of RBL is sensed by the sense amplifier. During read '1' operation, when Q='1' M6 remains off so there will be no discharge current flow through the read path. In this situation only a very small amount of leakage current flows which is called bit line leakage. Write operation of 8T cell is similar to 6T cell but the pre-charge circuitry at the bit lines is replaced by write driver.

IV. PROPOSED TECHNIQUE

The proposed 10T SRAM bit cell is shown in Fig. 3. It contains 10 transistors. M1-M3 and M2-M4 form a pair of cross coupled inverters. M5 & M6 are access transistors; M7 & M8 constitute a separate path for read operation. M9 & M10 act as switches to conditionally connect the read path to any one of the write bit lines depending upon the last written data. M5 & M6 are controlled by word line (WL) signal which is asserted during write cycle only. M7 & M9 are controlled by read word line (RWL) signal. Both WL & RWL signals are controlled by a row decoder.
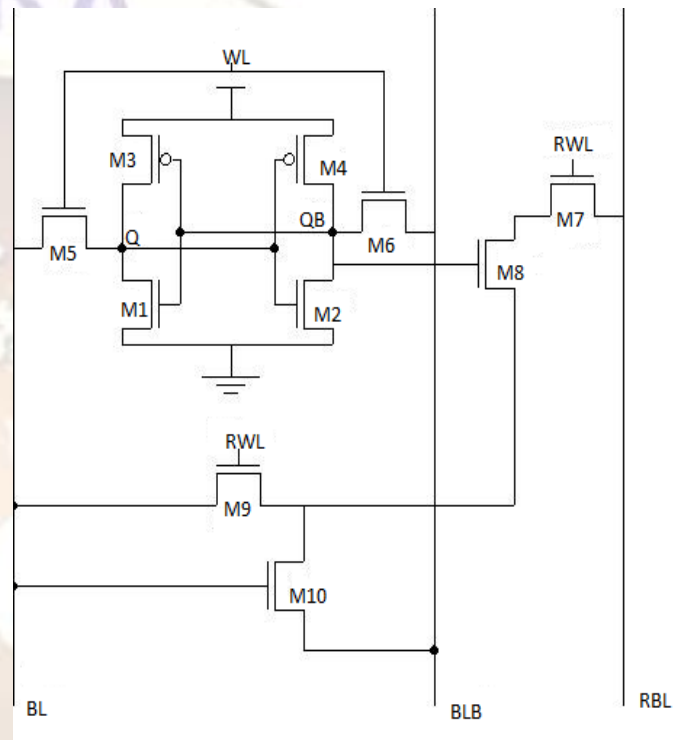

Fig. 3 Proposed 10-T SRAM CELL

Write operation of the proposed cell begins with WL going high which turns on M5 M6 transistors and write operation is performed similar to that of 6T SRAM cell. Read operation begins first pre-charging RBL line to full swing voltage & after that RWL signal is asserted. This turns on M7 & M9 transistors. Assume Q='1', so M8 will be off & hence no discharge current flows through read path, but when Q='0' then M8 will be on & hence RBL will discharge through M7, M8, M9/M10 to BL/BLB. This decrease in voltage of RBL is detected by sense amplifier.

A.   Power   reduction   mechanism   of   the proposed technique :-

In order to reduce the bit line leakage reduction in read '1' mode an additional transistor is used in read path. Bit line leakage is reduced by stacking effect. M9 transistor act as a stacking transistor.

i.   In order to reduce the read power, the swing of read bit line (RBL) is reduced. During read '0' operation charge is shared between RBL and BL or RBL and BLB depending on the fact that the last written data was logic '0' or '1' respectively. Due to charge sharing RBL does not discharge completely & stays at mid level voltage & so in the next cycle pre-charge circuitry consumes less power to drive the bit line from mid level value to the full swing voltage.

ii.   For write power reduction the proposed technique does not use pre-charge circuitry for the write bit lines instead a write driver is used that drives the bit lines high or low depending upon the data value. Write power reduction is possible only after read '0' operation, this can be understood as follows :- consider a write '0' operation followed by a write '1' operation. In this case initially BL=0 and BLB=1. During read '0' the read discharge flows through read path & M9 to BL & this charges BL partially. In next cycle of write '1' the write driver has to drive BL to logic 1 from an intermediate level voltage & this reduces the write power.

V. SIMULATION RESULTS

Proposed 10T SRAM cell & 8T SRAM cell have been designed & simulated using Tanner SPICE version 13.0 simulator & transistor models 0.18 micron technology were used. The impact of voltage scaling on the dynamic power consumption of 8T & proposed 10T SRAM cell is analyzed.

It is the quite clear from the simulation results that the proposed 10T SRAM cell reduces the read power consumption 66% at VDD=1.0 V as compared to 8T SRAM cell. The write '0' & write '1' powers are also reduced by 22.64% & 30.68% respectively.

Fig.4 shows the variation of bit line leakage with supply voltage scaling & this shows that bit line leakage is reduced by 64%. It must also be noted that reduction in the read power with reduced supply is due to the fact that the level of RBL discharge decreases with supply reduction.
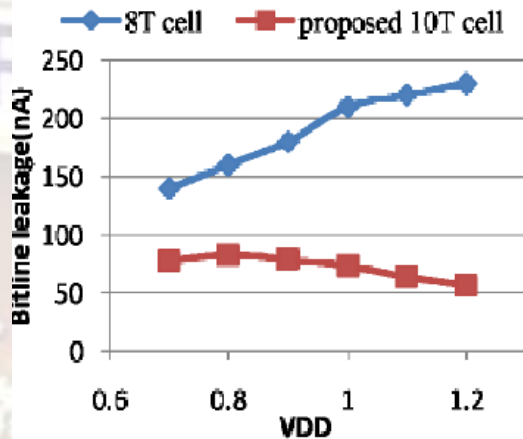

Fig.4 Bit line leakage variation with supply voltage scaling

VI. CONCLUSION

The feasibility of the proposed 10T SRAM has been shown by means of simulation and experimental results. The proposed technique provides an improvement in terms of dynamic power consumption as compared to 8T SRAM cell. As already shown in the simulation results that the proposed technique reduces the bit line leakage by 64%, write '0' & write '1' powers are reduced by 22.64% & 30.68% respectively as compared to 8T SRAM cell. An improvement of 66% is achieved in terms of read power consumption at supply voltage of 1V. These improvements are achieved at the cost of increased layout area due to addition of two extra transistors.

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SUPPLY VOLTAGE (Volts)	READ '0' POWER(μW)		WRITE '1' POWER(μW)		WRITE '0' POWER(μW)		BITLINE LEAKAGE(nA)	
	TECHNIQUE		TECHNIQUE		TECHNIQUE		TECHNIQUE	
	8T CELL	PROPOSED 10T CELL	8T CELL	PROPOSED 10T CELL	8T CELL	PROPOSED 10T CELL	8T CELL	PROPOSED 10T CELL
1.2	25	9.9	25.4	16.	22.7	17.	225	56.5
1.1	20.	8.0	21.3	15.	18.4	15.	215	63
1	18.	6.2	17.6	12.	15.9	12.	205	73.4
0.9	14.	4.1	14.3	10.	13.0	10.	185	78
0.8	11.	3.5	11.1	8.0	10.2	8.2	155	82
0.7	8.0	2.1	8.43	6.6	7.53	6.5	140	76.6

Table 1 power consumption of 8T & proposed 10T SRAM cell.

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