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Design Of High Speed FFT Processor Using Vedic Multiplication Technique

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ABSTRACT

All of us are familiar with the digital circuitry. Now days the digital circuitry has replaced most of the analog circuitry in various places because technically digital domain is much better than the analog domain. To operate these digital signals we use the Digital Signal Processors. In digital signal processing to perform different types of operations we use various algorithms , out of these algorithms Fast Fourier Transform (FFT) is the most important and significant algorithm. Basically the FFT algorithm is used as an efficient means to compute the DFT and IDFT. The FFT algorithm is used in variety of areas, including linear filtering, correlation and spectrum analysis, because of its capability to perform efficient computation in comparison to the DFT. There are mainly two ways, through which FFT algorithm can be performed, which are DIT and DIF whose acronyms are Decimation In Time and Decimation In Frequency respectively. Speed of both of these FFT algorithms mainly rely on the multiplier used in it. So performance of FFT processor can enhanced with the use of highly speed efficient multiplier. And in direction to achieve this goal of designing Speed efficient FFT processor, speed of different popular multiplication algorithms has been compared in this paper. Our work shows that Vedic multiplier is the best multiplication algorithm comparison to other popular multiplication algorithms, because of it there is the possibility to generate partially generated products in parallel manner. For this design the target FPGA which we have takes belongs to Virtex-2P (family), XC2VP2 (device), FG256 (package) with speed grade of -7. For synthesis purpose Xilinx synthesis tool (XST) of Xilinx ISE-9.2i has been used. The behavioral simulation purpose ISE simulator has been used.

Keywords - **Fast Fourier Transform, Vedic Multiplier, FPGA, FFT processor, Xilinx.**

1. Introduction

Digital technology that is omnipresent in almost every engineering discipline. Faster additions and multiplications are of extreme importance in DSP for convolution, discrete Fourier transform, digital filters, etc. The core computing process is always a multiplication routine; therefore, DSP engineers are constantly looking for new algorithms and hardware to implement them. Vedic mathematics is the name given to the ancient system of mathematics, which was rediscovered, from the Vedas between 1911 and 1918 by Sri Bharati Krishna Tirthaji. The whole of Vedic mathematics is based on 16 sutras (word formulae) and manifests a unified structure of mathematics. As such, the methods are complementary, direct and easy. signal processing (DSP) is the Due to a growing demand for such complex DSP application, high speed, low cost system-on-a-chip (SOC) implementation of DSP algorithm are receiving increased the attention among the researchers and design engineer. Fast Fourier Transform (FFT) is the one of the fundamental operations that is typically performed in any DSP system. Theory about it can be easily accessed from any standard reference book. The Fast Fourier Transform (FFT) is a computationally intensive digital signal processing (DSP) function widely used in applications such as imaging, software-defined radio, wireless communication, instrumentation and machine inspection. Historically, this has been a relatively difficult function to implement optimally in hardware leading many software designers to use digital signal

processors in soft implementations. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. Employing these techniques in the computation algorithms of the coprocessor will reduce the complexity, execution time, area, power etc. In this paper reconfigurable FFT is proposed to design by Vedic mathematics. Urdhva Triyakbhyam, being a general multiplication formula, is equally applicable to all cases of multiplication. Nikhilam algorithm with the compatibility to different data types. This sutra is to be used to build a high speed power efficient reconfigurable FFT [19].

2. Proposed Multiplier

For 2-Bit multiplication Conventional Vedic multiplication Hardware has been used it has been discussed in [11]. As at 2 bit level multiplication we have not to worry about the carry propagation path.

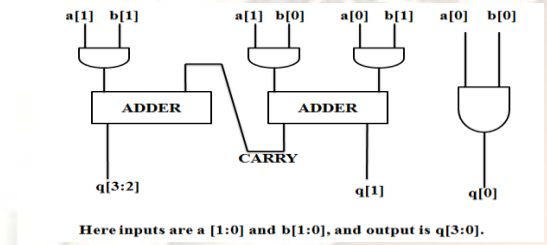


Figure 2.1: Two Bit Conventional Vedic Multiplier

Diagram for Unique addition tree structure for partial product addition for 4 bit is given in the following [18]:-

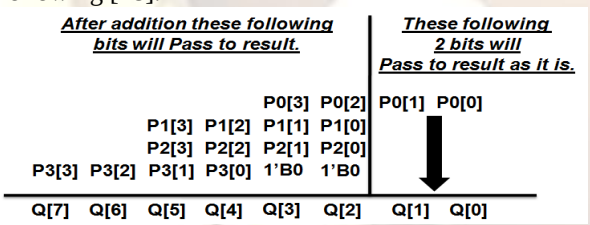


Figure 2.2: Proposed Addition Tree Structure of 4-Bit Multiplier

Diagram for Unique addition tree structure for partial product addition for 8 bit is given in the following [18]:-

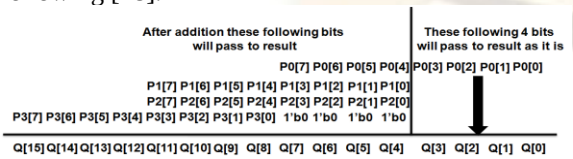


Figure 2.3: Proposed Addition Tree Structure of 8-Bit Multiplier.

Here the assignment of partial products P0, P1, P2, P3 has given from right to left at output of vedic N/2-Bit Vedic multiplier, where N shows the no. of bits in one input of multiplier. And also which addition tree structure we have designed is very simple to understand, design and implement. Here for the addition purpose the unique addition tree structure. The block diagram [18] for 4 bit level multiplication shown below.

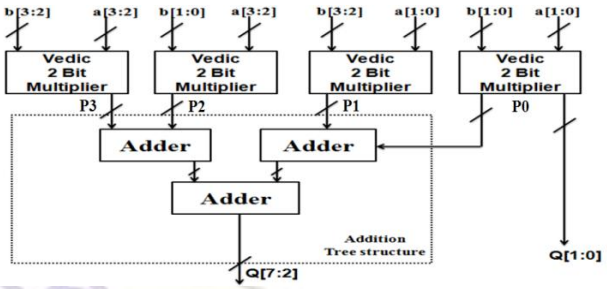


Figure 2.4: Block Diagram of Proposed 4-Bit Vedic Multiplier

Block diagram [18] of 8-Bit Vedic Multiplier is shown below:-

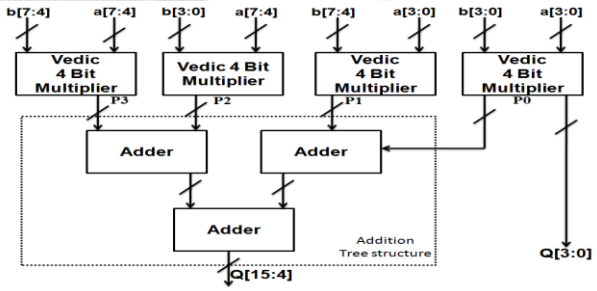


Figure 2.5: Block Diagram of Proposed 8-Bit Vedic Multiplier

3. Comparative Results

To show the efficiency of proposed Vedic multiplier at eight bit level, it has been compared with some other popular multiplier structures based on different multiplication algorithms at the eight bit level. For the comparison purpose some standard papers have been used. For true and reliable comparison, proposed multiplier has been implemented on the same platform of target FPGA, which has been used by the reference papers. Comparative tables are shown below:-

(a)In the following given table the target FPGA used belongs to Virtex 2P (family), XC2VP2 (device), FG 256 (Package), -7 (speed grade).

Table 3.1 Comparative Table 1 for Different Multipliers at 8-Bit Level

Maximum Combination Path Delay for Different Multipliers at Eight Level in Nano Seconds						
Karatsuba [10]	Vedic Karatsuba [10]	Modified Booth Wallace [4]	Vedic with Partitioning [4]	Conventional Vedic [10]	Vedic with CSA [4]	Proposed [18]
31.039	18.695	15.815	15.685	15.418	13.07	11.886

(b)In the following given table the target FPGA used belongs to Spartan 3 (family), XC3S50 (device), PQ 208 (Package), -4 (speed grade).

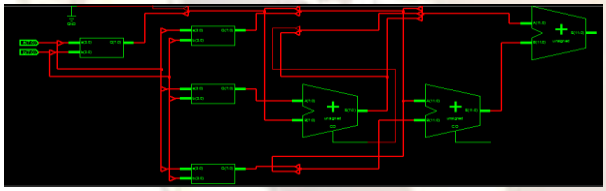
Table 3.2: Comparative Table 2 for Different Multipliers at 8-Bit Level

Maximum Combination Path Delay for Different Multipliers at Eight Level in Nano Seconds			
Array [2]	Booth [2]	Conventional Vedic [2]	Proposed [18]
32.01	29.549	21.679	19.467

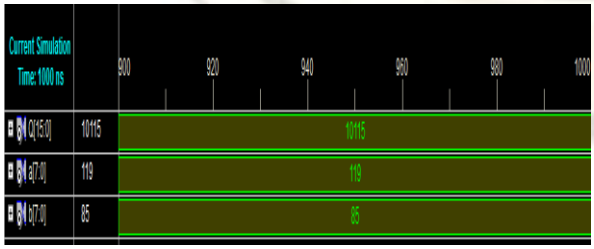
By designing the proposed Vedic multiplier for the same reconfigurable hardware as shown in [4] and [2], make the comparison platform (hardware) independent, algorithmic, technique and approach based comparison. So by comparing with different multipliers at the same platform it can be concluded that the algorithm and approaches which has been proposed to design Vedic multiplier, in this thesis work, is better in comparison to the other popular algorithms and approaches shown in [4] and [2]. In [10] M. Ramalatha et.al. Have not shown that which target FPGA they have used to design their modules so we have compared our proposed multiplier design with our conventional target FPGA, which we have used to make the overall design of ALU. So by this it can be concluded that our proposed algorithm, approach and platform are better than [10].

4. Synthesis and Simulation

1. RTL schematic of proposed 8 bit vedic multiplier:-



2. Simulation w/f of proposed 8 bit Vedic multiplier:-



5. Conclusion

We have proposed a new technique to design multiplication unit of FFT processor based on Vedic multiplier using unique addition tree structure, which gives better response in terms of speed in comparison to the conventional vedic multiplier hardware, Vedic multiplier with partitioning, Vedic multiplier with carry save adder, Modified Booth Wallace , Karatsuba, Vedic Karatsuba, Array, Booth, Wallace multiplier. And then this multiplier module has been put in the FFT processor along with conventional modules to achieve our goal of designing speed efficient FFT processor.

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