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High Performance CMOS Schimitt Trigger

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ABSTRACT

Portable electronic devices have extremely low power requirement to maximize the battery lifetime. Various device circuit architectural level techniques have been implemented to minimize the power consumption. Supply voltage scaling has significant impact on the overall power dissipation. With the supply voltage reduction, the dynamic power reduces quadratically while the leakage power reduces linearly (to the first order). However, as the supply voltage is reduced, the sensitivity of circuit parameters to process variations increases.

Keywords - Schmitt Trigger (ST), Micro Wind, V_{min}

I. INTRODUCTION

The Schmitt trigger circuit is widely used in analog and digital circuit as wave shaping circuit to solve the noise problem. Beside that this circuit is widely design in various styles in order to drive the load with fast switching low power dissipation and low-supply voltage.

Conventional Schmitt Trigger is shown in Figure 1 where the switching thresholds are dependent on the ratio of NMOS and PMOS. However this circuit will exhibit racing phenomena after the transition starts. Therefore in this paper we proposed CMOS Schmitt Trigger circuit which is capable to operate in low voltages (0.8V- 1.5V), less propagation delay and stable hysteresis width.

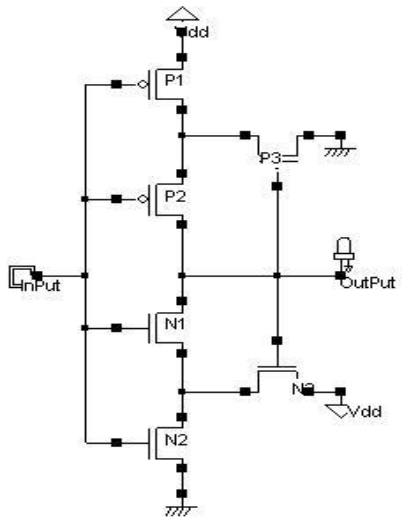

Figure 1.The Conventional Schmitt Trigger

II. CIRCUIT DESCRIPTION

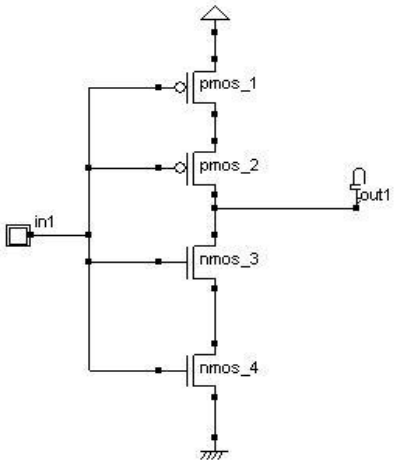

Figure 2. The Proposed Schmitt Trigger

The proposed Schmitt Trigger is shown in Figure 2. The proposed circuit is formed by a combination of two sub-circuits, P sub-circuit (which consist of P_1 and P_2) and N sub-circuit (which consist of N_1 and N_2). There is no direct connection between the source voltage and ground as P sub-circuit is connected to the path between the source voltage and output while the N sub- circuit is connected between the path of output and ground. Therefore, there is no static power consumption due to no direct path between source voltage and ground. Two PMOS ($P_1$and P_2) are formed by a parallel connection while two NMOS (N_1 and N_2) are formed by a series connection. By designing the PMOS in parallel, the resistance of the P sub-circuit will be reduced by halves. Thus, the propagation delay can be reduced as shown in equation (1).

$$t_P = 0.69\, RC_L = (t_{PHL} + t_{PLJH})/2 \quad (1)$$

It is preferably to reduce PMOS delay because delay is more concentrated to PMOS due to high mobility of PMOS compare to NMOS. The sizings of the transistor are set by locating the minimum component path of each sub-circuit. Each of the transistors is sized accordingly to their arrangement. For transistors that are in series, they are scaled by factor of 2 each while transistors in parallel are scaled by a factor of 1 each. The PMOS and NMOS ratio is set according to equation 2 with the effective length, L_{eff} = 0.30µ m (for 0.65 technology

$$(W|Leff)_{PMOS} = \gamma\, (W|Leff)_{NMOS} \quad (2)$$

It is recommended to widen the PMOS transistor to allow the resistance matches the pull down NMOS device. Typically, r = 3 → 3. Therefore, the ratio is set to be three to maximize the noise margin and to create a circuit with symmetrical voltage-transfer characteristic (VTC). By increasing the width of PMOS, it moves the switching threshold voltage towards V_{DD}, which makes the hysteresis width more rectangles which are desirable in a Schmitt Trigger design.

When the input is low, only the P sub-circuit will be considered and causes the output to be high (equal to V_{DD}). During this condition, both P_1 and P_2 are on (because VSG < |Vtp| source voltage and gate voltage is equal). Therefore, the output voltage is pull to V_{DD}. When the input increases to V_{DD}, N_1 and N_2 is turned on. Thus the output voltage is pull down to GND.

III. SIMULATION RESULTS

Three designs (1st, 2nd and 3rd Design) are simulated with 0.65 technology using Micro wind software. The 1st Design represent the Conventional Schmitt Trigger with the ratio of transistor is set according to 2nd Design represent the Conventional Schmitt Trigger with the ratio of transistor are set similarly with the 3rd Design which is the proposed Schmitt Trigger. The respective transistor dimensions for the three designs are shown in Table 1. The comparison are made in term of propagation delay, energy delay product and hysteresis width.

TABLE I. THE TRANSISTORS DIMENSION

(W/L_{eff})	1st Design	2nd Design	3rd Design
P1	2.40/0.30	1.80/0.30	0.90/0.30
P2	2.40/0.30	1.80/0.30	0.90/0.30
P3	0.30/0.30	0.90/0.30	0.90/0.30
N1	3.00/0.30	0.60/0.30	0.60/0.30
N2	3.00/0.30	0.60/0.30	0.60/0.30
N3	2.40/0.30	0.30/0.30	0.30/0.30

A. Propagation delay

The delay times of these circuits are measured as the average of the response time of the gate for positive and negative output transition for a square input waveform at 1GHz. As shown in Figure 3, the propagation delay will reduce when the source voltage is increased At lower source voltage (< 1.2V) and lower load capacitance (< 0.015pF), the 3rd Design has higher performance compared to the other two design. However, at higher supply voltage and larger load capacitance, the 1st Design gives better performances. The increasing of PMOS widths in 2nd and 3rd Design will improves t_{PLH} but will degrades t_{PHL} at the same time due to the increase of parasitic capacitance. This parasitic capacitance will be added into load capacitance and together will degrades the performance of the two designs.

B. Hysteresis width

Figure 4 show that the increasing of load capacitance will increase the hysteresis width (in small amount) for all three designs. Thus, the three designs are said to be stable at variation of load capacitance.

$$\Delta H = V_{TH} - V_{TL} \quad (4)$$

At V_{DD} = 0.8V, the 3rd Design has the highest hysteresis width followed by 2nd and 1st Design. While at V_{DD} > 0.8V, the 2nd Design has the widest hysteresis width and followed by 3rd and 1st Design. The decreased of hysteresis width for 1st and 3rd Design shows that the gap between the high- and low- threshold voltage is reduced as the source voltage increases. All the designs give a few mV hysteresis width, thus it is neither too wide nor too small for a Schmitt Trigger.

C. Energy-delay product

The Energy-Delay Product (EDP) is measured using equation (3) and theoretically EDP is directly proportional to Power-Delay Product (PDP) and propagation delay.

$$EDP = \left(\frac{1}{2} CLV2DD\right) t_P = PDP \times t_P \quad (3)$$

EDP also increases. The Proposed circuit give less EDP as low voltages (<1.2V) and low load capacitance (<0.015pF) due to less delay as discussed in section A. While at higher voltages (>1.0V) and high load capacitance (>0.010pF), the 1st Design gives the less EDP. As for the 2nd Design, it gives the highest EDP and thus is not preferably in a Schmitt Trigger.

IV. CONCLUSION

A new proposed CMOS Schmitt Trigger is presented which is capable to function under low voltages as much as 0.8V. The hysteresis width is clear and less sensitive to the variation of load capacitance and source voltages. Besides that, the proposed circuit gives less delay and Energy-Delay Product at low source voltage (< 1.2V).

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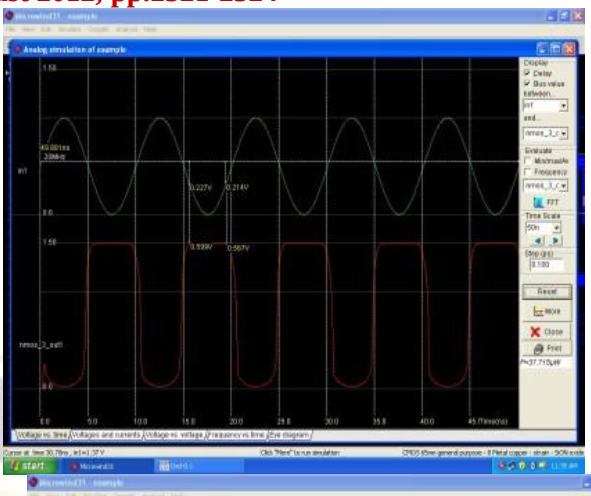
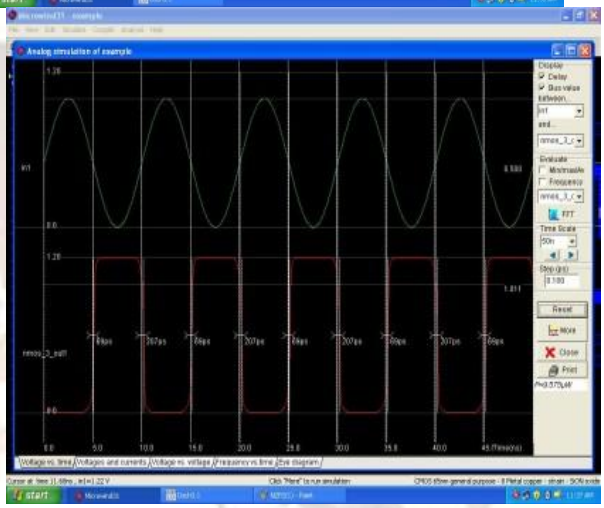
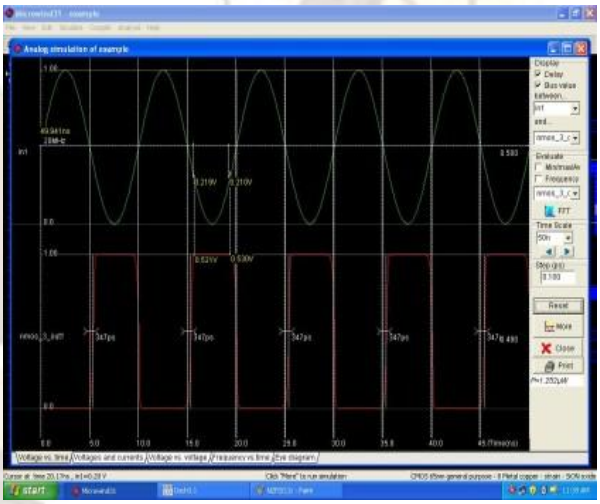
V. RESULTS

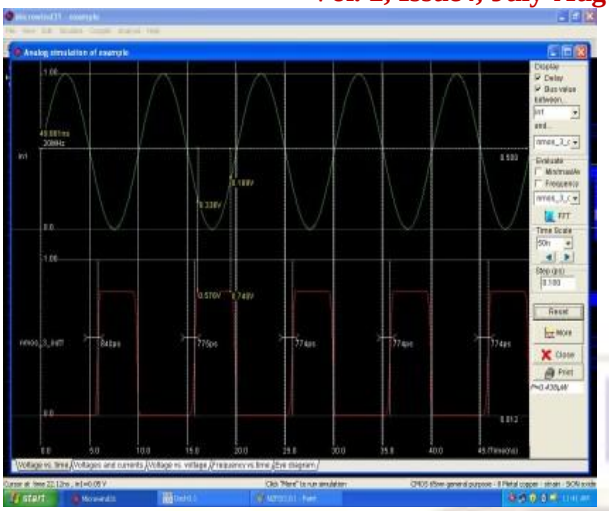
V_{DD}	Delay	Power for Design 1	Power for Design 2	Power for Design 3
0.8v	0.012ns	0.438µw	0.227µw	0.160µw
1.0v	0.012ns	1.252µw	0.560 µw	0.399µw
1.2v	0.012ns	9.575µw	4.246 µw	2.975µw
1.5v	0.012ns	37.715µw	18.062µw	12.136µw

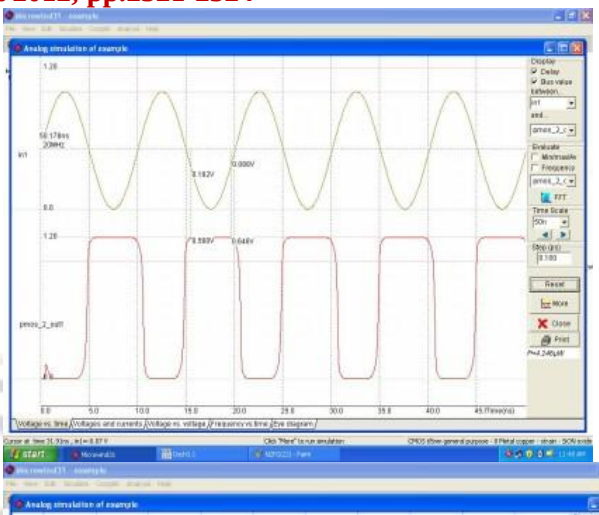
Simulation and Synthesis Results: Fig.2
Design 1:

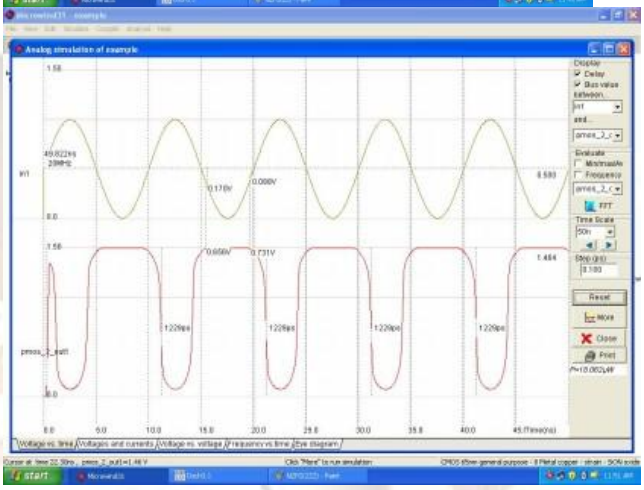




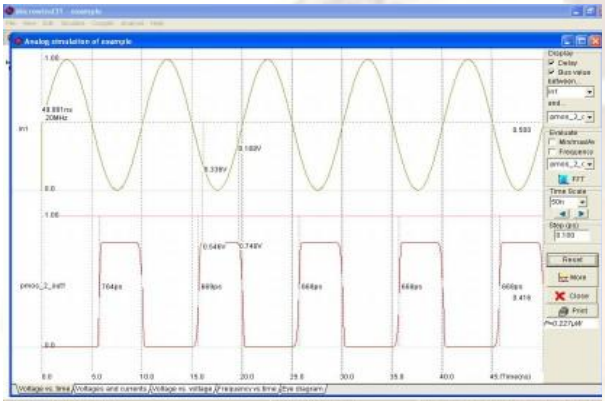


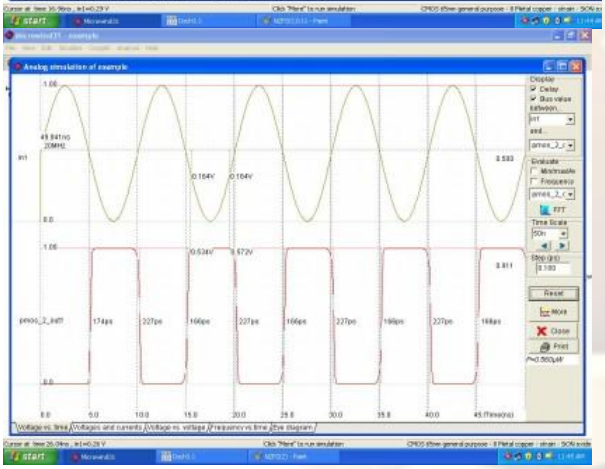






Design 2:





Design 3: