Deependra Singh Rajput, Manoj Kumar Yadav, Pooja Johri, Amit S. Rajput / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622
www.ijera.com Vol. 2, Issue4, July-August 2012, pp.2112-2117

SNM Analysis During Read Operation Of 7T SRAM Cells In 45nm Technology For Increase Cell Stability

Deependra Singh Rajput[*], Manoj Kumar Yadav[**], Pooja Johri[#], Amit S. Rajput[##]

[*](M.E. (CCN), MPCT, Gwalior, M.P. INDIA
[**] (M.TECH. (VLSI DESIGN), SRCEM, Banmore, Morena, M.P. INDIA
[#] (Assistant Professor, MPCT, Gwalior, M.P. INDIA
[##] (Assistant Professor, ITM, Gwalior, M.P. INDIA

ABSTRACT

In this paper, we propose a methodology to analyze the stability of a SRAM cell in the presence of random fluctuations in the device parameters. SRAM cell read stability are major concerns in CMOS technologies. Actually stability of SRAM cell only depends on the static noise margin (SNM), and SNM is effect the stability of SRAM cell during read operation of SRAM cells. So that SNM varies with each cell operation, a thorough analysis of SNM in read mode is required. In this paper we examine the 7T SRAM cell SNM during read operations analyzing various alternatives to improve cell stability during read operation. The techniques are based on word and bit-line voltage modulations, transistor width, and supply voltage. We show that it is possible to improve cell stability during read operations while varying in the transistor width and the word line voltage.

Index Terms— CMOS, 45nm, Static Noise Margin (SNM), 6T SRAM, 7T SRAM, Cell Ratio.

1.INTRODUCTION

Semiconductor memories, such as SRAMs, are widely used in electronic systems [6]. Now a day's we want a device which should be small as much as possible, for this we continue to scale down the device dimension, and for scaling continuously reduce supply voltage [7][8], but reduction in supply voltage gives unfavorable effect on SRAM cell performance because it reduces Static Noise Margin. Static Noise Margin is an important factor for stability and speed of SRAM cell. The SRAM cell stability depends on the different types of noise analysis. The pull up ratio and cell ratio are the two important parameter of SRAM cell because these are the only parameter change by the design engineer. Today's VLSI circuit designer has focused on lower supply voltage, but lower supply voltage can reduce the static noise margin and static noise margin is proportional to the performance of SRAM cell so performance of SRAM cell is also reduced. If increase in supply voltage, the value of SNM will be Increase with increase in leakage current, therefore VLSI designer has focused on such device which is good SNM and low leakage. The stability of a given SRAM cell is usually calculated by analyzing both its dynamic and static behavior during the typical operations: write, read and hold periods. According to this, the memory cell stability can be analysis from the Static Noise Margin analysis.

2. THE 6T SRAM CELL

2.1 6T SRAM Cell Structure

The conventional six-transistor (6T) SRAM consists of two cross coupled inverters and two NMOS access transistors, connecting the cell to the bit lines BL and BL_bar (Figure 1). The inverters are used as the storage element and the access transistors are used to communicate with the outside. The cell is symmetrical and has a relatively large area [1].

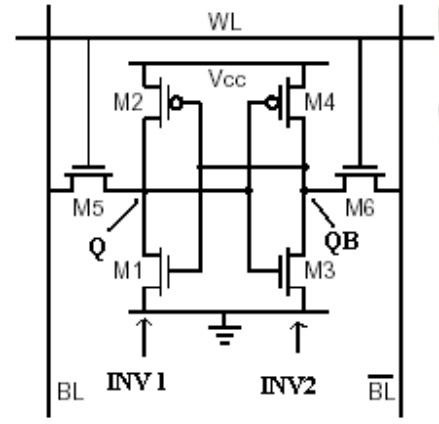

Fig. 1: Six-Transistor SRAM cell

2.2 Read Operation

Before the start of a read operation, the word line is held low (grounded) and the two bit lines connected to the cell through MOS transistors *M5* and *M6* (see figure 1) are pre charged high (to *VCC*). Since the gates of *M5* and *M6* are held low, these access transistors (M5 and M6) are off and the cross-coupled latch is disconnected from the bit lines. If a '0' is stored on the left storage node, the gates of the latch to the right are low. That means that transistor

M3 (see figure 1) is initially turned off. In the same way, *M2* will also be turned off initially since its gate is held high. This results in a simplified model, shown in figure 2, for reading a stored '0' [1].

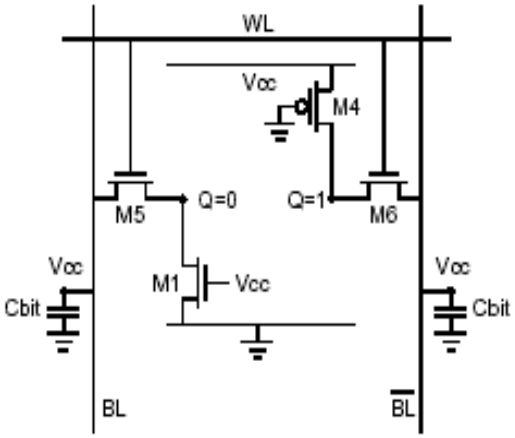

Fig. 2: Six-transistor SRAM cell at the read operation

If transistors *M*4 and *M*6 are properly sized, then the cell is flipped and its data is effectively overwritten. A statistical measure of SRAM cell write ability is defined as write margin. Write margin is defined as "the minimum bit line voltage required to flip the state of an SRAM cell". The write margin value and variation is a function of the cell design, SRAM array size and process variation [1].

2.3 Write Operation

The write operation is similar to a reset operation of an SR latch [10].For a standard 6T SRAM cell, writing is done by lowering one of the Bit-line to ground while asserting the word-line. To write a '0' BL is lowered, while writing a '1' BL to be lowered [1].

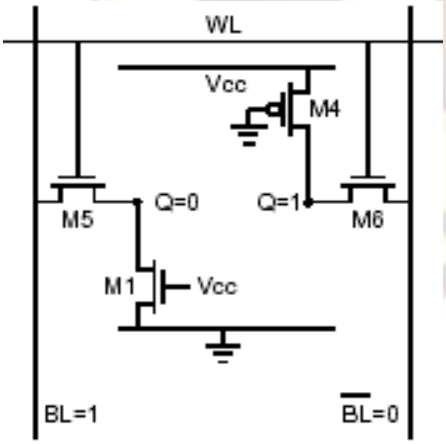

Fig. 3: Six-transistor SRAM cell at the write operation

3. STATIC NOISE MARGIN

The SNM is defined as the "maximum amount of noise voltage that can be introduced at the output of the two inverters, such that the cell retains its data". SNM calculate the amount of noise voltage required at the internal nodes of the SRAM cell to flip the cell's data[5][9]. SNM can be calculated by the use of butter fly curve method. Figure 4 shows the most common way of representing the SNM graphically for a bit cell holding data. The Figure 4 plots the voltage transfer characteristic (VTC) of Inverter 2 from Figure 1 and the inverse VTC from Inverter 1. The resulting two-lobed curve is called a "butterfly curve" and is used to determine the SNM. The SNM is defined as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve. To understand why this definition holds, consider the case when the value increases from 0. On the plot, this causes the Inverter 1 in the Figure 4 to move downward and the VTC for Inverter 2 to move to the right. Once they both move by the SNM value, the curves meet at only two points. Any further noise flips the cell (Read SNM) [1][4].

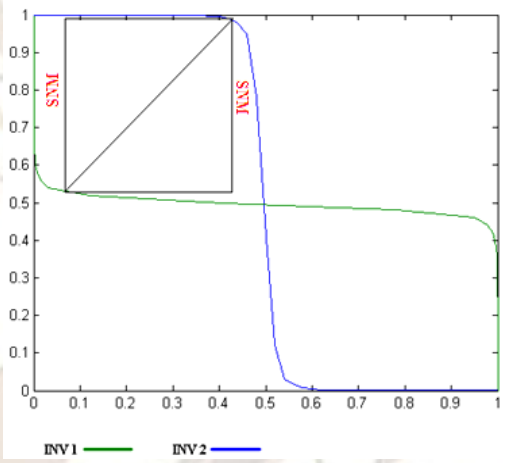

Fig. 4:"Butterfly" curve measuring SNM.

4. 7T SRAM CELL

The circuit of 7T SRAM cell consists of two CMOS inverters that connected to the cross coupled to each other with additional NMOS transistor which connected to write line (W) and having two pass NMOS transistors connected to bit lines (BL) and bit-lines bar (BL_bar) respectively. Figure 5 shows circuit of 7T SRAM Cell, where the access transistor N3 is connected to the word-line (WL) to perform the access write and N4 is connected to the Read-line (R) to perform the read operations. Bit-lines act as I/O nodes carrying the data from SRAM cells to a sense amplifier during read operation, or from write in the memory cells during write operations. The proposed

7T SRAM cell depends on cutting off the feedback connection between the two inverters, *inv1* and *inv2*, before a write operation. The feedback connection and disconnection is performed by an extra NMOS transistor N5 and the cell only depends on BL _bar to perform a write operation [3].

4.1 Write Operation

The write operation of 7T SRAM cell starts by turning N5 off this cut off the feedback connection. BL bar carries complement of the input data, N3 is turned on, while is N4 off as shown in Figure 6 (a).This types of 7T SRAM cell looks like two cascaded inverters connected in series,inv2 followed

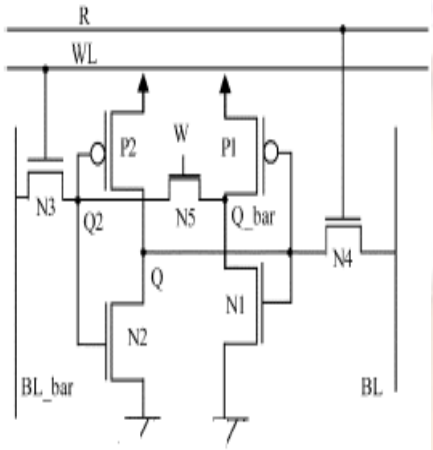

Fig. 5: 7T SRAM cell

by inv1, as shown in Figure 6 (b). N3 transistor transfers the data from BL_ bar to which drives *inv2*, P2 and N2, to develop Q, the cell data. Similarly, Q drives inv1, P1 and N1, to develop Q _bar which equals Q2 if data is "0" and lightly higher than Q2 if data is "1." Then, Word Line is turned off and N5 is turned on to reconnect the feedback connection between the two inverters to stably store the new data. Both bit line (BL and BL_bar) are pre-charged "high." By the use of proposed write scheme, BL _bar is kept "high" to write "0" with negligible power consumption and careful transistor sizing is essential to guarantee a stable write "0". To store "1" in the cell, BL _bar is discharged to "0". To store a "0" in the cell, there is no need to discharge bit line (BL _bar) and therefore, the activity factor of discharging bit line BL_bar is less than '1' and depends on the percentage of writing "1"[3].

4.2 Read Operation

In the read operation of 7T SRAM cell, both word line (WL) and read signal R are turned on, while transistor N5 is kept on. When Q = '0', the read path consists of transistor N2 and N4, as shown in Figure 7 (a), and it behaves like a conventional 6T cell.

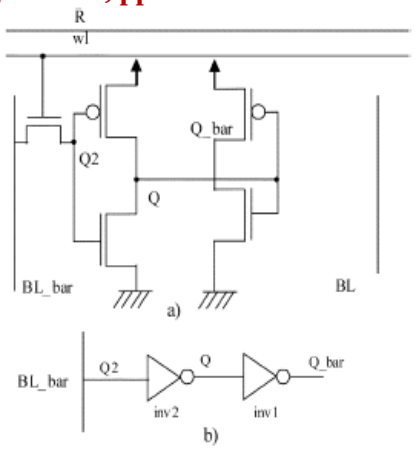

Fig. 6: (a) 7T SRAM cell during write operation (b) Equivalent circuit of 7T SRAM cell

When Q = '1', the read path consists of transistor N1, N5 and N3, which represents a read path as shown in Figure 7 (b). In this, the three transistors are connected in series, which reduces the driving capability of the cell unless these transistors are carefully sized [3].

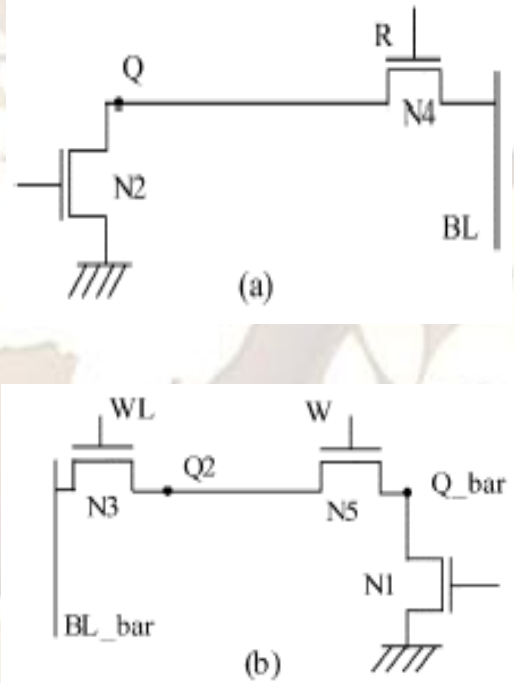

Fig. 7: (a) 7T SRAM cell during read operation (b) Equivalent circuit of 7T SRAM cell

5. SNM DEPENDENCE

Stability of 7T SRAM cell depends on the SNM; the factors are supply voltage, temperature, doping variations & transistor sizing etc. This section explores the different parameters on which the SNM is dependent.

5.1 Supply voltage (V_{CC})

Power supply voltage modulation is an important parameter which changes the stability of SRAM cell, actually Static Noise Margin of SRAM cell also depends on power supply (V_{CC}), during read and write mode and has been widely accepted in nanometer technologies. When we increase the value of power supply (V_{CC}), the value of SNM linearly increase with the increases in leakage current. Figure 8 shows the relationship between power supply voltage and SNM during read mode. It is clear from figure 8 the power supply voltage increases during read operation is suitable and SNM is also increase for all cases [4].

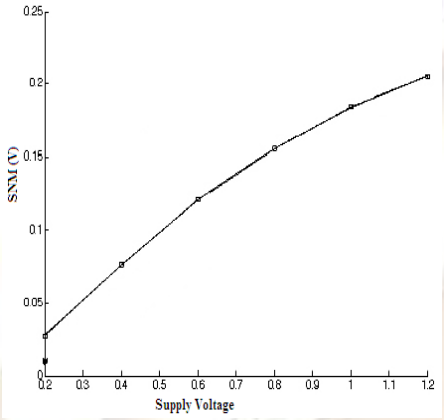

Fig. 8: SNM versus V_{CC} Curve [2]

5.2 Bit line voltage

Bit-line voltage modulation is observed to calculate the requirement of pre-charging bit-lines at the full power supply voltage. Figure 9 shows the relationship between the SNM and the bit-line voltage. Figure 9 shows that the SNM can be slightly improved by decreasing the bit-line voltage compare to V_{CC} during read operations. This technique increases the cell stability and is suitable with the voltage modulation. The reduced bit-line voltage move may allow for a read-mode SNM improve without need of any modification of the SRAM cell array design [4].

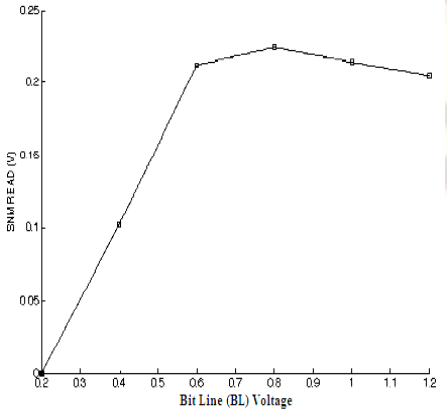

Fig. 9: SNM versus Bit line voltage [2]

5.3 Word line voltage

The word-line voltage modulation is another technique to improve the stability of cell at low power supply voltage levels suitable with recommended cell layout ($\alpha \approx \beta \approx 3$). This technique is based on minimizing the maximum voltage swing of the word-line to sustain the cell access transistor during the read operations [4].

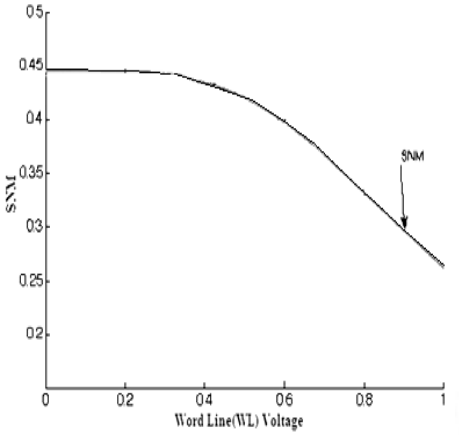

Fig. 10: SNM versus Word line voltage [2]

Figure 10 shows the connection between the SNM and the word-line voltage. As shown in Figure 10 the SNM can be improved by reducing the word-line voltage during read operations with respect to V_{CC}. This approach may allow a generous improvement of SNM.

Table: 1. Examples of SNM_{READ} improvement with lower Word Line voltage

Technology	Word Line Voltage (WL)	SNM_{READ} (v)
45 nm	1	0.2340v
	0.9	0.2662v
	0.8	0.3081v

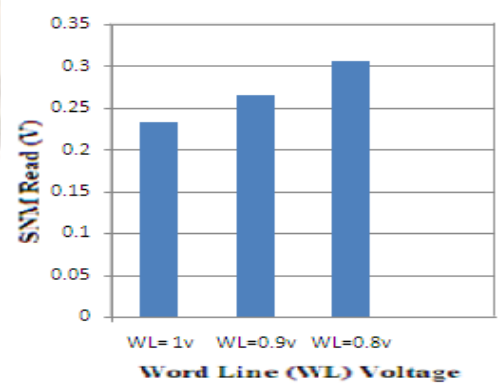

Fig. 11: SNM Vs WL

We can prove that from Table 1 and graph (above) at 45 nm technology, SNM can be improved by reducing the word-line voltage during read operations with respect to $V_{CC.}$

5.4 Cell ratio

Cell ratio is the ratio between sizes of the driver transistor to the load transistor during read operation [4]. The cell ratio of SRAM cell is given by-

$CR = (W/L)_{M5} / (W/L)_{M1}$ (During read mode)

If we make changes in the Cell Ratio, then the size of the driver transistor will also increase and current of SRAM cell will be change (increases). As current increases, then we got different speed of the SRAM cell. For different values of CR, we got different values of SNM. This is shown in table 2.

Table: 2. SNM_{READ} improvement with increases Cell ratio

Technology	Cell Ratio(CR)	SNM_{READ} (v)
45 nm	1	0.1970v
	2	0.2180v
	3	0.2340v

We can prove that from Table 2 and graph (below) at 45 nm technology, SNM can be improved by increasing in the cell size of transistor during read operations.

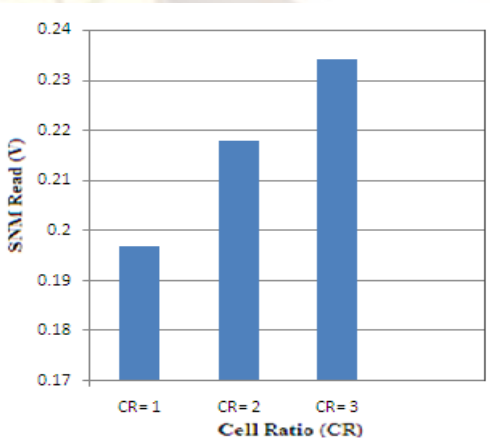

Fig.12: SNM Vs CR

6. SIMULATION AND RESULT

To improve the read stability of SRAM cell, three basic voltage signals are required Power supply voltage, Bit-line voltage and Word-line voltage. When supply voltage is increased, the value of SNM increases but there is a probability of increase in the leakage current. To decrease the possibility of leakage current, we use voltage modulation scheme such as Bit line voltage modulation, Word line voltage modulation, Transistor width modulation, with the help of the voltage modulation combination, reducing in leakage current with improved in static Noise Margin. From the above analysis, for increasing SNM and stability of SRAM cell, supply voltage should take maximum, word line voltage keep as minimum as possible, bit line voltage should take maximum but below to supply voltage (Vcc) and cell ratio keep as maximum as possible, so that with the increasing SNM, the stability of SRAM cell will also be increased.

SNM calculation: We have done the SNM calculation by this way with respect to above butterfly curve:

SNM = 'Maximum Side of the square'.
Maximum side of the Square = Maximum lengths of diagonal of Square / √ 2.
So, SNM = Maximum length of diagonal of square / √ 2.

EXAMPLE: This is the graphical method of SNM calculation. We evaluate the maximum length of diagonal of Butter Fly curve, after that for the calculation of Static Noise Margin, divide this maximum length of diagonal by √ 2. This is shown in figure 13. Assume a square into the BUTTER FLY curve.

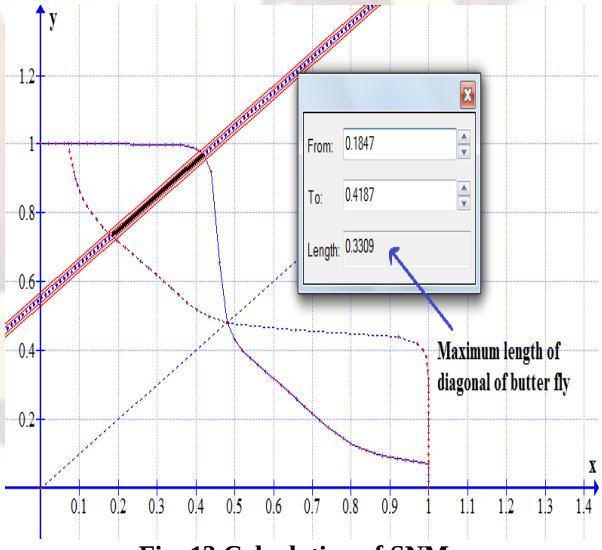

Fig. 13 Calculation of SNM

SNM = Maximum length of diagonal /√ 2
So, SNM = 0.3309 / √ 2
SNM = 0.2340 V.
or SNM = 234 mV.

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