Santosh A, Shivashankar Tallada / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue4, July-August 2012, pp.2043-2050

Simulation Of High-Efficiency AC/DC Converter For Power Factor Correction

Santosh A and Shivashankar Tallada

Abstract

This paper presents a novel input current shaper based on a quasi-active power factor correction (PFC) scheme. The PFC cell is formed by connecting the energy buffer (L_B) and an auxiliary winding (L_3) coupled to the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. The input inductor L_B operates in discontinuous current mode such that a lower total harmonic distortion of the input current can be achieved. It eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher efficiency. Operating principles, analysis, and experimental results of the proposed method are presented.

Keywords---AC/DC converters, power factor correction (PFC), single stage, Flyback converter.

I. INTRODUCTION

Most electronic equipment is supplied by 50/60 Hz utility power, and more than 50% of power is processed through some kind of power converters. Conventionally, most of the power conversion equipment employs either diode rectifier or thyristor rectifier with a bulk capacitor to converter AC voltage to DC voltage before processing it. Such rectifiers produce input current with rich harmonic content, which pollute the power system and the utility lines. Power quality is becoming a major concern for many electrical users.

To measure the quality of input power of electrical equipment, power factor is a widely used term. The power factor of an off-line equipment is defined as the product of two components: the displacement factor *cos*ϕ, which is caused by the phase difference between the fundamental component of the input current and the sinusoidal input voltage, and the distortion factor, which can be presented by the total-harmonic-distortion (THD) of the input current. In fact, the greatest concern of the off-line rectifier's impact on the power system is not the displacement between the voltage and current, but the input current distortion and current harmonics, since they pollute the power system and causes interference among off-line utilities. To limit the input current Harmonics drawn by the off-line equipment, several international regulations, such as the IEC 61000-3-2 and its corresponding Japanese regulation, have been proposed and just enforced.

To comply with the line harmonics standards, a variety of passive and active PFC techniques have been proposed. The passive techniques normally use a simple line-frequency LC filter to both extend the current conduction angle and reduce the THD of the input current of the diode-capacitor rectifier. Due to its simplicity, the passive LC filter could be the high-efficiency and low-cost PFC solution to meet the IEC 61000-3-2 class D specifications in the low power range. However, the passive LC filter has a major drawback, which is its heavy and bulky low-frequency filter inductor.

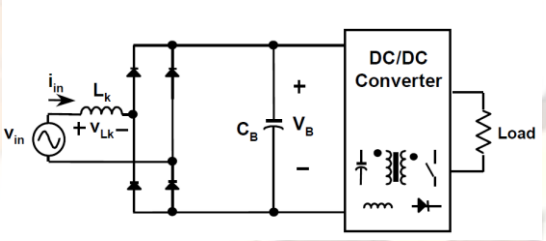

Fig.1. Circuit diagram of the conventional diode-capacitor rectifier

To reduce the size and weight of the filter inductor, the active PFC techniques have been introduced. In an active PFC converter, the filter inductor "sees" the switching frequency, which is normally in the 10 kHz to hundreds of kHz range. Therefore, the size and weight of the power converter can be significantly reduced by using a high-frequency inductor. The cost of the active PFC approach can also be lower than that of the passive filter approach if the conversion power increases. The most popular implementation of active PFC is to insert a PFC power stage into the existing equipment to satisfy the regulation. This is referred as the two-stage PFC approach. However, the converter cost and complexity increases with the increased component count.

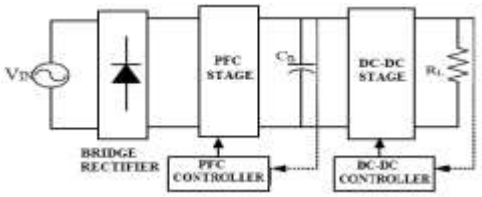

Fig.2.Functional block diagram of two stage

The two-stage scheme results in high power factor and fast response output voltage by using two independent controllers and optimized power stages. The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications. In order to reduce the cost, the single-stage approach, which integrates the PFC stage with a dc/dc converter into one stage, is developed. These integrated single-stage power factor correction (PFC) converters - usually use a boost converter to achieve PFC with discontinuous current mode (DCM) operation. Usually, the DCM operation gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode (CCM). However, the CCM operation yields slightly higher efficiency compared to the DCM operation.

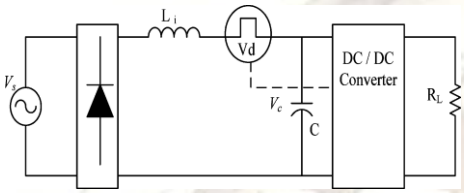

Fig.3. General Circuit diagram of single stage conversion.

Generally, single-stage PFC converters meet the regulatory requirements regarding the input current harmonics, but they do not improve the power factor and reduce the THD as much as their conventional two-stage counterpart. The power factor could be as low as 0.8, however, they still meet the regulation. In addition, although the single-stage scheme is especially attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and high as well as wide-range intermediate dc bus voltage stress .

To solve the input current harmonics problem in a single-stage, the "dither-rectifier" concept was introduced with the conceptual Single Stage PFC structure in Fig. 3, in which, a high frequency "dither source" is between the input boost inductor L_B and the bulk energy-storage capacitor C_B. As shown in Fig. 3, the dither source introduces high-frequency pulsating voltage on L_B during line cycle; therefore, the rectifier diode can conduct current even while the instantaneous input line voltage is much lower than the capacitor voltage V_B. As a result, the input current conduction angle is significantly enlarged and the input current harmonics are reduced. However, the harmonic content can meet the regulatory standard by a small margin and also the "dither" concept does not specify the switch duty-cycle to be constant.

In this, a new concept of quasi-active PFC is proposed to improve the efficiency of a single-stage converter by preventing the input current or voltage stress due the PFC cell from being added to the active switch. In this circuit, the dc/dc cell operates in DCM so that a series of discontinuous pulses is used to shape the input inductor current and the PFC is achieved. As the circuit uses resonance of circuit parameters to achieve PFC, the control of the power factor will be very sensitive to the variation of components values.

II. PROPOSED QUASI-ACTIVE PFC CIRCUIT

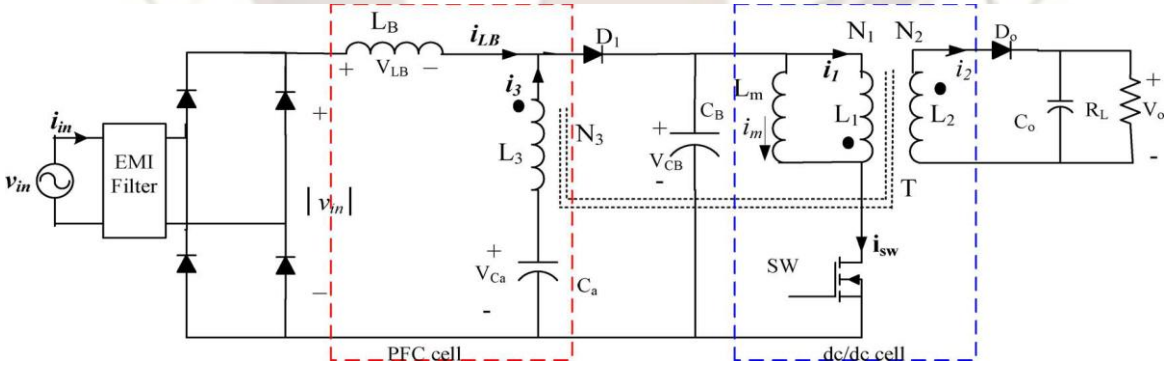

Fig.4.Proposed single stage PFC circuit diagram

The proposed quasi-active PFC circuit is analyzed in this section. As shown in Fig. 4, the circuit comprised of a bridge rectifier, a boost inductor L_B , a bulk capacitor C_a in series with the auxiliary windings L_3 , an intermediate dc-bus voltage capacitor C_B , and a discontinuous input current power load, such as flyback converter. The flyback transformer (T) has three windings $N1$,$N2$, and $N3$. The secondary winding $N2$ = 1 is assumed. In the proposed PFC scheme, the dc/dc converter section offers a driving power with high-frequency pulsating source. The quasi active PFC cell can be considered one power stage but without an active switch.

To simplify the analysis, the following assumptions have been made.

1) All semiconductors components are ideal. According to this assumption, the primary switch and the rectifiers do not have parasitic capacitances and represent ideal short and open circuits in their ON and OFF states, respectively.

2) The power transformer does not have the leakage inductances because of the ideal coupling.

3) All the capacitors are high enough so that the voltage across them is considered constant.

4) Finally, the input voltage of the converter is considered constant during a switching cycle because the switching frequency is much higher than the line frequency.

A. Principles of Operation of the Proposed Circuit

To facilitate the analysis of operation, Fig. 5(a) and (b) shows the topological stages and the key waveforms of the proposed circuit. It is assumed that both the input inductor L_B and the magnetizing inductance of the flyback converter operate in DCM. Therefore, currents i_{LB} , i_m, and i_2 are zero at the beginning of each switching period. It is also assumed that the average capacitor voltage V_{Ca} is greater than the average rectified input voltage $|v_{in}|$. To ensure proper operation of the converter, the transformer's turns ratio should be $(N1/N3) \geq 2$ and the boost inductor $L_B < L_m$. In steady-state operation, the topology can be divided into four operating stages.

1) Stage 1 *(to − t1):* When the switch (SW) is turned on at $t = to$, diodes D_1 and Do are OFF, therefore, the dc-bus voltage VCB is applied to the magnetizing inductor L_m, which causes the magnetizing current to linearly increases. This current can be expressed as

$$i_m = \frac{V_{CB}}{L_m}(t_o - t_1). \quad (1)$$

And since diode D_1 is OFF, the input inductor L_B is charged by input voltage, therefore, the inductor current i_{LB} is linearly increased from zero since it is assumed that the PFC cell operates in DCM. This current can be expressed as

$$i_{LB} = \frac{|V_{in}| + (N_3/N_1)V_{CB} - V_{Ca}}{L_B}(t_o - t_1) \quad (2)$$

Where, $V_{in} = V_m|\sin\theta|$ is the rectified input voltage, $(to - t_1) = dT_S$ is the ON-time of the switch (SW), L_B is the boost inductor and $N1$, $N3$ are the primary and auxiliary turns ratio, respectively. At this stage, $i_{LB} = -i3$ and the capacitor C_a is in the charging mode. On the other hand, Do is reversed biased and there is no current flow through the secondary winding. Since the transformer is assumed ideal, based on Ampere's law, it has

$$N_1 i_1 + N_2 i_2 - N_3 i_{LB} = 0$$

Where $i2 = 0$ at this stage therefore,

$$i_1 = \frac{N_3}{N_1} i_{LB} = -\frac{N_3}{N_1} i_3. \quad (3)$$

Thus

$$i_m = i_{CB} - i_1 = i_{CB} + \frac{N_3}{N_1} i_3. \quad (4)$$

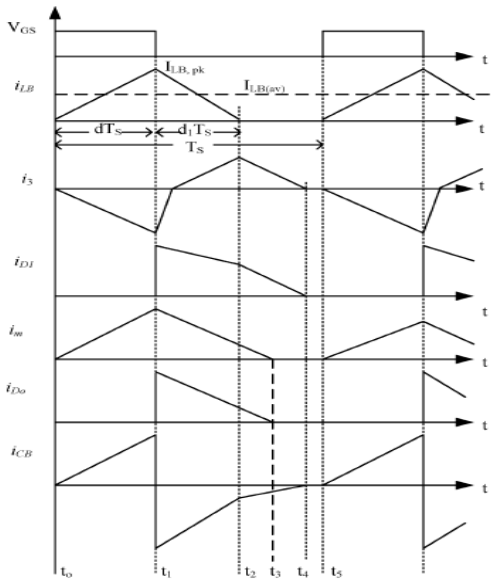

Fig. 5. (a) Key switching waveforms of the proposed PFC.

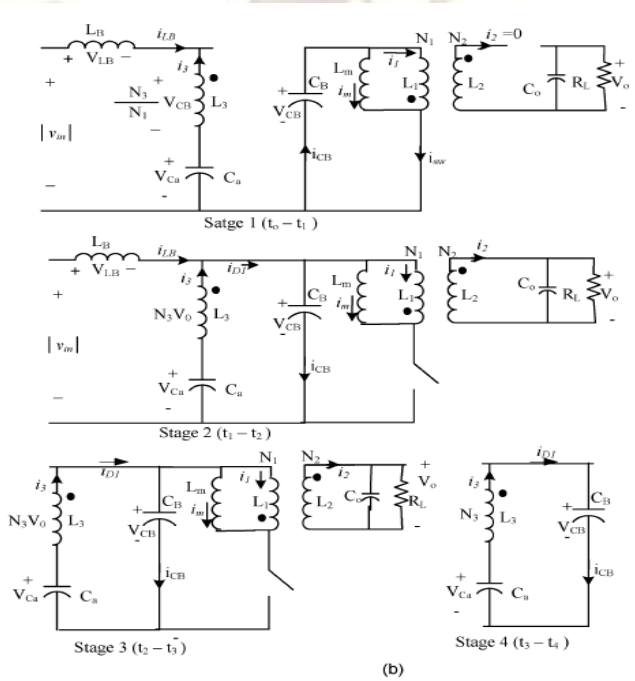

Fig. 5. (b) Equivalent circuit operation stages of the proposed PFC circuit during one switching period

Therefore, from (4) it can be seen that the magnetizing current i_m is supplied by the discharging current from the dc bus capacitor C_B and the current i_3 which is equal to input current i_{LB} at this stage. The current through the main switch (SW) is given by

$$i_{\mathrm{SW}} = i_{CB} = i_m - \frac{N_3}{N_1} i_3 = i_m + \frac{N_3}{N_1} i_{LB}. \quad (5)$$

Therefore, the current stress of the switch can be reduced by selecting the turns ratio ($N3/N1$), which is designed to be less than 1 to ensure proper operation of the transformer. Compared to the single-stage BIFRED converter, the switch current is given by

$$i_{\mathrm{SW}} = i_m + i_{LB}. \quad (6)$$

Obviously, the proposed circuit has less switch current stress, therefore, the conduction loss and switching losses are reduced, and the efficiency is improved correspondingly. This stage ends when the switch is turned off at $t = t_1$.

2) Stage 2 ($t_1 - t_2$): When the switch is turned OFF at $t = t1$, output diode *Do* begins to be forward biased. Therefore, the energy stored in the transformer magnetizing inductor is delivered to the load through the secondary winding. Similarly, the diode D_1 is also forward biased and the voltage across L_B now $V_{\mathrm{in}} - V_{CB}$. Therefore, the current I_{LB} is linearly decreased to zero at $t = t_2$ (DCM operation), and the energy stored in L_B is delivered to the dc bus capacitor C_B . Therefore

$$i_{LB} = \frac{|V_{\mathrm{in}}| - V_{CB}}{L_B}(t_1 - t_2). \quad (7)$$

The capacitor (C_a) is also discharging its energy to the dc bus capacitor C_B and the current i_3 reverse its direction. Therefore, the capacitor current is given by

$$i_{D_1} = i_{CB} = i_{LB} + i_3. \quad (8)$$

3) Stage 3 *($t_2 - t_3$):* At this stage, the input inductor current i_{LB} reaches zero and the capacitor C_a continues to discharge its energy to the dc bus capacitor C_B . Therefore, $i_{D1} = i_{CB} = i_3$. At $t = t_3$, the magnetizing inductor releases all its energy to the load and the currents i_m and i_2 reach to zero level because a DCM operation is assumed.

4) Stage 4 *($t_3 - t_4$):* This stage starts when the currents i_m and i_2 reach to zero. Diode D_1 still forward biased, therefore, the capacitor C_a still releasing its energy to the dc bus capacitor C_B . This stage ends when the capacitor C_a is completely discharged and current i_3 reaches zero. At $t = t_5$, the switch is turned on again to repeat the switching cycle.

B. Steady-State Analysis

The voltage conversion ratio of the proposed converter can be estimated from the volt-second balance on the inductors and the input–output power balance as explained in the following. From the volt-second balance on L_B

$$\left(V_{\mathrm{in}} + \frac{N_3}{N_1} V_{CB} - V_{Ca}\right) dT_S = (V_{CB} - V_{\mathrm{in}})\, d_1 T_S \quad (9)$$

Where d_1 is the OFF-time of the switch (SW). Therefore, d_1 could be given by

$$d_1 = \frac{V_{\mathrm{in}} + (N_3/N_1) V_{CB} - V_{Ca}}{V_{CB} - V_{\mathrm{in}}} d. \quad (10)$$

From Fig. 4(a), the average current of the boost inductor in a switching cycle is given by

$$I_{\mathrm{in}} = I_{LB,\mathrm{av}} = \frac{i_{LB,\mathrm{peak}}}{2}(d + d_1) T_S. \quad (11)$$

Substituting for i_{LB},peak given in (2) and using (10), the average input current is given by

$$I_{\mathrm{in}} = \frac{V_{\mathrm{in}} + (N_3/N_1) V_{CB} - V_{Ca}}{2L_B} d^2 T_S \times \left(\frac{(1 + N_3/N_1) V_{CB} - V_{Ca}}{V_{CB} - V_{\mathrm{in}}}\right). \quad (12)$$

Based on (12) for a given input voltage, Fig. 6(a) shows the normalized input current waveform for a half cycle for a change in the turns ratio $N3/N1$. It can be seen that to reduce the dead time and improve the power factor of the input current the turn's ratio must be ≥0.5. Similarly, Fig. 6(b) shows the normalized input current waveform for a change in dc bus capacitor voltage V_{CB}. As it can be seen that the higher the V_{CB} the better quality of the input current waveform (lower THD). However, higher V_{CB} means higher voltage stress on the power switch (SW), which can reduce the efficiency of the converter. Therefore, a tradeoff between THD and efficiency must be made. The energy absorbed by the circuit from the source during a half switching cycle is given by

$$P_{\mathrm{in}} = \frac{1}{\pi} \int_0^{\pi} V_m \sin(t) I_{\mathrm{in}}\, dt.$$

Substitution for I_{in} in given (12) yields

$$P_{\mathrm{in}} = \frac{1}{\pi} \frac{V_m}{2L_B} d^2 T_S(A) \int_0^{\pi} \sin(t) B\, dt \quad (13)$$

Where

$$A = \left[\left(1 + \frac{N_3}{N_1}\right) V_{CB} - V_{Ca}\right],$$

$$B = \frac{V_m \sin(t) + (N_3/N_1) V_{CB} - V_{Ca}}{V_{CB} - V_m \sin(t)}.$$

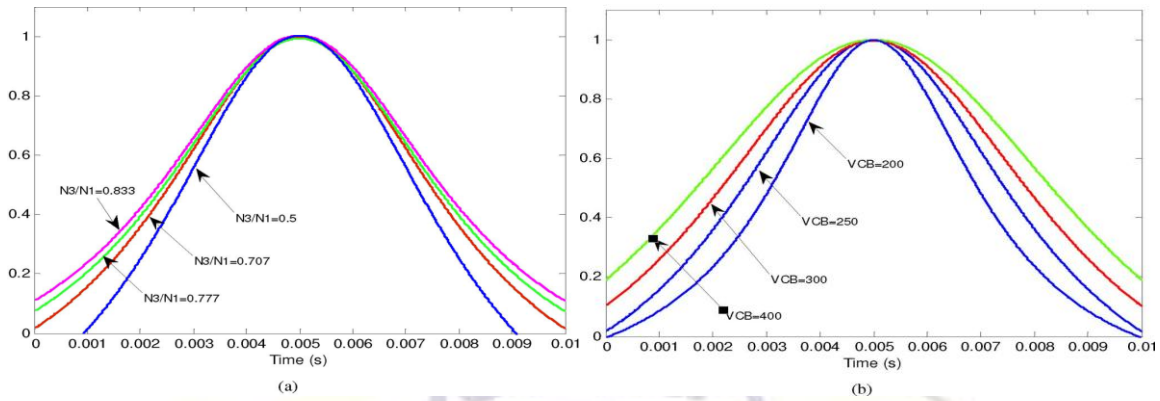

Fig. 6. Normalized input current waveform in half cycle for a change in (a) turns ratio *N3/N1* and (b) bus capacitor voltage V_{CB}

The average output power for a DCM flyback converter is given by

$$P_o = \frac{V_{CB}^2}{2L_m} d^2 T_S. \tag{14}$$

Assume 100% efficiency, *P*in = *Po* , yields

$$V_{CB}^2 = \frac{V_m}{\pi} \frac{L_m}{L_B} (A) \int_0^{\pi} \sin(t) B dt. \tag{15}$$

Equation (15) shows that the dc bus capacitor is independent of load variation; V_{CB} is determined by the input voltage and circuit parameters L_m/L_B,*N3/N1* . Note that, (15) is transcendental and can only be solved by numerical method using specific circuit parameters.

III. SIMULATION RESULTS AND EXPERIMENTAL VERIFICATION

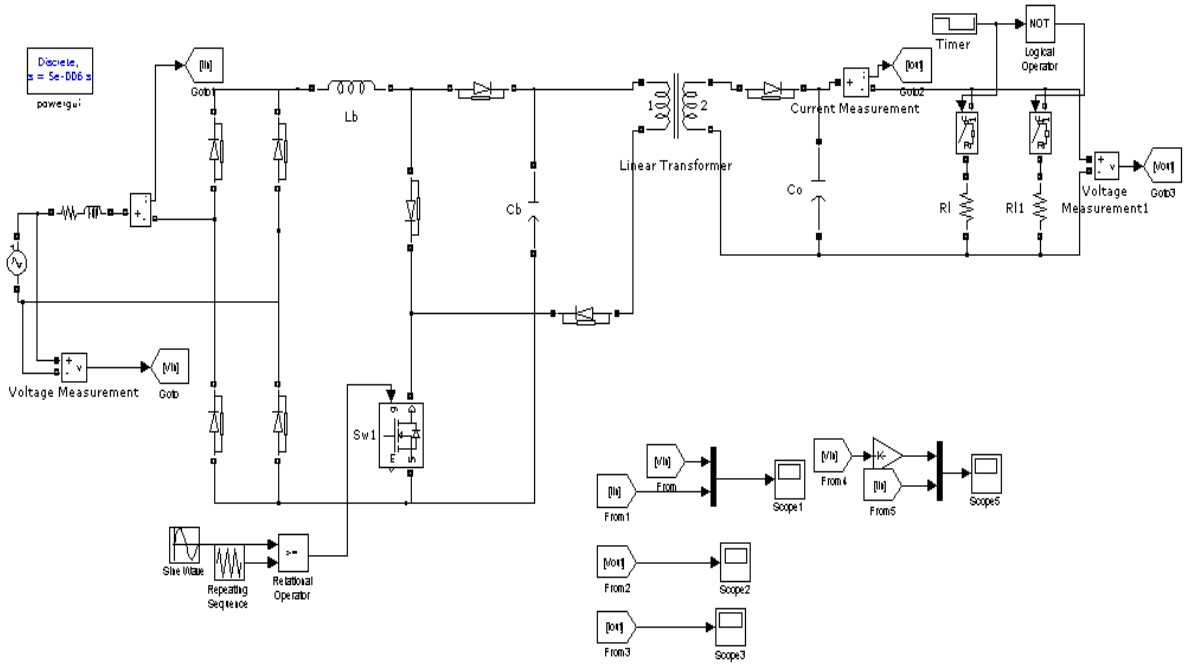

Fig. 7. Simulation of proposed circuit

In order to verify the proposed concept, a prototype of the converter shown in Fig. 4 was constructed as fig 7 by using MATLAB Simulation and experimentally tested. To ensure proper operation of the converter, the dc bus voltage (*VCB*) must be higher than the input voltage, such that the diode D_1 is OFF and the inductor L_B stores energy when the switch (SW) is ON. Therefore, from (15) the inductor L_m must be higher than the input inductor L_B. The DCM fly back converter was designed and implemented for 50 V/80 W output, V_{in},rms (100–240 V) universal line voltage, and overall efficiency of 86% is assumed. The switching frequency is selected to be 100 kHz and the maximum duty cycle of is 0.45. The major components of the circuit are follows: transformer turns ratio ($N1$ = 30,$N2$ = 10,$N3$ = 15) with core ETD34, L_m = 200 μH, LB = 80 μH, C_B = 47 μF, C_a = 22 μF, C_o = 470 μF, the switch SW (SPW22N60), the bridge rectifier and diodes D_1,Do using MUR1560. Fig. 8 shows the measured input voltage and filtered input current waveforms for a 100 V_{ac} input voltage at full load. As it may be seen from Figs. 6 (a),(b) and 8, that selecting the turns ratio $N3/N1$ and the dc bus voltage V_{CB} can be optimized in order to reduce the dead time and improve the quality of the input current.

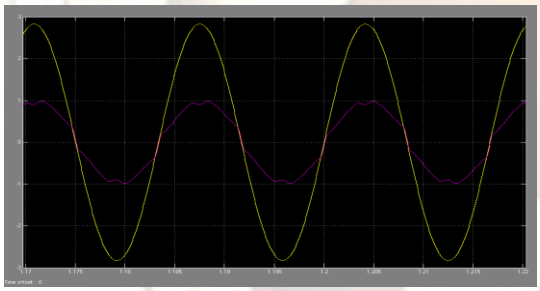

Fig. 8. Measured input voltage and filtered input current at full load (THD = 8.2%).

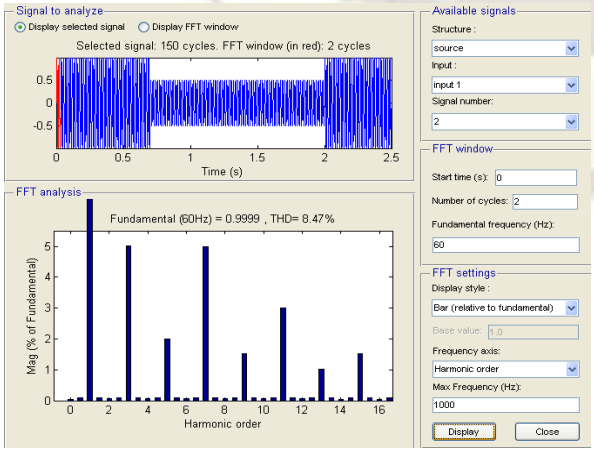

Fig. 9.Measured harmonics content of the input current.

Fig. 9 shows the measured harmonic content of the input current compared to the Classes A and D regulation standards. Note that, in order to improve the visibility of the higher order harmonics, class A limits are scaled down by a factor of 5 (class A limits/5). The measured THD = 7% and the power factor is 0.997. Obviously, the input current is much closer to the sinusoidal waveform and it meets the regulation standards. Fig. 10 shows the transient response of the converter for a step change of load between 50% and 100%. It may be seen that a fast dynamic response has been obtained.

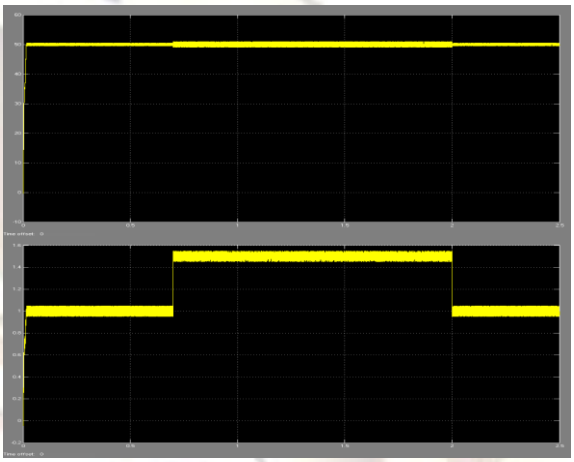

Fig. 10. The transient response of the converter for a step change of load between 50% and 100%.

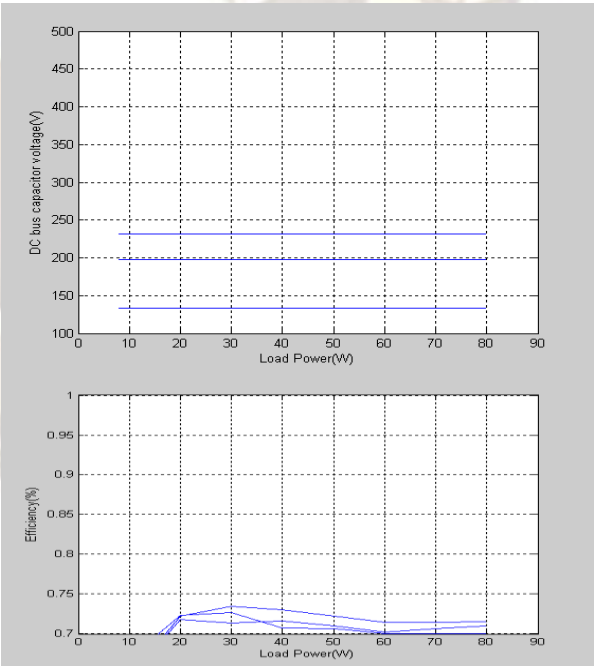

Fig. 11. Measured dc bus capacitor voltage and efficiency versus load power for a range of input voltage.

Fig. 11 shows the measured dc bus voltage V_{CB} and efficiency of the converter for range of load and input voltage variation. It may be seen that the capacitor voltage can be maintained below 450 V by properly designing the turns ratio $N3/N1$ and the inductors ratio L_m/L_B.

Furthermore, the proposed converter can maintains 90% efficiency or above at high load. Finally, Table I summarizes the comparison between conventional single-stage boost-flyback converter and the proposed converter in terms of circuit construction and performance. It may be seen, that the proposed converter presents a high quality input current with THD <10% and high efficiency. However, the proposed converter has additional winding $N3$ in series with capacitor (Ca), but they are small in size since $N3$ operate at the converter switching frequency.

TABLE I :
COMPARISON BETWEEN THE CONVENTIONAL BOOST + FLYBACK AND THE PROPOSED PFC CIRCUIT

	Boost+flyback (DCM+DCM)	Proposed converter(DCM+DCM)
Semiconductors	3 diodes, 1 switch, 1 bridge rectifier	2 diodes, 1 switch, 1 bridge rectifier
Passive components	1 inductor, 2 capacitors, 2-winding Transformer	1 inductor, 3 capacitors, 3-winding Transformer
Switch current	$I_{LB}+I_{Lm}$	$(N_3/N_1)I_{LB}+I_{Lm}$, where $N_3/N_1<1$
Efficiency (at full load)	70%	>90%
Capacitor voltage V_{CB} (for constant input voltage)	Controlled by the ratio L_m/L_B	Controlled by the ratio L_m/L_B and winding ratio N_3/N_1
THD of the input current	>20%	<10%

IV. CONCLUSIONS

The proposed method shapes the input current based on a quasi-active power factor correction (PFC) scheme. In this method, high power factor and low harmonic content are achieved by providing an auxiliary PFC circuit with a driving voltage which is derived from a third winding of the transformer of a cascaded dc/dc flyback converter. It eliminates the use of active switch and control circuit for PFC. The auxiliary winding provides a controlled voltage-boost function for bulk capacitor without inducing a dead angle in the line current. The input inductor can operates in DCM to achieve lower THD and high power factor. By properly designing the converter components, a tradeoff between efficiency and harmonic content can be established to obtain compliance with the regulation and efficiency as high as possible

REFERENCES

[1] O. Gracia, J. A. Cobos, R. Prieto, and J. Uceda, "Single-phase power factor correction: A survey," *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749–755, May 2003.

[2] R. Redle, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power factor correctors with fast regulation of the output voltage," in *Proc. IEEE PESC 1994 Conf.*, pp. 1137–1144.

[3] C. Qian and K. Smedley, "A topology survey of single-stage power factor with a boost type input-current-shaper," *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 360–368, May 2001.

[4] T.-F. Wu, T.-H. Yu, and Y.-C. Liu, "An alternative approach to synthesizing single-stage converters with power factor correction feature," *IEEE Trans. Ind. Electron.*, vol. 46, no. 4, pp. 734–748, Aug. 1999.

[5] L. Huber, J. Zhang, M. Jovanovic, and F.C. Lee, "Generalized topologies of single-stage input-current-shaping circuits," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 508–513, Jul. 2001.

[6] H. Wei, I. Batarseh, G. Zhu, and K. Peter, "A single-switch AC-DC converter with power factor correction," *IEEE Trans. Power Electron.*, vol. 15, no. 3, pp. 421–430, May 2000.

[7] L. K. Chang and H. F. Liu, "A novel forward AC/DC converter with input

current shaping and fast output voltage regulation via reset winding," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 125–131, Feb. 2005.

[8] H. L. Do, "Single-stage single-switch power factor correction AC/DC converter," *Inst. Electr. Eng. Proc. Electr. Power Appl.*, vol. 152, no. 6, pp. 1578–1584, Nov. 2005.

[9] J. Qian, Q. Zhao, and F. C. Lee, "Single-stage single-switch power factor correction ac/dc converters with dc-bus voltage feedback for universal line applications," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1079–1088, Nov. 1998.

[10] S. Luo,W. Qiu,W.Wu, and I. Batarseh, "Flyboost power factor correction cell and a new family of single-stage AC/DC converters," *IEEE Trans. Power Electron.*, vol. 20, no. 1, pp. 24–33, Jan. 2005.

[11] M. M. Jovanovic, D. M. Tsang, and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifiers-regulators by variablefrequency control," in *Proc. IEEE APEC 1994 Conf.*, pp. 569–575.

[12] J. Sebastian, A. Femandez, P. Villegas, M. Hemando, and J. Prieto, "New topologies of active input current shapers to allow AC-to-DC converterswith asymmetrically driven transformers to comply with the IEC-1000- 3-2," *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 493–501, Jul. 2002.

[13] N. Vazquez, J. Lopez, J. Arau, C. Hernandez, and Elias Rodriguez, "A different approach to implement an active input current shaper," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 132–138, Feb. 2005.

[14] K. Zhou, J. G. Zhang, S. Yuvarajan, and D. F. Weng, "Quasiactive power factor correction circuit for switching power supply," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1410–1414, May 2008.

BIOGRAPHY

Santosh A, II-M.Tech P.E, Department of EEE, SV Engineering College, Suryapet.

Shivashankar Tallada, II-M.Tech P.E, Department of EEE, Annamacharya institute of technology & sciences, Bata Singaram(V), Hayath Nagar(M)