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Area Efficient Wide Frequency Range CMOS Voltage Controlled Oscillator For PLL In 0.18µm CMOS Process

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ABSTRACT

Current starved VCO is simple ring oscillator consisting of cascaded inverters. Differential ring oscillator has a differential output to reject common-mode noise, power supply noise and so on. In this paper we have designed and simulated Current Starved VCO and Differential VCO for PLL in Tanner 13.0v 0.18µm digital CMOS process. Performance comparison is done in terms of high oscillation frequency, low power consumption, and low area. It is observed that maximum oscillation frequency about 2GHz is achieved in three stage differential VCO. But area has been reduced to 688µm^2 with low power consumption of 359.08µW with large tuning range in three stage current starved VCO for a frequency of 1.1GHz at 1.8 V_{DD}.

Keywords: **Current starved VCO, Three stage Differential VCO**

1 Introduction

A CMOS Voltage controlled oscillator (VCO) is a critical building block in PLL which decides the power consumed by the PLL and area occupied by the PLL. VCO constitute a critical component in many RF transceivers and are commonly associated with signal processing tasks like frequency selection and signal generation. RF transceivers of today require programmable carrier frequencies and rely on phase locked loops (PLL) to accomplish the same. These PLLs embed a less accurate RF oscillator in a feedback loop, whose frequency can be controlled with a control signal. Transceivers for wireless communication system contain low-noise amplifiers, power amplifiers, mixers, digital signal-processing chips, filters, and phase-locked loops.

Voltage controlled oscillators play a critical role in communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency Circuits. Their output frequency is a function of a control input usually a voltage.

An ideal voltage-controlled voltage oscillator is a circuit whose output frequency is a linear function of its control voltage. Most application required that oscillator be tunable, i.e. their output frequency be a function of a control input, usually a voltage.

There are two different types of voltage controlled oscillators used in PLL, Current starved VCO and Differential VCO [1].In recent years LC tank oscillators have shown good phase-noise performance with low power consumption. However, there are some disadvantages. First, the tuning range of an *LC*-oscillator (around 10 - 20%) is relatively low when compared to ring oscillators (>50%). So the output frequency may fall out of the desired range in the presence of process variation. Second, the phase-noise performance of the oscillators highly depends on the quality factor of on-chip spiral inductors. For most digital CMOS processes, it is difficult to obtain a quality factor of the inductor larger than three.[2] Therefore, some extra processing steps may be required. Finally, on-chip spiral inductors occupy a lot of chip area, typically around 200 ×200-300 ×300 m^2, which is undesirable for cost and yield consideration [3].

The ring oscillators, however, do not have the complication of the on-chip inductors required for the LC oscillators. Thus the chip area is reduced. In addition to a wide tuning range; ring oscillators with even number of delay cells can produce quadrature-phase outputs [4]. The phase noise performance of ring oscillators is much poorer in general [4], [5]. Also, at high oscillation frequencies, the power consumption of the ring oscillators may not be low which is a key requirement for battery operated devices [6]. To overcome these problems, we worked on Three stage current starved Oscillator and Differential voltage controlled oscillator without an LC tank. Finally their performances are compared based on their simulation results.

2 Circuit Description

2.1. Three stage Current Starved VCO

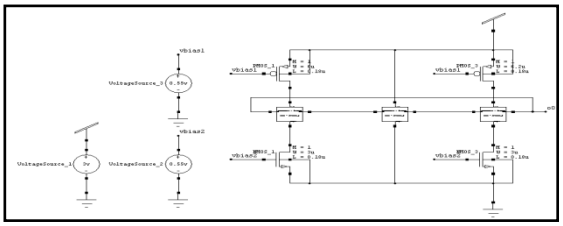

Fig 1 Designed current starved VCO

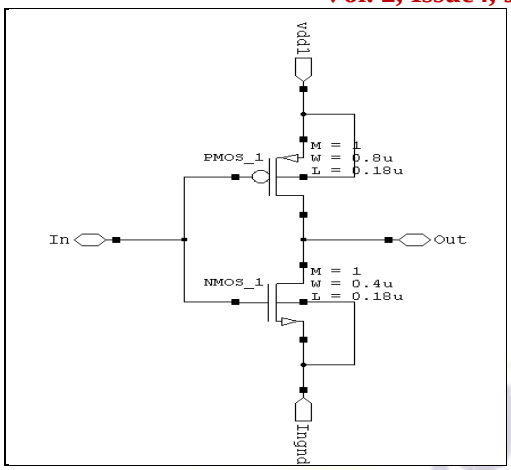

Fig 2 Inverter schematic

The operation of current starved VCO is similar to the ring oscillator. Fig1. Shows designed three stage Current-Starved VCO [7].Each delay cell consist of one PMOS and NMOS which operate as inverter, while upper PMOS and lower NMOS operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter current source stage. PMOS and NMOS drain currents are the same and are set by the input control voltage [8],[9].Fig 2 shows the inverter schematic.

The total capacitance Ctot is given by,

$$\mathbf{Ctot} = \frac{5*\mathbf{Cox}(\mathbf{WpLp}+\mathbf{WnLn})}{2} \qquad (1)$$

where Cox is the oxide capacitance.

The number of stages of the oscillator is selected; there are 3 stages. The centre drain current is calculated as:

$$\text{IDcentre} = N * VDD * Ctot * Fcen \qquad (2)$$

where N is the number of stages of inverter.

The sizes of PMOS and NMOS of inverter stage are determined as:

$$\text{Dcentre} = \frac{\beta(Vgs - Vthn)2}{2} \qquad (3)$$

$$\text{Where, } \beta = \frac{Kp*W}{L}$$

It can be shown that the oscillation frequency is:

$$Fosc = 1/N * Td \qquad (4)$$

$$= \frac{ID}{N*Ctot*VDD} \qquad (5)$$

where Td is the time delay.

Above equation gives the centre frequency of the VCO when

ID=IDcentre.

The VCO stops oscillating, neglecting subthreshold currents,

When, V_{inVCO}<Vthn.

Thus, Vmin=Vthn and Fmin=0

The max VCO oscillation frequency Fmax is determined by finding ID when

Vi_{nVCO}=VDD

2.2. Differential VCO

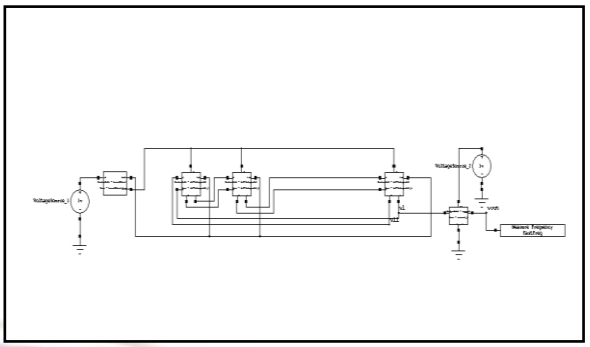

Fig 3 Designed Differential VCO

Fig 3 shows designed differential VCO consisting of three delay cells.

In the delay cells proposed in this work, we provide the necessary bias condition for the circuit to oscillate by means of using the positive partial feedback [10] Fig 4 shows the delay cell used in differential VCO.

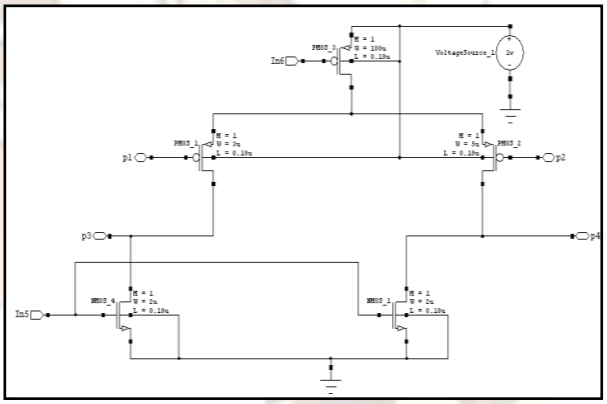

Fig 4 Delay cell used in Differential VCO.

To achieve maximum frequency the bias scheme has been improved further. The bias scheme composed by transistors PMOS1 to PMOS6 and NMOS1 to NMOS5 provides a controlled bias current and a controlled voltage *Vc* in such a way that the transistors of delay cell stay in saturation region for the entire control voltage range[11],[12].

Fig 5 shows the necessary bias scheme used in differential VCO.

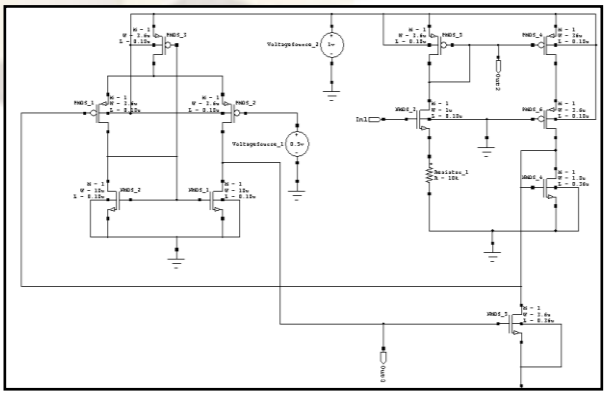

Fig 5 Bias scheme used in Differential VCO.

3 Simulation Result

3.1Output waveforms

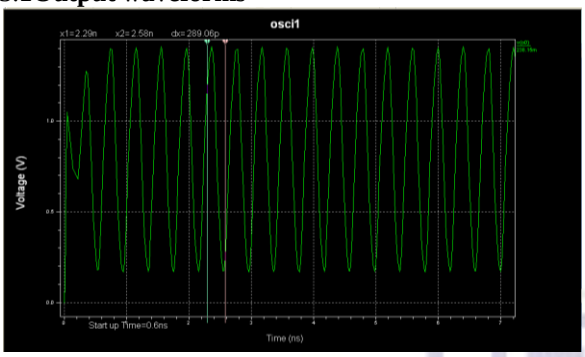

Fig 6 Output waveforms of current starved VCO

Fig 6.shows the output waveforms of current starved VCO. It is noted that at a constant control voltage of 1.15V the output frequency of current starved VCO is 1.153GHz.Simulation results reported that the power consumption is 359.08µW at 1.1GHz

When the control voltage is varied from 0.4V to 1.15V,the oscillation frequency of the designed current starved VCO ranges from 426.80 MHz-1.153GHz Table I. shows the characteristics of the current starved VCO between control voltage (V) and frequency (MHz). The relationship between frequency and control voltage is shown in fig 7.The relationship between frequency and control voltage is predicted using curve hitting algorithm by polynomial

$$y=62.10x+594.1 \quad (6)$$

with coefficient of correlation of ,R^2=0.864

Table 1 Control Voltage (V) Vs Frequency (MHz) of Current Starved VCO

Voltage(V)	Frequency(MHz)
0.4	426.80
0.55	805.15
0.65	813.00
0.75	861.32
0.85	893.65
0.95	908.26
1.05	977.51
1.15	1153.40

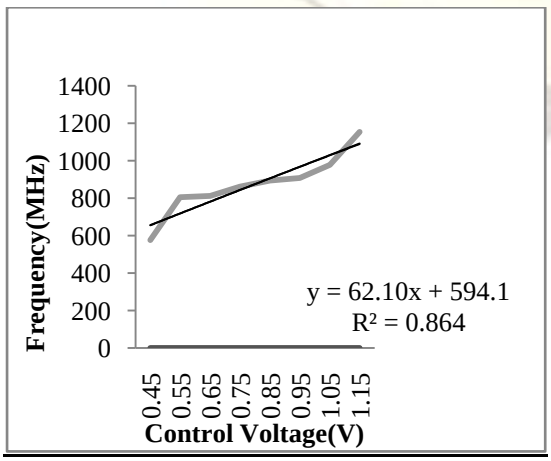

Fig 7 Control Voltage (V) VS Frequency (MHz)

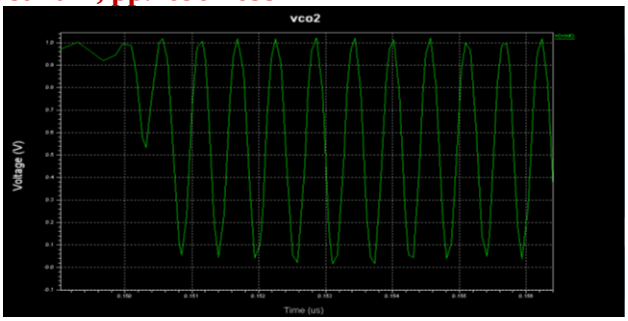

Fig 8 Output waveforms of Differential VCO

Fig 8.shows the output waveforms of differential VCO. It is noted that at a constant control voltage of 0.26V the output frequency of current starved VCO is 2GHz.Simulation results reported that the power consumption is 0.91mW at 2GHz.

When the control voltage is varied from 0.26V to 0.7V, the Oscillation frequency of the designed differential VCO ranges from 2GHz to 60MHz.Due to PMOS based differential VCO, frequency decreases with an increase in supply voltage. Table 2 gives the characteristics of the differential VCO between control voltage (V) and frequency (GHz). The relationship between frequency and control voltage is predicted using curve hitting algorithm by polynomial

$$y = -0.209x+2.120 \quad (7)$$

with coefficient of correlation of ,R^2=0.980

Table 2 Control Voltage (V) Vs Frequency (GHz) of Differential VCO

Voltage(V)	Frequency(GHz)
0.26	2
0.3	1.78
0.35	1.51
0.4	1.21
0.45	0.92
0.5	0.79
0.55	0.59
0.6	0.49
0.65	0.36
0.7	0.06

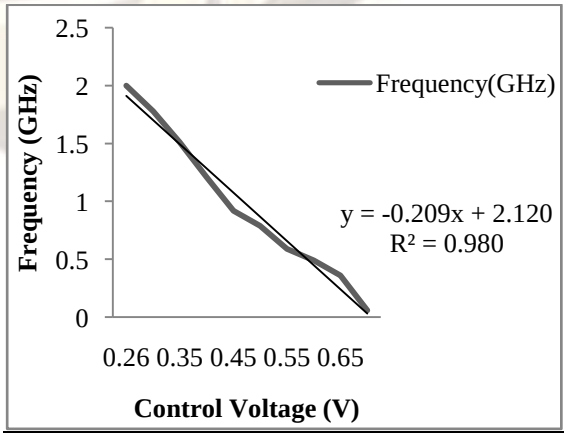

Fig 9 Control Voltage (V) Vs Frequency (GHz)

3.2. **Performance comparison**

The results of current starved VCO and Differential VCO are compared in table 3.

From comparison table it has been observed that as the number of delay cells and number of transistor in delay cell are less in current starved VCO area and power consumption has been reduced in current starved VCO than differential VCO.But maximum oscillation frequency about 2GHz has been achieved in differential VCO due to improved bias scheme.

Table 3 Comparison Table

Parameters	Diff VCO	Three Stage Current Starved VCO
Tool	Tanner 13.0v	Tanner 13.0v
Technology	0.18µm	0.18µm
Supply Voltage	1V	1.8V
I/P Tuning Range	0.26-0.7V	0.45 -1.15 V
Range of Oscillation Frequency	60MHz-2GHz	426.80 MHz-1.153GHz
Area	1648µm^2	688µm^2
Power Consumption	0.91mW	359.08µW
Gate Length	0.18µm	0.18µm
.# no of delay cells	03	03
No of transistors in delay cell	05	02

4 Conclusion

This paper compares the performance of a current starved VCO and differential VCO with the design experiment and with the quantitative evaluation. Simulation results shows that area wise, power consumption and tunable frequency range, Current starved VCO is superior to a differential VCO. Power consumption and area of both VCO will decrease proportional to the technology node. However, noise characteristics will get worse inversely proportional to the technology node. Designed VCO is used as frequency synthesizer, frequency multiplier and for clock systems design

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