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FPGA Implementation of low power multiserial to Ethernet gateway for Unmanned Aerial Vehicle (UAV) data acquisition systems

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Abstract-

The Unmanned Aerial Vehicle (UAV) data link is a combination of ground control station and airborne data terminal. The computers on the ground need control and check more than ten assemblies, containing main and sub remote control transmitters, telemetry receivers, image decompression board, ground positioning receiver and radio location tracking servo system etc. The communication between them is asynchronous serial form and at present, the serial ports are expanded by typical serial control card, which are used for interfacing with different types of sensors and separate microprocessor /microcontroller is used for Ethernet connectivity which increases cost,space and power consumption .

To resolve these problems, a method of multi-serials to Ethernet Gateway based on the field programmable gate array (FPGA) +network interface chip is implemented in this project. The Ethernet Gateway will send data as Ethernet frame format after receiving serial data, indirectly achieves multi-serials communication, simplifies cabinet wiring and improves CPU's efficiency.

Keywords- Ethernet, FPGA, Gateway, UAV,UART, Multiserial

I . Introduction

The data is acquired from multiple serial digital modules and are transmitted to the Ethernet module, and is received by ground station, by the TCP/IP protocol. The Gateway[1] consists of FPGA and Ethernet module .Using a flexible FPGA programming feature, a UART [1] can be designed in it. If several UARTs are in it, the system has the capacity of communication with multiple serial ports. The Ethernet module provides Ethernet communication and is configured at the time of initialization. The Gateway's function is to achieve communication between the serial devices and Ethernet.

When Gateway receives data from devices, it will choose useful data from serial data frame following the communication protocol, and send data after packaged. When it receives data from Ethernet, it first unpacks the frame and determines the port number to transfer data to its buffer and adds the synchronous heads.

In this project we use Hardwired TCP/IP Embedded Ethernet Controller chip will be interfaced to FPGA[2] [3] to provide Ethernet interface. Various digital signals will be captured by FPGA and will be sent on a serial line. The FPGA implements all the necessary logic to read the data from these sensors and store the data in it. On FPGA logic also will be implemented to read data from multiple number of serial ports. The Ethernet module takes data from serial port and sends to PC in Ethernet form. In PC application will be developed to read data from Ethernet and store it on PC harddisk. .

II. Multiserial to Ethernet gateway

A.LM35 (Precision Centigrade Temperature Sensors) The LM35 is an integrated circuit temperature sensor that can be used to measure temperature with an electrical output proportional to the temperature (in ^{o}C).The LM35 operates over a range of −55° to +150°C temperature range. LM35 draws only 60 micro amps from its supply and possesses a low self-heating capability and generates a higher output voltage .The block diagram of data acquisition system with Ethernet module is shown below.

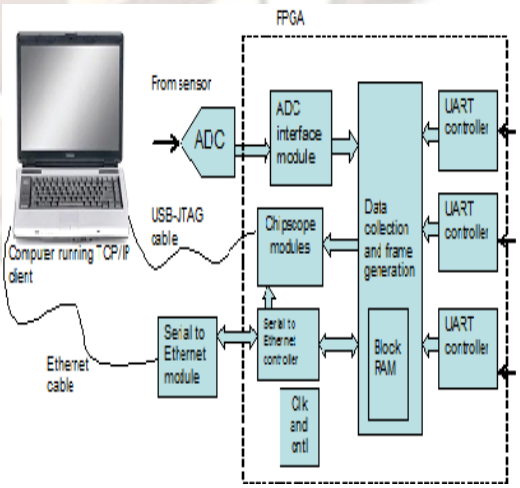

Fig1. Data acquisition system with Ethernet gateway block diagram

B.Analog to digital converter

An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a device that converts a continuous quantity to a discrete time digital representation.

The ADC internal diagram is shown below.It consists of 4 bit up counter and 12 bit left shift register.

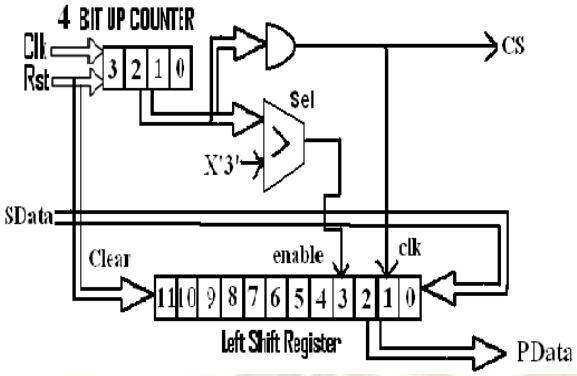

Fig2. ADC internal diagram

Above module is a single ADC interface block. When reset is given for 4 bit up counter and 12 bit left shift register, it will clear the data and make initially zero's in all bits. When Reset is active low then counter will start counting, this count is given to a comparator (it will be active high when count is more than reference i.e x'3'). The comparator output is referred as enable signal and is given to the shift register .when enable is active high it will shift the register values from right to left by one bit. The count bits are given to an And gate and that will be active high, when the counter having maximum count and that will be taken as output to CS(chip select) signal. This signal is given to shift counter as clk, when clk is present, shift register will give parallel output data as pdata.

C. ADC Interface Module

The interface module is ADCS7476A is a high speed, low power, 12-bit serial A/D converter that interfaces easily to FPGAs. The A/D interface adapter (AD1_PMOD) is implemented within the FPGA.

D.UART Module

A universal asynchronous receiver/transmitter, abbreviated UART is a microchip with programming features that translates data between parallel and serial forms.

The Universal Asynchronous Receiver/Transmitter (UART) takes bytes of data and transmits the individual bits in a sequential manner. At the destination, an another UART re-assembles the bits into complete bytes. Each UART contains a shift register which is the fundamental method of conversion between serial and parallel forms. Serial transmission of digital information (bits) is cost effective than parallel transmission .

UART BLOCK

The UART is a serial interface with a frame format of start bit of active low '0'at beginning of frame and 8 bit of information with a stop bit of active high'1' signal at the end. The operation of UART is controlled by Clock signal which is fed from external crystal. The UART serial data format is shown in fig. 3.

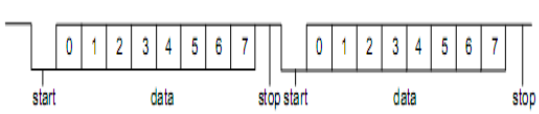

Fig 3. UART serial data format

UART Receiver

The uart receiver diagram is shown below in fig .4 Itconsists of baud generator and receiver section module .The receiver section module in turn consists of a receiver.

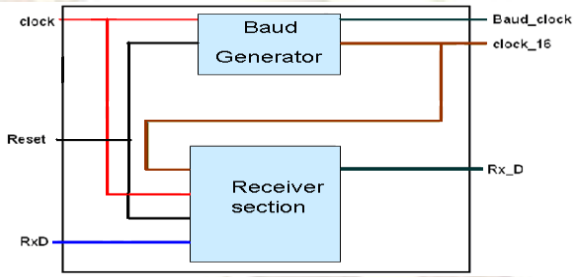

Fig 4. UART receiver diagram

As shown in above figure Receiver section is a combination of a baud generator and receiver section module, each module has been explained below in detail.

Baud Generator

Baud generation section is a clock divider circuit, FPGA board clock runs at 50MHz, but UART transfers data at predefined standards that had to be maintained, in present system it is designed for a rate of 9600 bits/sec(i.e $50x10^6$ is scaled down for 9600). It generates 9600 pluses per sec; this implies the speed of UART is 9600 bits per sec. Another clock is with a 16 times faster than required, and it is given to the receiver section, so that the data will not be corrupted.

Receiver Section UART receiver handles reception of data from RS232 port. Main functions of receiver block are to convert the serial data to parallel data, and check the correctness of data from parity and store the received data. UART receiver state machine is shown in Figure . The receiver is in IDLE state by default. When the serial data pin goes low, indicating the start bit, the

state machine enters DATA0 state. The data is received, one bit at a time from LSB to MSB in states DATA0 to DATA7.

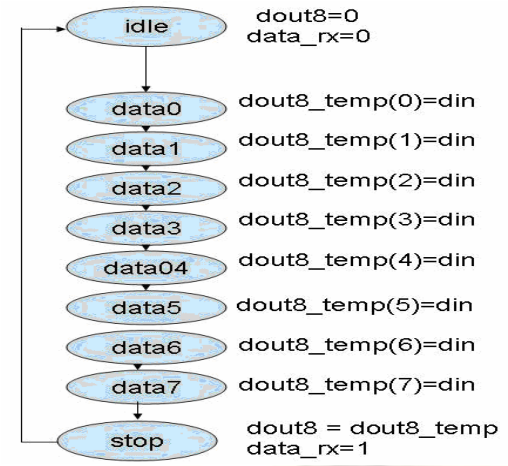

Fig 5. UART receiver state machine

UART receiver state machine is shown in Figure 5. If parity is enabled, the state machine checks the parity bit received against the parity obtained from received data. If the data received is fine, the data_rx (data_rx_done) bit is set to '1' and the receiver goes back to IDLE state again.

E. Transmitter

In this project Transmission operation is simpler since it is under the control of the transmitting system. As soon as data is accumulated in the shift register after completion of the previous character, the UART hardware generates a start bit, shifts the required number of data bits, generates and add the parity bit (if used), and the stop bits. Since transmission of a single character may take a long time , the UART will maintain a flag showing busy status so that the host system does not allow a new character for transmission until the previous one has been completed; this may also be done with an interrupt. Transmitting and receiving UARTs must be synchronized for the same bit speed, character length, parity, and stop bits for proper operation.

F.Data collection module

Adc_in, UART 's input1,input2 and input3 are the inputs for this block .These input's are selected with select lines that are generated from input address counter .Rd_address, wr_address, data, clk and rd_wr are inputs to connection memory module and data(q) is the output. The diagram for data collection module is shown in below fig.

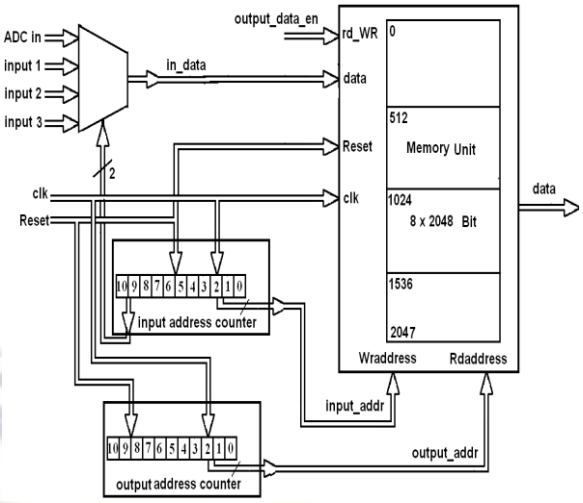

Fig 6. Data collection module internal diagram

In_Data is stored in the ROM (i.e it contains 2048 memory locations) memory according to address given by the wr_address that is generated by input address counter, when rd_wr signal is at logic high value with raising edge of the clk.

Data is forced on to output line data according to rd_address that is generated by output address counter ,whenever rd_wr signal is at logic high with falling edge of the clk. When reset is at active high then the module will clear the data .If it is in active low ,then module will be working in normal operation.

G. Serial to Ethernet module:

The serial to Ethernet module [1] is shown in below fig.7 The Serial to Ethernet converters transmit RS232, RS422 or RS485 data across an IP network.

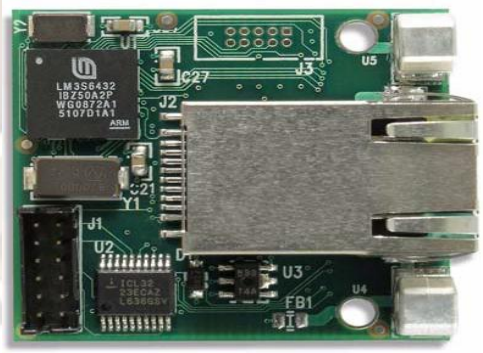

Fig 7.serial to Ethernet module

Features:

The S2E module is a simple add-on product to existing systems to provide network connectivity. It consists of all the necessary hardware to quickly evaluate the module capabilities. The S2E module possess the following features:

1. LM3S6432 Stellaris microcontroller with 96 kB of Flash memory and 32 kB of SRAM.
2. 10/100 Mbit Ethernet port.
3. Two serial ports

I.PORT0 is an asynchronous serial port with RS232 levels

- Data rates up to 230,400 bits/sec.
- Includes RTS/CTS for flow control.

II .PORT1 has 4 CMOS/TTL level signals that can be configured several ways

- Data rates up to 1 Mbit/sec.
- As an asynchronous serial port with RTS/CTS flow control or with 2 GPIOs.
- As 4 GPIOs.
- As a synchronous serial port (master or slave) with support for SPI and other synchronous protocols.

4. RDK is USB-powered, no additional power supply required.
5. Ethernet boot loader for firmware upgrades.
6. JTAG 10-pin debug header.

III. Simulation Results

Fig inputs are adc(sdata1),rd1,rd2,rd3.These inputs are selected based on selection signal. The data_in is the output signal .According to selection signal, the input is received by the UART and it transmitted to the Ethernet module which acts as a transmitter section and which can be seen outputs on the pc.In this project the selection signal is 00.

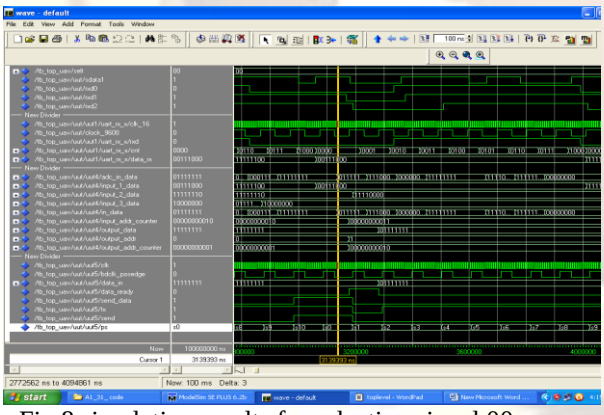

Fig 8 simulation results for selection signal 00

IV. CHIPSCOPE PRO RESULTS

The chipscope result is shown below. The Temp_data is a data received from the temperature sensor module, and Data_LED1, Data_LED2, Data_LED3 represents the received input data from their respective UART modules. According to the selection line input, the respective UART module data is displayed on the output_data.

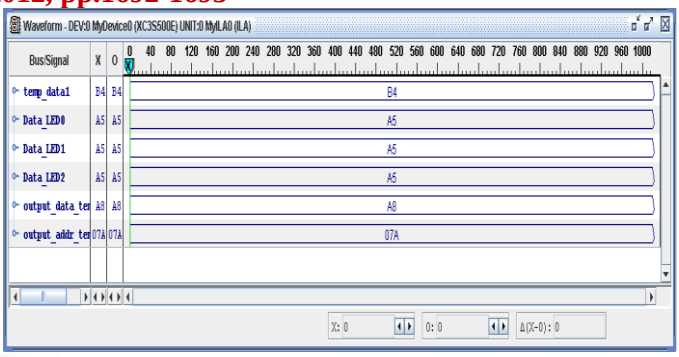

Fig 9chipscope results

The power analysis can be done by using xpower analyzer.In this project the total power obtained is 87.66 milliwatts(mw).

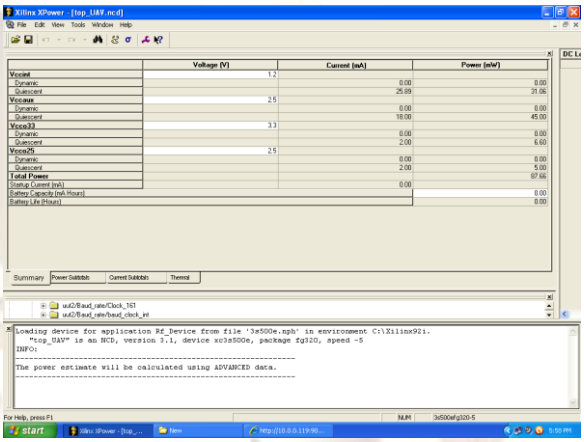

Fig 10. Xpower analyzer

V. Conclusion

The results of test denote that using this method, we can simplify the communication between pc and port devices and it improves the efficiency of CPU and ensure the processing of system in real time .FPGA programming features provide lot of scope for adding additional functionality for further upgrade of system.This design could be used in the domain of industrial automation and data acquisition systems.

References

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