M.Praveen Kumar, G.Kumaraswamy / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 4, July-August 2012, pp.1370-1376

Comparison of Single-Phase Uninterruptible Power Supply Based on Z-Source Inverter with traditional UPS

***M.Praveen Kumar, Pg Student, **G.Kumaraswamy**
*Power Electronics, Dept of EEE, RGM College of engg. & Tech,
Nandyal, Andhra Pradesh, India
**Assoc Prof Dept of EEE, RGM college of engg.& Tech,
Nandyal, Andhra Pradesh,India

Abstract:

This paper presents a new topology of uninterruptible power supply (UPS) by using a Z-source inverter, where a symmetrical LC network is employed to couple the main power circuit of an inverter to a battery bank. With this new topology, the proposed UPS can maintain the desired ac output voltage at the significant voltage drop of the battery bank with high efficiency, low harmonics, fast response, and good steady-state performance in comparison with traditional UPSs. The simulation and experimental results of a 3-kW UPS with the new topology confirm its validity.

***Index Terms*: Dual loops shoot-through, uninterruptible power supply (UPS), Z-source inverter.**

I.INTRODUCTION

UNINTERRUPTIBLE power supplies (UPSs) are widely used to supply critical loads, such as airline computers and life-support systems in hospitals [1]–[5], providing protection against power failure or anomalies of power-line
Voltage [6]. In general, there are two types of traditional single-phase UPSs. The first one couples a battery bank to a half or full-bridge inverter with a low-frequency transformer [7], as shown in Fig. 1(a). In this type of UPSs, the ac output voltage is higher than that of the battery bank; thus, a step-up transformer is required to boost voltage. Due to the presence of the step-up transformer, the inverter current is much higher than the load current, causing high current stress on the switches of the inverter. The transformer also increases the weight, volume, and cost of the system. The second one couples a battery bank to a dc/dc booster with a half- or full bridge inverter [8], [9], as shown in Fig. 1(b). In this type of UPSs, the additional booster is needed, leading to high cost and low efficiency. The controlling of the switches in the booster also complicates the system. Furthermore, the dead time in the pulse width-modulation (PWM) signals to prevent the upper and lower switches at the same phase leg from shooting through has to be provided in the aforementioned two types of UPSs, and it distorts the voltage waveform of the ac output voltage.

In this paper, a new topology of the UPS is proposed by using a Z-source inverter [10]–[13]. With this new topology, the proposed UPS offers the following advantages over the traditional UPSs:1)The dc/dc booster and the inverter have been combined into one single-stage power conversion 2)the distortion of the ac output-voltage waveform is reduced in the absence of dead time in the PWM signals; and 3) the system has achieved fast transient Response and good steady state performance by adopting dual-loop control

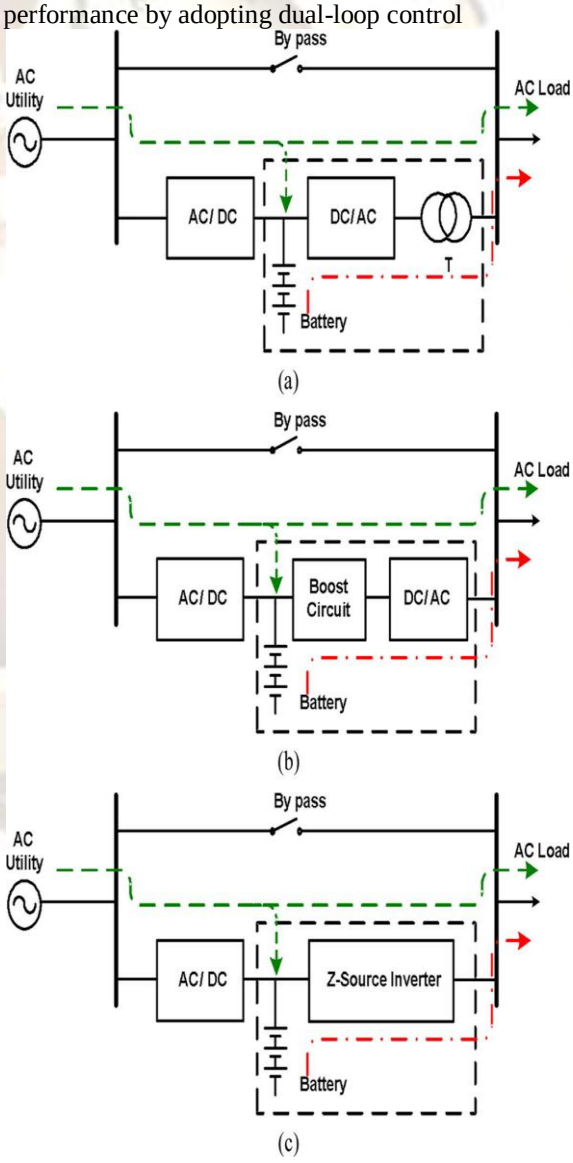


Fig. 1. Topologies of UPS. (a) DC/AC inverter + transformer. (b) DC/DC booster + DC/AC inverter. (c) Z-source inverter.

II. SYSTEM CONFIGURATION AND OPERATING PRINCIPLE

Fig. 1(c) shows a new topology of the UPS with a Z-source inverter. In the normal operation, the rectifier provides power to the inverter. In the case of power outage, the battery bank supplies the inverter, as shown in Fig. 2. It consists of a dc source (E, C3, and D), a Z-source symmetrical network (L1 = L2 and C1 = C2), an H-bridge inverter (S1–S4), and a filter (L*s* and C*s*) . Table I shows a total of nine switching states and their vector representations, where the switching function S*x* (*x* = 1, 2, 3, or 4) is defined as 1 when switch S*x* turns on and as 0 when switch S*x* turns off.

Thus, when two active vectors {1 0}, {0 1}) are taken, the battery bank voltage is applied to he load through two inductances (L1 and L2); when two null vectors ({0 0}, {1 1}) are taken, the load terminal is shorted by either the upper or lower two switches; when the shoot-through zero vectors are taken, the load is shorted by the upper and lower switches at the same phase leg. These zero vectors are allowed in the Z-source inverter, whereas they are forbidden in the voltage source inverter. Because of this unique feature of the Z-source inverter, the proposed UPS can generate the desired ac output voltage *u*o, regardless of the battery bank voltage *u*B, by using the shoot-through zero vectors.

TABLE I
SWITCHING STATES AND VECTOR REPRESENTATIONS OF THE Z-SOURCE INVERTER

Switching States	S_1	S_2	S_3	S_4
Active {1 0}	1	0	0	1
Active {0 1}	0	1	1	0
null {0 0}	0	1	0	1
null {1 1}	1	0	1	0
Shoot through	1	1	0	1
Shoot through	1	1	1	0
Shoot through	0	1	1	1
Shoot through	1	0	1	1
Shoot through	1	1	1	1

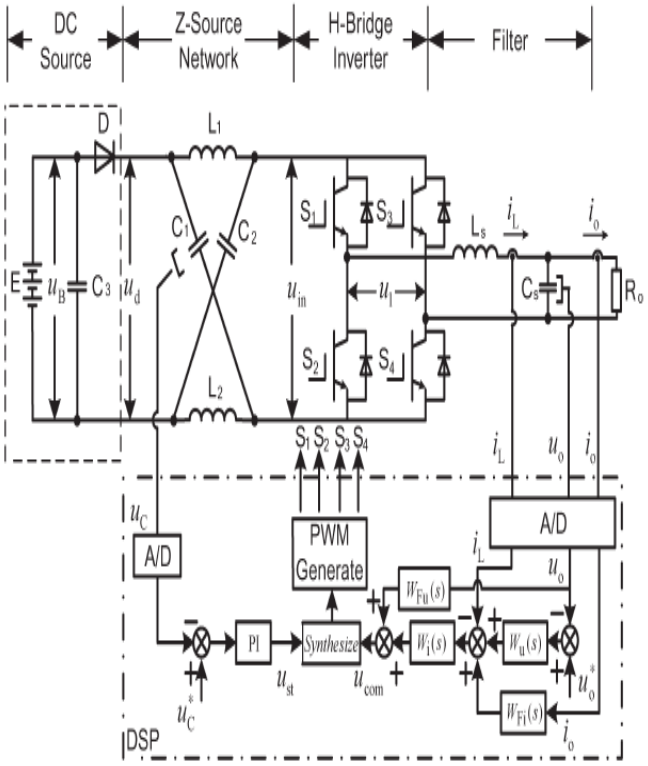


Fig. 2. Z-source inverter for the proposed UPS.

As shown in Fig. 2, the voltage equations of the Z-source inverter [10], [20] can be written as

$$uC1 = uC2 = uC \; uL1 = uL2 = uL. \quad (1)$$

When the Z-source inverter is working in nonshoot-through states during time interval *T*1, the diode D is on, and the H-bridge inverter can be considered as a current source *i*n. Consequently, the equivalent circuit of the Z-source inverter at nonshoot-through states is shown in Fig. 3(a), and its voltage equations are

$$u_b = u_d = u_C + u_L \quad (2)$$

$$u_{in} = u_C - u_L \quad (3)$$

Substituting (2) into (3) yields

$$U_{in} = 2u_C - u_B \quad (4)$$

When the Z-source inverter is working in shoot-through states during time interval *T*0, where *T*0 = *T*s − *T*1, and *T*s is the switching period, the diode D is off, and the H-bridge inverter can be considered as a short circuit. As a result, the equivalent circuit of the Z-source inverter at shoot-through states is shown in Fig. 3(b), and its voltage equations are

$$u_C = u_L \; ui_n = 0 \quad (5)$$

It is recognized that the average voltage of inductor L1 (or L2) over one switching period in steady-state operation is zero

$$(uB - uC)T1 + uCT0 = 0 \quad (6)$$

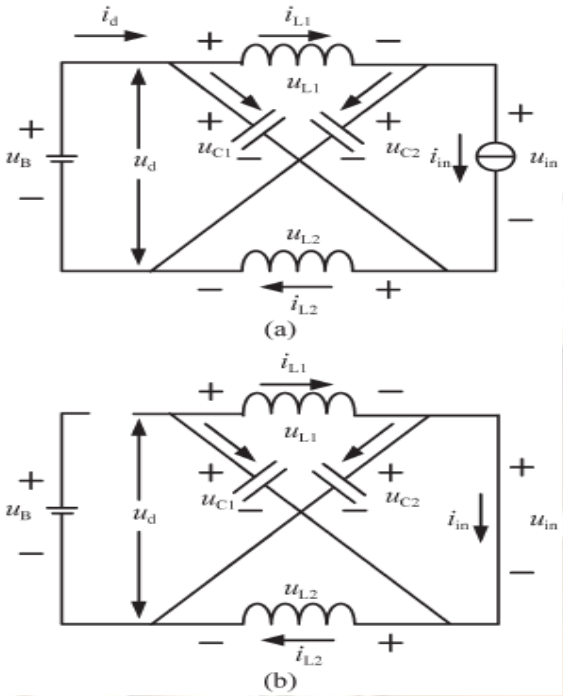


Fig. 3. Equivalent circuit of the Z-source inverter. (a) Nonshoot-through state. (b) Shoot-through state.

with B being the boost factor. If the voltage across the inductor Ls is ignored, the output peak voltage is

$$uom \approx u1m = muin = mBuB \quad (7)$$

where $u1m$ is the peak value of fundamental voltage of the H-bridge inverter and m is modulation index ($m \leq 1$). Thus, the appropriate selection of the booster factor and the modulation index can obtain the desired ac output voltage regardless of the battery bank voltage.

III. CONTROL PRINCIPLE OF THE PROPOSED UPS WITH THE Z-SOURCE INVERTER

Fig. 4 shows the dual-loop control in the proposed UPS with theZ-source inverter, namely, the control of inductor current iL in the inner loop and output voltage uo in the outer loop, where $KPWM/(sTs + 1)$ is the transfer function of the H-bridge inverter and $KPWM$ is the average voltage gain viewed from dc link.

Due to high system switching frequency fs($fs = 1/Ts$), the capacitor voltage of the Z-source inverter is considered constant in one switching period, which is equal to the average input voltage of the Z-source network ud, and thus, the gain $KPWM$ is constant as well.

A. Current Inner Loop

In Fig. 4, the output voltage uo is regarded as a disturbance to the current inner loop. To smooth the output voltage, a voltage feed forward control is adopted

$$uoWFU(s).\frac{(1-d)uB}{(1-2d)(sTs+1)}\text{-uo=0} \quad (8)$$

where $WFu(s)$ is the transfer function of the voltage feed forward controller. As the bandwidth of the inner loop (fi) is designed to be much lower than the system switching frequency, namely, $|sTs|s=j\omega i\_1$,

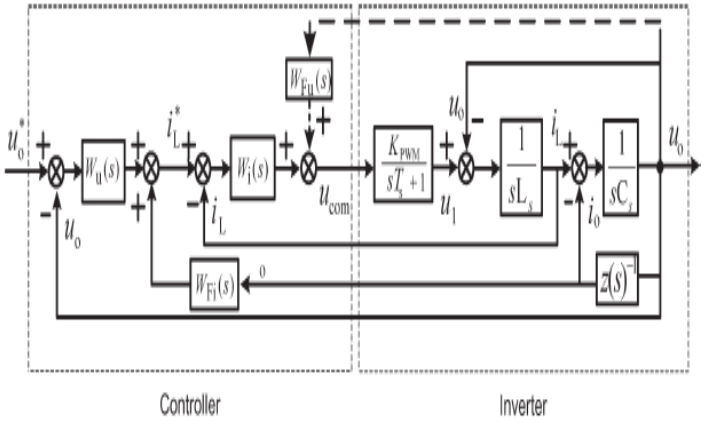


Fig. 4. Control system of the Z-source inverter for the proposed UPS.

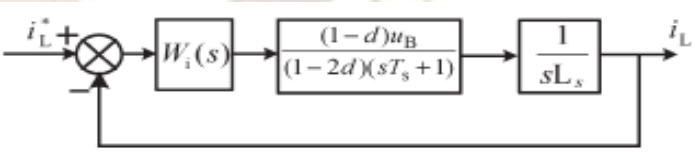


Fig. 5. Block diagram of the inner loop.

TABLE II
PARAMETERS OF THE SIMULATION MODEL

u_0^* (V)	L_S (mH)	C_s (μF)	K_i	K_1	τ_1	d	K_{PWM}	f_s (KHz)
220	1.5	5	0.029	0.013	0.0012	0.12	350	10

TABLE III
STEP RESPONSE OF THE INNER LOOP

K_i	ζ_i	f_{ni} (Hz)	t_s (ms)	σ_i	t_r (ms)
0.0429	0.5	1590	0.81	16.3%	0.16
0.0296	0.6	1320	0.71	9.3%	0.22

loop system to achieve fast response. The tradeoff between
the generation of high-order harmonics and the tracking speed of the reference current is made to choose the bandwidth of the inner loop (*f*i). From the practical engineering point of view, it can be approximately selected as the natural frequency of the inner loop (*f*ni) in the range of 10*f*0 to *f*s/5. The parameters for step response, namely, settle time (*t*s) > 2 ms, current overshoot (*σ*i) < 10%, and rise time (*t*r) > 0.3 ms, are suggested as the criteria to evaluate the tracking performance of the inner loop [26]. Tables II and III show the parameters in the simulation model and the step response of the inner loop, respectively, where ζi is the damping ratio and *γ*i is the phase margin. It can be seen that the step response of the inner loop meets the criteria when the gain of the proportion controller is 0.0296.

B. Output-Voltage Outer Loop

In Fig. 6, the control of the outer voltage loop has taken the inner current loop into account, where *z*(*s*) is an equivalent output impedance. Consider that the current feed forward control of the inner loop has eliminated the load current disturbance

$$io\,WFi(s)\,Wci(s) - io = 0 \qquad (9)$$

where *io* is the load current, *W*Fi(*s*) is the transfer function of the current feed forward controller, *W*ci(*s*) is the closed-loop

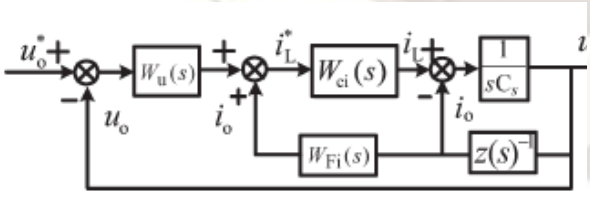


Fig. 6. Block diagram of the outer loop.

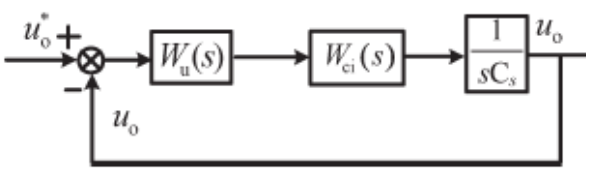


Fig. 7. Simplified block diagram of the outer loop.

transfer function of the inner loop. Because the bandwidth of the outer loop is designed to be much lower than that of the inner loop, the inner loop has faster tracking capability than the outer loop. As a result, the current gain*W*ci(*s*) of the inner loop can be approximately equal to one

$$Wci(s) \approx 1. \qquad (10)$$

Substituting (18) into (17) and solving (17) yield

$$WFi(s) \approx 1. \qquad (11)$$

From (10) and (11), the block diagram of the outer voltage
loop can be simplified to Fig. 7, and its open-loop transfer
function

TABLE IV
STEP RESPONSE OF THE OUTER LOOP

K_1	τ_1	ζ_u	f_{nu} (Hz)	t_s (ms)	σ_u	t_r (ms)
0.013	0.0012	0.9	440	3.05	26.6%	0.449

TABLE V
SPECIFICATIONS OF A 3-KW UPS WITH THE Z-SOURCE INVERTER

u_B	u_o	$C_1(C_2)$	C_3	$L_1(L_2)$	L_S	C_s
360V	220V	1500 μF	1000 μF	2mH	1.5mH	5 μF

than the system switching frequency, namely,

|*s*2|*s*=*jω*u _|*s*/*Ts*|*s*=*jω*u

From the practical engineering point of view, the bandwidth of the outer loop *f*u is chosen to be in the range of (1/51/3)*f*i, and similarly, the natural frequency of the outer loop *f*nu is chosen to be *f*ni/3. In addition, the damping ratio of the outer loop ζu is set to 0.9. Table IV summarizes the step response of the outer loop, where *σ*u is the voltage overshoot.

C. Shoot-Through Zero-Vector Control

As mentioned earlier, the shoot-through zero vectors are allowed in the Z-source inverter. These zero vectors can be controlled to boost the capacitor voltage in the Z-source network, maintaining the desired level of the average input voltage of the Z-source inverter. As shown in Fig. 2,

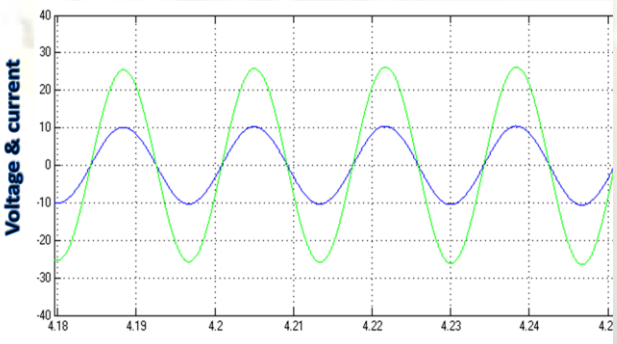
when the battery bank voltage drops significantly under heavy load, the capacitor voltage of the Z-source inverter drops significantly as well; thus, the voltage difference between the reference $u*$ C and the actual capacitor voltage uC is sent to the PI controller which generates the shoot-through zero vectors [27]. The PWM signals with the synthesis of the shoot-through zero vectors ust's and the PWM vectors $u$com's [20] control the Z-source inverter to achieve the
desired ac output voltage uo.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The simulation model and the experimental setup of a 3-kW UPS with the Z-source inverter have been developed to confirm its validity. The technical specifications of the proposed UPS are shown in Table V, where the battery has the normal voltage of 12 V and the normal capacity of 12 A · h. Thirty batteries are connected in series in the proposed UPS, so the normal voltage of the battery bank is 360 V. Both the simulation and the experimentation have been carried out. The results are shown hereafter.

A. Simulation Results

Fig. 8(a) and (b) shows the output voltages and currents, respectively, of the proposed UPS with the Z-source inverter when both pure resistive and nonlinear loads are suddenly



Fia(a)

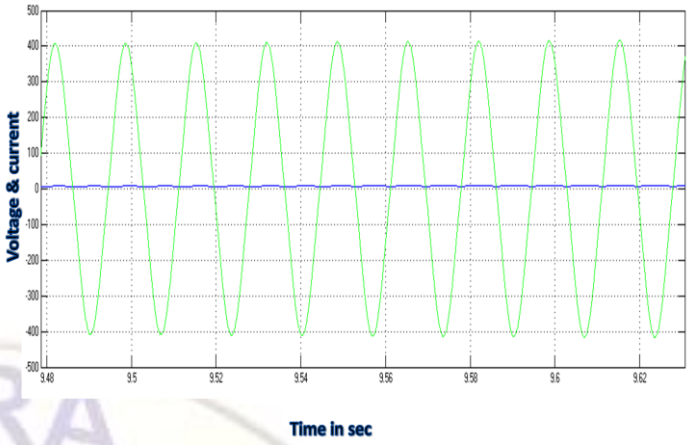


Fig (b)

Fig. 8. Simulation results of the proposed UPS.

(a) Pure resistive load.
(b) Nonlinear load.

Applied. In the steady state, the total harmonic distortion (THD) of the output voltage is less than 1% under the pure resistive load, whereas the THD of the output voltage is less than 3% under the nonlinear load. Fig. 9(a) and (b) shows the output voltages for both the traditional UPS with the voltage source inverter and the proposed UPS with the Z-source inverter, respectively, when the battery bank voltage declines by 20% of its normal voltage. The waveform distortion can be observed for the traditional UPS, whereas the sinusoidal waveform can be kept for the proposed UPS. Fig. 9(c) further shows the strong regulation capability of the proposed UPS at the voltage drop of 50%. It should be noted that the capacitor voltage of the Z-source inverter can be much higher than the battery bank voltage by controlling the shoot-through zero vectors, as shown in Fig. 9(b) and (c).

B. Experimental Results

Fig. 9(a) and (b) shows the output voltages and currents, respectively, of the proposed UPS with the Z-source inverter under both pure resistive and nonlinear loads. In the steady state, the THD of the output voltage is less than 2% for the pure resistive load, whereas the THD of the output voltage is less than 4% for the nonlinear load.

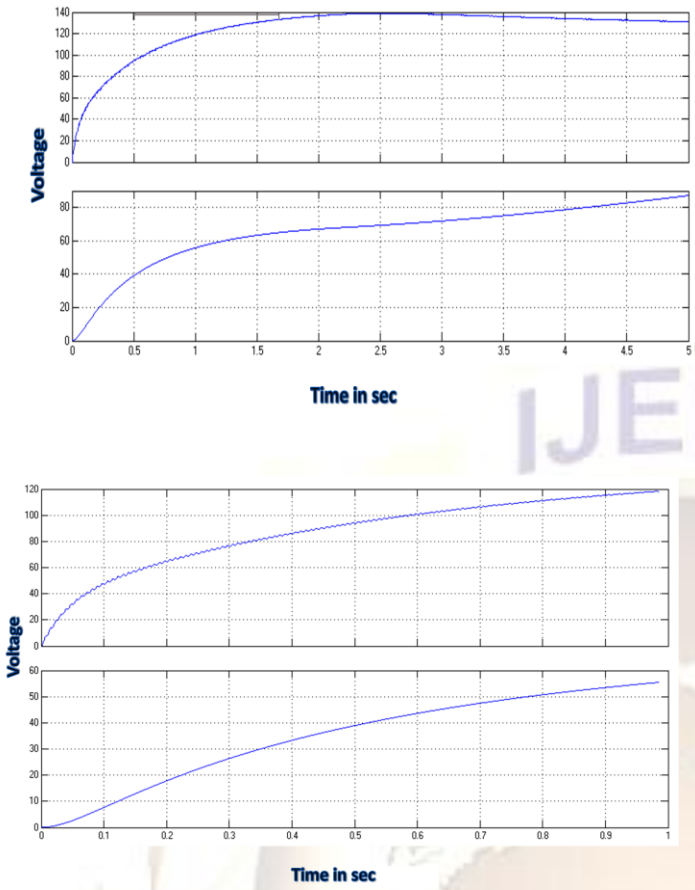


Fig. 9. Simulation results. (a) Proposed UPS when the battery bank voltage declines by 20%. (b)Proposed UPS when the battery bank voltage declines by 50%.

V. CONCLUSION

In this paper, a new topology of the UPS with the Z-source inverter has been presented. Compared with traditional UPSs, the proposed UPS shows the strong regulation capability to maintain the desired ac output voltage at 50% voltage sag of the battery bank with high efficiency, low harmonics, fast response,

REFERENCES

[1] R. Krishnan and S. Srinivasan, "Topologies for uninterruptible power supplies," in *Proc. IEEE Int. Symp. Ind. Electron.*, Budapest, Hungary, 1993, pp. 122–127.

[2] M. S. Racine, J. D. Parham, and M. H. Rashid, "An overview of uninterruptible power supplies," in *Proc. 37th Annu. North Amer. Power Symp.*, Oct. 23–25, 2005, pp. 159–164. Fig. 12. Comparison of efficiencies between proposed and traditional UPSs.

[3] H. Pinheiro and P. Jain, "Comparison of UPS topologies based on high frequency transformers for powering the emerging hybrid fiber–coaxial networks," in *Proc. 21st Int. Telecommun. Energy Conf.*, Copenhagen, Denmark, 1999, pp. 2–11.

[4] J. M. Guerrero, L. Garcia de Vicuna, J. Matas, M. Castilla, and J. Miret, "Output impedance design of parallel-connected UPS inverters with wireless load-sharing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 4, pp. 1126–1135, Aug. 2005.

[5] A. Fernandez, J. Sebastian, M. M. Hernando, J. A. Martin-Ramos, and J. Corral, "Multiple output AC/DC converter with an internal DC UPS," *IEEE Trans. Ind. Electron.*, vol. 53, no. 1, pp. 296–304, Feb. 2006.

[6] J.M. Guerrero, L. Garcia de Vicuna, and J. Uceda, "Uninterruptible power supply systems provide protection," *IEEE Ind. Electron. Mag.*, vol. 1, no. 1, pp. 28–38, Spring 2007.

[7] P. K. Jain, J. R. Espinoza, and H. Jin, "Performance of a single-stage UPS system for single-phase trapezoidal-shaped AC-voltage supplies," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 912–923, Sep. 1998.

[8] C. G. C. Brancol, C. M. T. Cruz, R. P. Torrico-Bascope, F. L. M. Antunes, and L. H. S. C. Barreto, "A transformerless single phase on-line UPS with 110V/220V input output voltage," in *Proc. 21st Annu. IEEE Conf. Expo. Appl. Power Electron.*, Mar. 19–23, 2006, pp. 348–354.

[9] C.-H. Lai and Y.-Y. Tzou, "DSP-embedded UPS controller for highperformance single-phase on-line UPS systems," in *Proc. 28th IEEE Annu. Conf. Ind. Electron. Soc.*, Nov. 5–8, 2002, vol. 1, pp. 268–273.

[10] F. Z. Peng, "Z-source inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, Mar./Apr. 2003.

[11] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and Z-source inverter," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, Sep. 11–14, 2005, pp. 1692–1698.

[12] F. Z. Peng, X. M. Yuan, X. P. Fang, and Z.M. Qian, "Z-source inverter for adjustable speed drives," *IEEE Power Electron Lett.*, vol. 1, no. 2, pp. 33– 35, Jun. 2003.

[13] K. Holland, M. Shen, and F. Z. Peng, "Z-source inverter control for traction drive of fuel cell–battery hybrid vehicles," in *Proc. 40th Annu. Meeting Ind. Appl.*, Oct. 2–6, 2005, vol. 3, pp. 1651–1656.

[14] A. Kawamura, R. Chuarayapratip, and T. Haneysoshi, "Deadbeat control of PWM inverter with modified pulse patterns for uninterruptible power supply," *IEEE*

Trans. Ind. Electron., vol. 35, no. 2, pp. 295–300, May 1988.

[15] M. J. Ryan, W. E. Brumsickle, and R. D. Lorenz, "Control topology options for single-phase UPS inverters," *IEEE Trans. Ind. Appl.*, vol. 33, no. 2, pp. 493–501, Mar./Apr. 1997.

M.Praveen Kumar is born in 1988 in India. He is graduated from JNTU Hyderabad in 2010. Presently he is doing Post graduation in Power Electronics and Electrical Drives Specialization at J.N.T.U.A, Anantapur His main areas of interest include Induction motor drives, Electrical machines,Power Electronics & Converters and Power Electronic Drives

G.Kumaraswamy is born in 1983 in India. He is graduated from JNTU university in 2005 and pursued Post graduation from the same university. He is currently working as a Assistant professor in the department of electrical and electronics engineering R.G.M college of engineering and technology, Nandyal, Andhra Pradesh, India. He has seven years of teaching experience. He has attended several National workshops. His main areas of research include Induction motor drives, Electrical machines FACTS and Harmonic reduction in power converters.