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Comparative Analysis of Low Power 4-bit Multipliers Using 120nm CMOS Technology

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Abstract

In the recent years growth of the portable electronics is forcing the designers to optimize the existing design for better performance. Multiplication is the most commonly used arithmetic operation in various applications like, DSP processor, math processor and in various scientific applications. Overall performance of these devices is strongly depends on the arithmetic circuits like multiplier. This paper presented detailed analysis of low power CMOS multiplier which is very important for today's scientific application. Simulation results are presented at 120nm technology.

Key Words: Multiplier, CMOS, Full Adder, Low Power, Bypassing.

I. INTRODUCTION

Multiplication is one of the most basic functions in a various VLSI applications. The multipliers are widely used in Arithmetic and logic unit in various processors, Digital signal processors (DSP), FIR filters, Math processors, floating point units [3]. Different types of multipliers are available in the literature, depending on the requirements various companies are using the different types of multipliers according to their needs. On the basis of required application, the particular multiplier architecture can be chosen. In DSP applications, the two major constraints for delay perspective in the multiplier is latency and throughput. Latency is the real delay of computing a function whereas throughput is the measure of how many multiplications can be performed in a given period of time [1]. Power consumption in a multiplier has also become a more prominent design factor in addition with the performance.

In CMOS circuits, power dissipation can be divided into static power dissipation and dynamic power dissipation. The static dissipation is due to leakage current which is proportional to the number of transistors used [8]. Since the amount of leakage current is usually small, the major source of power dissipation in CMOS circuits is the dynamic power dissipation. Dynamic power dissipation is due to switching transient current as well as charging and discharging of load capacitances.

To reduce the power dissipation of an array multiplier, the simplest approach is to design a full adder (FA) that consumes less power. The other method is to reduce the switching activities by architectural modification via row or column bypassing techniques [5]. The bypassing scheme disables the operation in some rows or columns to reduce the power dissipation. For the parallel multiplier, the array implementation is the Braun's design. The components used in the Braun's design are full adder as well as AND gate. The logical circuit of full adder is shown in fig 1.

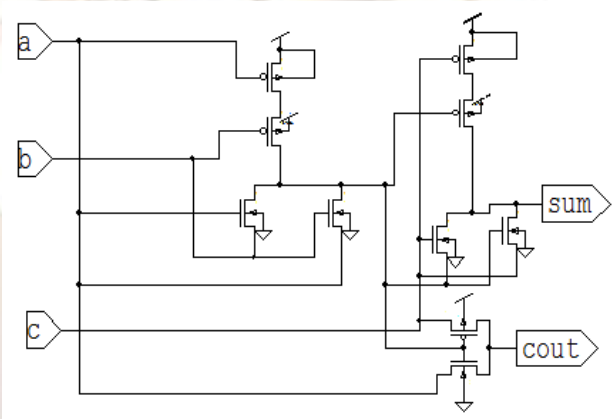


Fig 1: Full adder

The Braun's design consists of (n-1) rows of carry-save adders (CSA), in which each row contain (n-1) full adders. The full adders in the first CSA rows have two valid inputs whereas third input is disabled and two outputs. Full adders in the second CSA rows have three valid inputs, the third input is from the carry output of the above row. The last rows of the full adders can be replaced by 3-bit ripple carry adder (RCA) for carry propagation.

II. ROW BYPASSING AND COLUMN BYPASSING TECHNIQUES

1) Row Bypassing Technique

The Row bypassing scheme disables the operation in some rows in order to save switching power consumption. To understand the row bypassing technique, let take an example of an unsigned 4×4 multiplication. In fig 2, if bit b_j is 0, all product in row j (a_ib_j for $0 \leq i \leq n-1$) are 0. As a result, the addition in corresponding row can be bypassed. For example, let b_1 of fig 2 be 0. For this case, the output from the first CSA row can be fed directly to the third CSA row and the second CSA row is disabled, thus the switching activities are reduced by disabling the second CSA row which results in low power dissipation.

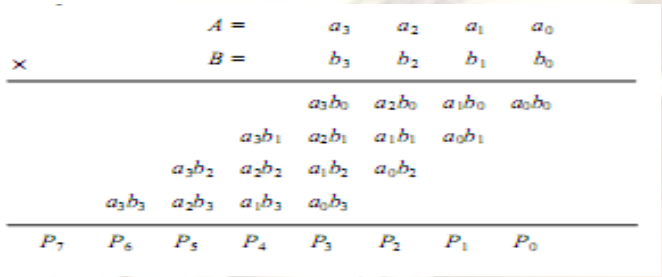


Fig 2: Example of 4×4 multiplication

Since the rightmost FA in the second row is disabled, it does not execute the addition and thus the output is not correct. In order to remedy this problem, extra circuit must be added in the row bypassing technique.

2) Column Bypassing Technique In this technique, if the corresponding bit in the multiplicand is 0, the operations in a column can be disabled. There are two advantages of this technique. First, it eliminates the extra correcting circuit. Second, the modified FA is simpler than that used in the row-bypassing multiplier [2]. To understand the column bypassing technique, let take an example of 4×4 multiplication as shown in Figure 3, which executes 1010×1111.

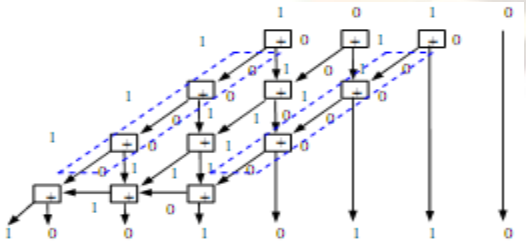


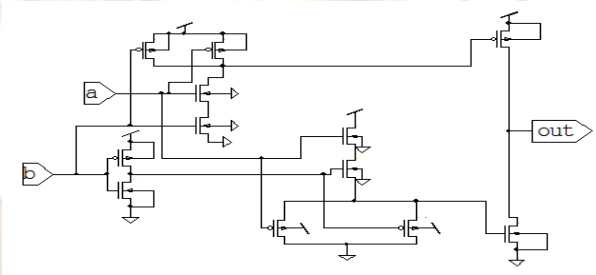
Fig 3: Example of column bypassing

Out of the three input bits, in the first and third diagonals (enclosed by dashed lines), two input bits are 0: the "carry" bit from its upper right FA, and the partial product a_ib_j .Thus, the output carry bit of the FA is 0, and the output sum bit is equal to the third bit, which is the "sum" output of its upper FA.

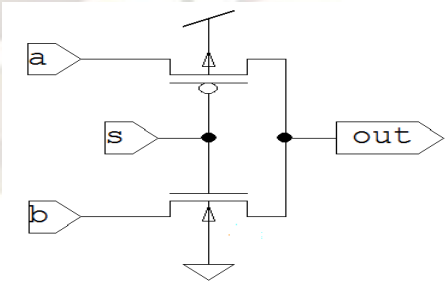
III. LOW POWER MULTIPLIER DESIGNS

In this section, low power multiplier designs based on row bypassing and column bypassing techniques as well as the different blocks used in the low power multiplier designs are discussed.

1) Braun multiplier with row bypassing The Braun multiplier with row bypassing uses additional tri-state buffers and multiplexers in order to skip the FA cell in rows of zero bits. In the multiplier design, the first three CSA rows are attached with three tri-state buffers and two 2:1 multiplexers. The multiplexers are used to select between the full adder output and the bypass signal and the input tri-state buffers serve as input gating when bypassing [5]. The components used in the Braun multiplier with row bypassing are full adder, AND gate, tri-state buffer, multiplexer as well as NOT gate. In Fig. 4, the logical circuits of the tri-state buffer and multiplexer are shown.



(a) Tri-state buffer



(b) Multiplexer

Fig 4: Logical circuits of different blocks used in row bypassing multiplier design

2) Braun multiplier with column bypassing

The Braun multiplier with column bypassing uses additional tri-state buffers and Multiplexers in order to

skip the FA cell in columns of zero bits. In the multiplier design, the first three CSA rows are attached with two tri-state buffers and one 2:1 multiplexer. For the first CSA row, two inputs of FA are provided by tri-state buffers whereas third input is disabled [4]. The components used in the Braun multiplier with column bypassing are full adder, AND gate, tri-state buffer as well as multiplexer.

3) Braun 2-dimensional bypassing multiplier

The 2-dimensional bypassing technique disables the operation in some rows or columns to save switching power consumption. The carry bit of previous bit is considered in 2-dimensional bypassing multiplier. In this technique, the addition operations in the (i+1)-th column or the j-th row can be bypassed if the bit, a_i, in the multiplicand is 0 or the bit, b_j, in the multiplier is 0. The bypass logics are added into the necessary FA to form a correct adder cell (AC) [2]. The components used in the Braun 2-dimensional multiplier are full adder, AND gate, NOT gate as well as multiplexer. The 4-bit Braun 2-dimensional bypassing multiplier is illustrated in Fig 5.

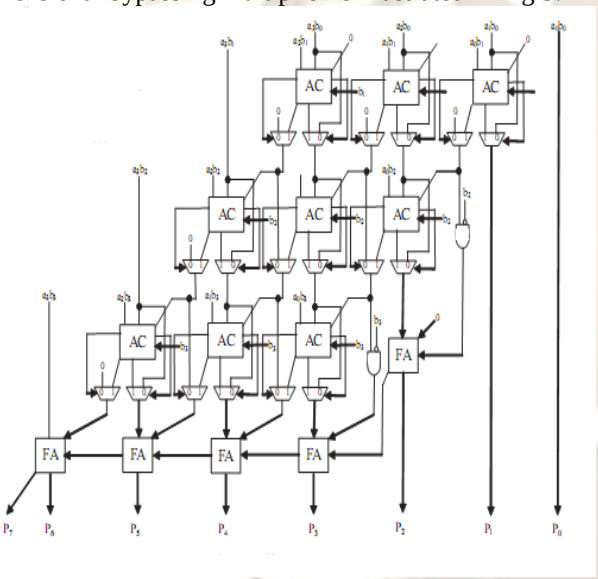
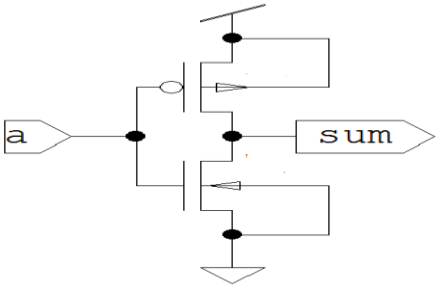


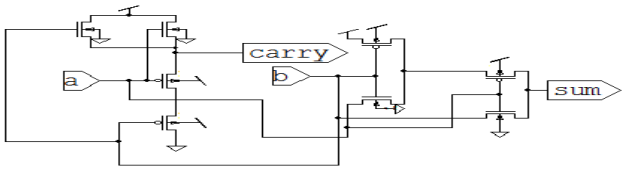
Fig 5: Braun 2-dimensional bypassing multiplier

4) Braun multiplier with row and column bypassing

In this bypassing technique, the carry bit in the (i+1, j)-th FA can be replaced by the AND operation of the product, a_ib_j, and the carry bit, $c_{i,j-1}$. For the addition operation in FA, the (i+1, j)-th FA, $1 < j < n$, can be replaced with the modified half adder, A+B+1, and the HAs in the first row of CSAs can be replaced with the incremental adder, A+1 be obtained [3]. The components used in the Braun multiplier with row and column bypassing are full adder, AND gate, tri-state buffer, multiplexer, OR gate, A+1 adder, A+B adder and A+B+1 adder. For A+1 adder, the carry output is the input itself. In Fig. 6, the logical circuits of A+1 adder and A+B+1 adder are shown.



(a) A+1 adder



(b) A+B+1 adder

Fig 6: Logical circuits of different blocks used in Braun multiplier with row and column bypassing.

IV. PHYSICAL LAYOUT DESIGN OF DIFFERENT BLOCKS OF MULTIPLIER DESIGNS

Integrated Circuit Layout or mask design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. In other words, Layout is the process by which a circuit specification is converted to a physical implementation with enough information to deduce all the relevant physical parameters of the circuit. A layout engineer's job is to place and connect all the components that make up a chip so that they meet all criteria [12]. The physical layout design of different blocks of Multiplier designs is done in MICROWIND Tool. The MICROWIND program design and simulate an integrated circuit at physical description level.

1) Layout Design of Full adder

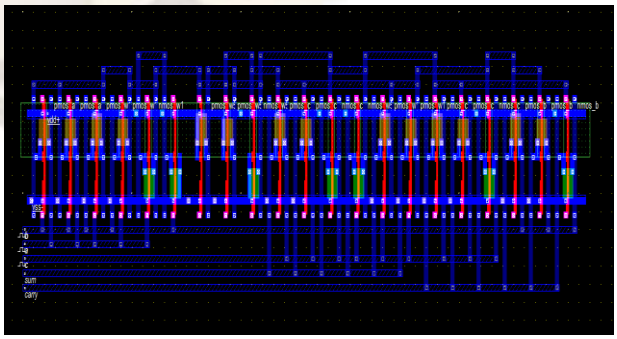


Fig 7: Full adder layout

2) Layout Design of A+B+1 Adder

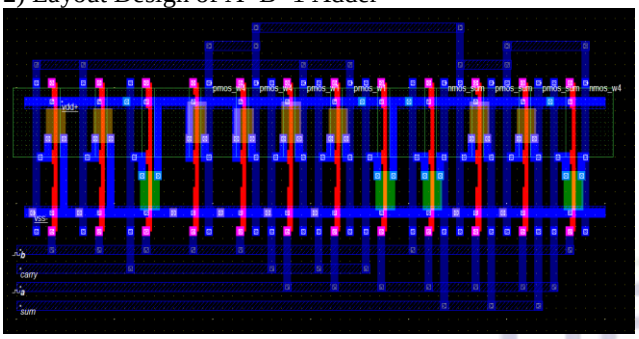


Fig 8: A+B+1 adder layout

3) Layout Design of Tri- state buffer

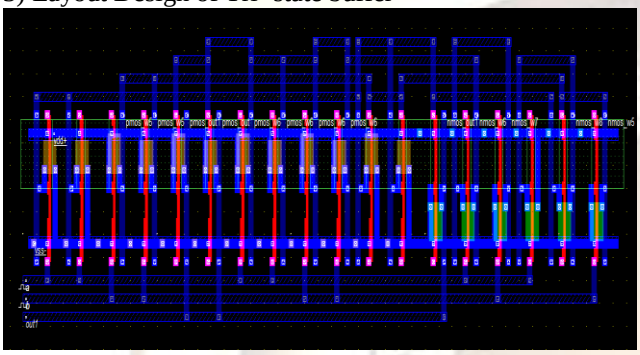


Fig 9: Tri- state buffer layout

4) Layout Design of Multiplexer

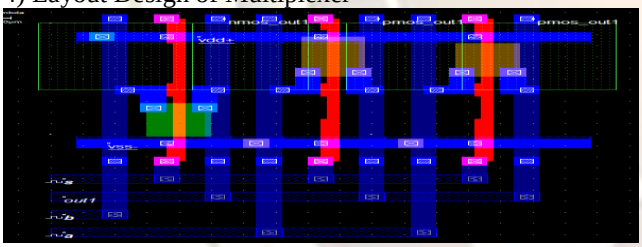


Fig 10: Multiplexer layout

5) Layout Design of A+1 adder

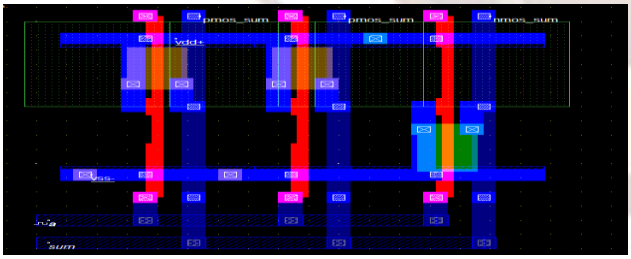


Fig 11: A+1 adder layout

V. CONCLUSION

From the comparison table I, it is clear that Braun 2-dimensional bypassing multiplier has least power consumption at 1GHz and also it is most effective in terms of area.

Table I. Comparative analysis of 4-bit multipliers

Multiplier name	Dynamic Power Consumption	Delay	Area
BRAUN MULTIPLIER	0.43mw	52ns	14666 μm^2
BRAUN MULTIPLIER WITH ROW BYPASSING	0.82mw	37ns	24821 μm^2
BRAUN MULTIPLIER WITH COLUMN BYPASSING	0.40mw	26ns	15354 μm^2
BRAUN 2-DIMENSIONAL BYPASSING MULTIPLIER	0.31mw	11ns	13863 μm^2
BRAUN MULTIPLIER WITH ROW AND COLUMN BYPASSING	0.49mw	85ns	16895 μm^2
WALLACE TREE MULTIPLIER	4.19mw	4.32ns	27767 μm^2

VI. SIMULATION AND COMPARISON

A. SIMULATION ENVIRONMENT: Braun multiplier designs based on Row and Column bypassing techniques are simulated in MICROWIND tool. All the results are obtained in 120nm CMOS process technology.

B. COMPARISON: Row and Column bypassing based multipliers are compared on the basis of the parameters like dynamic power consumption, delay as well as area. Comparative analysis of 4-bit multipliers using Row and Column bypassing techniques working at 1GHz is done with Wallace tree multiplier [11] as shown in the table I.

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