D.Sree Vani, K.Gopala Krishna/ International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 3, May-Jun 2012, pp.2723-2733

A Fast-Acting DC-Link Voltage Controller for Three-Phase DSTATCOM to Compensate AC and DC Loads USING FUZZY LOGIC

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ABSTRACT

The transient response of the distribution static compensator (DSTATCOM) is very important while compensating rapidly varying unbalanced and nonlinear loads. Any change in the load affects the dc-link voltage directly. The sudden removal of load would result in an increase in the dc-link voltage above the reference value, whereas a sudden increase in load would reduce the dc-link voltage below its reference value. The proper operation of DSTATCOM requires variation of the dc-link voltage within the prescribed limits. Conventionally, a proportional-integral (PI) controller is used to maintain the dc-link voltage the reference value. It uses deviation of the capacitor voltage from its reference value as its input. However, the transient response of the conventional PI dc-link voltage controller is slow. In this paper, a fast-acting dc-link voltage controller based on the energy of a dc-link capacitor is proposed. Mathematical equations are given to compute the gains of the conventional controller based on fast-acting dc-link voltage controllers to achieve similar fast transient response. The detailed simulation and experimental studies are carried out to validate the proposed controller.

KEY WORDS—DC-link voltage controller, distribution static compensator (DSTATCOM), fast transient response, harmonics, load compensation, power factor, power quality (PQ), unbalance, voltage-source inverter (VSI).

1.INTRODUCTION

The proliferation of power electronic equipment, nonlinear and unbalanced loads has aggravagated the power-quality (PQ) problems in the power distribution net-work. They cause excessive neutral currents, overheating of electrical apparatus, poor power factor, voltage distortion, high levels of neutral-to-ground voltage,and interference with communication systems.The literature records the evolution of different custom power devices to mitigate the above power-quality problems by injecting voltages/currents or both into the system .The shunt-connected custom power device, called the distribution static compensator (DSTATCOM), injects current at the point of common coupling (PCC) so that harmonic filtering, power factor correction, and load balancing can be achieved. The DSTATCOM consists of a current-controlled voltage-source inverter (VSI) which injects current at the PCC through the interface inductor. The operation of VSI is supported by a dc storage capacitor with proper dc voltage across it.One important aspect of the compensation is the extraction of reference currents. Various control algorithms are available in literature to compute the reference compensator currents. However, due to the simplicity in formulation and no confusion regarding the definition of powers, the control algorithm based on instantaneous symmetrical component theory is preferred. Based on this algorithm, the compensator reference currents $(i_{fa}^*, i_{fb}^*, i_{fc}^*)$ are given as follows:

$$\left.\begin{aligned} i_{fa}^* &= i_{la} - \frac{v_{sa}+\gamma(v_{sb}-v_{sc})}{\sum_{i=a,b,c} v_{si}^2}(P_{\text{lavg}}+P_{\text{dc}}) \\ i_{fb}^* &= i_{lb} - \frac{v_{sb}+\gamma(v_{sc}-v_{sa})}{\sum_{i=a,b,c} v_{si}^2}(P_{\text{lavg}}+P_{\text{dc}}) \\ i_{fc}^* &= i_{lc} - \frac{v_{sc}+\gamma(v_{sa}-v_{sb})}{\sum_{i=a,b,c} v_{si}^2}(P_{\text{lavg}}+P_{\text{dc}}) \end{aligned}\right\} \quad (1)$$

where $\gamma = \tan\phi/\sqrt{3}, \phi$ is the desired phase angle between the supply voltages and compensated source currents in the respective phases. For unity power factor operation $\Phi=0$ thus $\gamma=0$. The term $\boldsymbol{P_{lavg}}$ is the d c or average value of the load power. The term P_{DC} in (1) accounts for the losses in the VSI without any dc loads in its dc link. To generate P_{DC}, a suitable closed-loop dc-link voltage controller should be used, which will regulate the dc voltage to the reference value.

For the DSTATCOM compensating unbalanced and non-linear loads, the transient performance of the compensator is decided by the computation time of

average load power and losses in the compensator. In most DSTATCOM applications, losses in the VSI are a fraction of the average load power. Therefore, the transient performance of the compensator mostly depends on the computation of P_{DC}. In this paper, P_{lavg} is computed by using a moving average filter (MAF) to ensure fast dynamic response. The settling time of the MAF is a half-cycle period in case of odd harmonics and one cycle period in case of even harmonics presence in voltages and currents. Although the computation of P_{DC} is generally slow and updated once or twice in a cycle, being a small value compared to P_{lavg}, it does not play a significant role in transient performance of the compensator.

In some of the electric power consumers, such as the telecommunications industry, power-electronics drive applications, etc., there is a requirement for ac as well as dc loads. The telecommunication industry uses several parallel-connected switch-mode rectifiers to support dc bus voltage. Such an arrangement draws nonlinear load currents from the utility. This causes poor power factor and, hence, more losses and less efficiency. Clearly, there are PQ issues, such as unbalance, poor power factor, and harmonics produced by telecom equipment in power distribution networks. Therefore, the functionalities of the conventional DSTATCOM should be increased to mitigate the aforementioned PQ problems and to supply the dc loads from its dc link as well. The load sharing by the ac and dc bus depends upon the design and the rating of the VSI. This DSTATCOM differs from conventional one in the sense that its dc link not only supports instantaneous compensation but also supplies dc loads.

However, when the dc link of the DSTATCOM supplies the dc load as well, the corresponding dc power is comparable to the average load power and, hence, plays a major role in the transient response of the compensator. Hence, there are two important issues. The first one is the regulation of the dc-link voltage
within prescribed limits under transient load conditions. The second one is the settling time of the dc-link voltage controller. Conventionally, a PI controller is used to maintain the dc-link voltage. It uses the deviation of the capacitor voltage from its reference value as its input. However, the transient response of the conventional dc-link voltage controllers is slow, especially in applications where the load changes rapidly. Some work related to dc-link voltage controllers and their stability is reported.

However, the work is limited to rectifier units where switching patterns are well defined and analysis can be easily carried out. In this paper, a fast-acting dc-link voltage controller based on the dc-link capacitor energy is proposed. The detailed modeling, simulation, and experimental verifications are given to prove the efficacy of this fast-acting dc-link voltage controller. There is no systematic procedure to design the gains of the conventional PI controller used to regulate the dc-link voltage of the DSTATCOM. Herewith, mathematical equations are given to design the gains of the conventional controller based on the fast-acting dc-link voltage controllers to achieve similar fast transient response.

2. DSTATCOM FOR COMPENSATING AC AND DC LOADS

Various VSI topologies are described in the literature for realizing DSTATCOM to compensate unbalanced and nonlinear loads. Due to the simplicity, the absence of unbalance in the dc-link voltage and independent current tracking with respect to other phases, a three-phase H-bridge VSI topology is chosen. Fig. 1 shows a three-phase, four-wire-compensated system using an H-bridge VSI topology-based DSTATCOM compensating unbalanced and nonlinear ac load. In addition to this, a dc load is connected across the dc link. The DSTATCOM consists of 12 insulated-gate biploar transistor(IGBT) switches each with an antiparallel diode, dc storage capacitor, three isolation transformers, and three interface inductors. The star point of the isolation transformers is connected to the neutral of load*(n)*and source (*N*). The H-bridge VSIs are connected to the PCC through interface inductors. The isolation transformers prevent a short circuit of the dc capacitor for various combinations of the switching states of the VSI. The inductance and resistance of the isolation transformers are also included in L_f and R_f. The source voltages are assumed to be balanced and sinusoidal. With the supply being considered as a stiff source, the feeder impedance (L_S-R_S) shown in Fig.1 is negligible and, hence, it is not accounted in state-space modeling. To track the desired compensator currents, the VSIs operate under the hysteresis band current control mode due to their simplicity, fast response, and being independent of the load parameters. The DSTATCOM injects currents into the PCC in such a way as to cancel unbalance and harmonics in the load currents. The VSI operation is supported by the dc storage capacitor with voltage v_{dc} across it. The dc bus voltage has two functions, that is, to support the compensator operation and to supply dc load. While compensating, the DSTATCOM maintains the balanced sinusoidal source currents with unity power factor and supplies the dc load through its dc bus.

3. STATE-SPACE MODEL OF THE DSTATCOM

For the DSTATCOM topology shown in Fig. 1, the pairs of switches S_{1a}-S_{2a} and S_{3a}-S_{4a} are always ON and

OFF in complimentary mode. The ON and OFF states of these switches are represented by a binary logic variable S_a and it complement $\hat{S}a$. Thus, when switches S_{1a}-S_{2a} are ON, it implies that switches S_{4a}-S_{3a} are OFF. This is represented by S_a=1 and $\hat{S}_a$=0 and vice versa. In a similar way, S_b, $\hat{S}_b$ S_c and $\hat{S}_c$ represent gating signals for switches S_{1b}-S_{2b}, S_{4b}-S_{3b}, S_{1c}-S_{2c}, S_{4c}-S_{3c}, respectively. Using these notations for the system shown in Fig. 1, the state-space equations are written as follows:

$$\dot{x} = Ax + Bu \quad (2)$$

where state vector x and input vector u are given by

$$x = [i_{fa} \quad i_{fb} \quad i_{fc} \quad v_{dc}]^{\Gamma} \quad (3)$$

$$u = [v_{sa} \quad v_{sb} \quad v_{sc}]^{\Gamma} \quad (4)$$

where the superscript Γ stands for the transpose operator. System matrix *(A)* and input matrix *(B)* are given as follows:

$$A = \begin{bmatrix} -\frac{R_f}{L_f} & 0 & 0 & \frac{(S_a-\hat{S}_a)}{L_f} \\ 0 & -\frac{R_f}{L_f} & 0 & \frac{(S_b-\hat{S}_b)}{L_f} \\ 0 & 0 & -\frac{R_f}{L_f} & \frac{(S_c-\hat{S}_c)}{L_f} \\ -\frac{(S_a-\hat{S}_a)}{C_{dc}} & -\frac{(S_b-\hat{S}_b)}{C_{dc}} & -\frac{(S_c-\hat{S}_c)}{C_{dc}} & -\frac{1}{R_{dc}C_{dc}} \end{bmatrix} \quad (5)$$

$$B = \begin{bmatrix} \frac{1}{L_f} & 0 & 0 \\ 0 & \frac{1}{L_f} & 0 \\ 0 & 0 & \frac{1}{L_f} \\ 0 & 0 & 0 \end{bmatrix}. \quad (6)$$

Using the above state-space model, the system state variables
(x) are computed at every instant.

4. DC-LINK VOLTAGE CONTROLLERS

As mentioned before, the source supplies an unbalanced non-linear ac load directly and a dc load through the dc link of the DSTATCOM, as shown in Fig. 1. Due to transients on the load side, the dc bus voltage is significantly affected. To regulate this dc-link voltage, closed-loop controllers are used. The proportional-integral-derivative (PID) control provides a generic and efficient solution to many control problems. The control signal from PID controller to regulate dc link voltage is expressed as

$$u_c = K_p\,(V_{dc\,ref} - v_{dc}) + K_i \int (V_{dc\,ref} - v_{dc})dt + K_d\, d(V_{dc\,ref} - v_{dc})/dt. \quad (7)$$

In (7), K_p, K_i, and K_d, are proportional,integral, and derivative gains of the PID controller, respectively. The proportional term provides overall control action proportional to the error signal. An increase in proportional controller gain K_p reduces rise time and steady-state error but increases the overshoot and settling time. An increase in integral gain K_i reduces steady-state error but increases overshoot and settling time. Increasing derivative gain (K_d) will lead to improved stability. However, practitioners have often found that the derivative term can be-have against anticipatory action in case of transport delay. A cumbersome trial-and-error method to tune its parameters made many practitioners switch off or even exclude the derivative term [31], [32]. Therefore, the description of conventional and the proposed fast-acting dc-link voltage controllers using PI controllers are given in the following subsections.

4.1 Conventional DC-Link Voltage Controller

The conventional PI controller used for maintaining the dc-link voltage is shown in Fig. 2.To maintain the dc-link voltage at the reference value, the dc-link capacitor needs a certain amount of real power, which is proportional to the difference between the actual and reference voltages. The power required by the capacitor can be expressed as follows:

$$P_{dc} = K_p(V_{dc\,ref} - v_{dc}) + K_i \int (V_{dc\,ref} - v_{dc})dt. \quad (8)$$

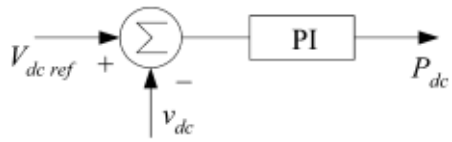


Fig. 2. Schematic diagram of the conventional dc-link voltage controller.

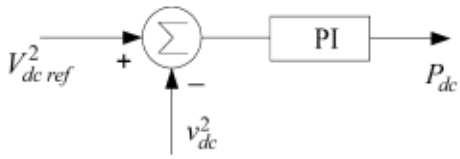


Fig. 3. Schematic diagram of the fast-acting dc-link voltage controller.

The dc-link capacitor has slow dynamics compared to the compensator, since the capacitor voltage is sampled at every zero crossing of phase *a* supply voltage. The sampling can also be performed at a quarter cycle depending upon the symmetry of the dc-link voltage waveform. The drawback of this conventional controller is that its transient response is slow, especially for fast-changing loads. Also, the design of PI controller parameters is quite difficult for a complex system and, hence, these parameters are chosen by trial and error. Moreover, the dynamic response during the transients is totally dependent on the values of K_P and K_i when P_{dc} is

comparable to P_{lavg}.

4.2. Fast-Acting DC Link Voltage Controller

To overcome the disadvantages of the aforementioned controller, an energy-based dc-link voltage controller is proposed. The energy required by the dc-link capacitor **(W_{dc})** to charge from actual voltage (v_{dc}) to the reference value (v_{dcref}) can be computed as.

$$W_{dc} = \frac{1}{2}C_{dc}\left(V_{dc\,ref}^2 - v_{dc}^2\right). \quad (9)$$

In general, the dc-link capacitor voltage has ripples with double frequency, that of the supply frequency. The dc power (P'_{dc}) required by the dc-link capacitor is given as

$$P'_{dc} = \frac{W_{dc}}{T_c} = \frac{1}{2T_c}C_{dc}\left(V_{dc\,ref}^2 - v_{dc}^2\right) \quad (10)$$

where T_C is the ripple period of the dc-link capacitor voltage. Some control schemes have been reported. However, due to the lack of integral term, there is a steady-state error while compensating the combined ac and dc loads. This is eliminated by including an integral term. The input to this controller is the error between the squares of reference and the actual capacitor voltages. This controller is shown in Fig. 3 and the total dc power required by the dc-link capacitor is computed as follows:

$$P_{dc} = K_{pe}\left(V_{dc\,ref}^2 - v_{dc}^2\right) + K_{ie}\int\left(V_{dc\,ref}^2 - v_{dc}^2\right)dt. \quad (11)$$

The coefficients K_{pe} and K_{ie} are the proportional and integral As an energy-based controller, it gives fast response compared to the conventional PI controller. Thus, it can be called a fast-acting dc-link voltage controller. The ease in the calculation of the proportional and integral gains is an additional advantage. The value of the proportional controller gain K_{pe} can be given as gains of the proposed energy-based dc-link voltage controller.

$$K_{pe} = \frac{C_{dc}}{2T_c}. \quad (12)$$

For example, if the value of dc-link capacitor is 2200 μF and the capacitor voltage ripple period as 0.01s, then K_{pe} is computed as 0.11 by using (12). The selection of K_{ie} depends upon the tradeoff between the transient response and overshoot in the compensated source current. Once this proportional gain is selected, integral gain is tuned around and chosen to be 0.5. It is found that if K_{ie} is greater than $K_{pe}/2$, the response tends to be oscillatory and if K_{ie} is less than $K_{pe}/2$, then response tends to be sluggish. Hence, K_{ie} is chosen to be $K_{pe}/2$.

5. DESIGN OF CONVENTIONAL CONTROLLER BASED ON THE FAST-ACTING DC-LINK VOLTAGE CONTROLLER

The conventional dc-link voltage controller can be designed based on equations given for the fast-acting dc-link voltage controller as in (11) and can be written as

$$P_{dc} = K_{pe}(V_{dc\,ref} + v_{dc})(V_{dc\,ref} - v_{dc}) + K_{ie}\int(V_{dc\,ref} + v_{dc})(V_{dc\,ref} - v_{dc})dt. \quad (13)$$

It can also be written as

$$P_{dc} = K'_p(V_{dc\,ref} - v_{dc}) + K'_i\int(V_{dc\,ref} - v_{dc})dt \quad (14)$$

Where

$$K'_p = K_{pe}(V_{dc\,ref} + v_{dc}) \quad (15)$$

$$K'_i = K_{ie}(V_{dc\,ref} + v_{dc}). \quad (16)$$

It is observed from the aforementioned equations that the gains of proportional and integral controllers vary with respect to time. However, for small ripples in the dc-link voltage, $V_{dc} \approx V_{dcref}$, therefore, we can approximate the above gains to the following

$$K'_p \approx 2K_{pe}V_{dc\,ref} \quad (17)$$

$$K'_i \approx 2K_{ie}V_{dc\,ref}. \quad (18)$$

The relations (17)-(18) give approximate gains for a conventional PI controller. This is due to the fact that $V_{dcref} + V_{dc}$ is not really equal to $2V_{dcref}$ until variation in V_{dc} is small during transients. Hence, the designed conventional PI controller works only on approximation. The open-loop gains for the two cases are given by:

$$\frac{P_{dc}}{E_{er}} = \frac{K_{pe}(s + K_{ie}/K_{pe})}{s} \quad (19)$$

TABLE I
SIMULATION PARAMETERS

System Parameters	Values
supply voltage	400 V (L-L), 50 Hz
Unbalanced load	Z_a = 25 Ω, Z_b = 44 + j25.5 Ω and Z_c = 50 + j86.6 Ω
Nonlinear load	Three-phase full wave rectifier drawing a dc current of 5 A
DC load	R_{dc} = 100 Ω
DC capacitor	C_{dc} = 2000 μF
Interface inductor	L_f = 26 mH, R_f = 0.25 Ω
Reference dc link voltage	$V_{dc\,ref}$ = 520 V
Hysteresis band	±h = 1.0 A
Gains of conventional dc link voltage controller	K_p = 40, K_i = 20
Gains of fast acting dc link voltage controller	K_p = 0.11, K_i = 0.055

where $E_{er} = V_{\text{dcref}}^2 - v_{\text{dc}}^2$ and

$$\frac{P_{\text{dc}}}{E_r} = \frac{K_p'(s + K_i'/K_p')}{s} \quad (20)$$

Where $E_r = V_{\text{dcref}} - V_{\text{dc}}$. Since K_i'/K_P' is the same as K_{ie}/K_{pe}, the higher gain in the conventional PI controller renders less stability than that of the proposed energy-based dc-link controller. For nearly the same performance, the conventional PI controller has gains which are 364 (40/0.11 from Table I) times larger than that of that proposed one. Also, the amplifier units used to realize these gains need more design considerations and are likely to saturate when used with higher gains.

6.SELECTION OF THE DC-LINK CAPACITOR

The value of the dc-link capacitor can be selected based on its ability to regulate the voltage under transient conditions. Let us assume that the compensator in Fig. 1 is connected to a system with the rating of X kilovolt amperes. The energy of the system is given by $X \times 100$ J/s. Let us further assume that the compensator deals with half (i.e., $X/2$) and twice (i.e., $2X$) capacity under the transient conditions for cycles with the system voltage period of T s. Then, the change in energy to be dealt with by the dc capacitor is given as

$$\Delta E = (2X - X/2)nT. \quad (21)$$

Now this change in energy (21) should be supported by the energy stored in the dc capacitor. Let us allow the dc capacitor to change its total dc-link voltage from $1.4V_m$ to $1.8V_m$ during the transient conditions where V_m is the peak value of phase voltage. Hence, we can write

$$\frac{1}{2}C_{\text{dc}}[(1.8\,V_m)^2 - (1.4\,V_m)^2] = (2X - X/2)nT \quad (22)$$

Which implies that

$$C_{\text{dc}} = \frac{3XnT}{(1.8\,V_m)^2 - (1.4\,V_m)^2}. \quad (23)$$

For example, consider a 10-kVA system (i.e., X = 10 kVA), system peak voltage V_m = 325.2 V, n = 0.5, and T = 0.02 s. The value of C_{dc} computed using (23) is 2216 µF. Practically, 2000 µF is readily available and the same value has been taken for simulation and experimental studies.

7. SIMULATION STUDIES

The load compensator with H-bridge VSI topology as shown in Fig. 1 is realized by digital simulation by using MATLAB. The load and the compensator are connected at the PCC. The ac load consists of a three-phase unbalanced load and a three-phase diode bridge rectifier feeding a highly inductive R-L load. A dc load is realized by an equivalent resistance (R_{dc}) as shown in the figure. The dc load forms 50% of the total power requirement. The system and compensator parameters are given in Table I.

By monitoring the load currents and PCC voltages, the average load power is computed. At every zero crossing of phase *a* voltage, P_{dc} is generated by using the dc-link voltage controller. The state-space equations are solved to compute the actual compensator currents and dc-link voltage. These actual currents are compared with the reference currents given by (1) using hysteresis current control. Based on the comparison, switching signals are generated to compute the actual state variables by solving the state-space model given in (2). The source voltages and load currents are plotted in Fig. 4(a) and (b). The load currents have total harmonic distortions of 8.9%, 14.3%, and 21.5% in phases *a*, *b* and *c*, respectively. The unbalance in load currents results in neutral current as illustrated in the figure.

The compensator currents and compensated source currents are shown in Fig. 4(c) and (d). As seen from Fig. 4(d), the source currents are balanced sinusoids; however, the switching frequency components are superimposed over the reference currents due to the switching action of the VSI. The currents have a unity power factor relationship with the voltages in the respective phases. The THDs in these currents are 3.6%, 3.7%, and 3.9% in phases *a*, *b* and *c*, respectively. There are notches in the source currents due to finite baniddwth of the VSI.

The transient performance of the conventional and fast-acting dc-link voltage controllers are studied by making sudden changes in the ac load supplied by the ac load bus as well as the dc load supplied by the dc link. In the simulation study, the load is halved at the instant t = 0.4 s and brought back to full load at t = 0.8 s. The transient performance is explained in the following subsections.

7.1 Transient Performance of Conventional DC-Link Voltage Controller

The conventional dc-link voltage controller as given in (8) is used to generate the dc load power P_{dc} which is inclusive of losses in the inverter The transient performance of the compensator is shown in Fig. 5(a) and (b). The total load, which is a combination of linear unbalanced and nonlinear load (as given in Table I), is halved at the instant t = 0.4 s. Due to a sudden reduction in the load, the dc-link

capacitor absorbs surplus power from the source. Therefore, there is an increase in dc-link capacitor voltage above the reference value. Based on the values of PI controller gains, the dc-link capacitor voltage controller will be brought back to the reference value after a few cycles.

Similarly, when the load is switched back to the full load at instant $t = 0.8$ s, the dc capacitor supplies power to the load momentarily and, hence, the dc-link voltage falls below the reference value. Due to the PI controller action, the capacitor voltage will gradually build up and reach its reference value. If gains of the conventional dc-link voltage controller are not properly chosen, the dc-link voltage would have undesirable overshoot and considerably large settling time. Consequently, the performance of the load connected to the dc link also gets affected due to the above factors. It can be observed from Fig. 5(a) and (b) that the conventional dc-link voltage controller takes about a ten cycle period to reach the reference voltage during load transient. This is indicated by time duration in these figures.

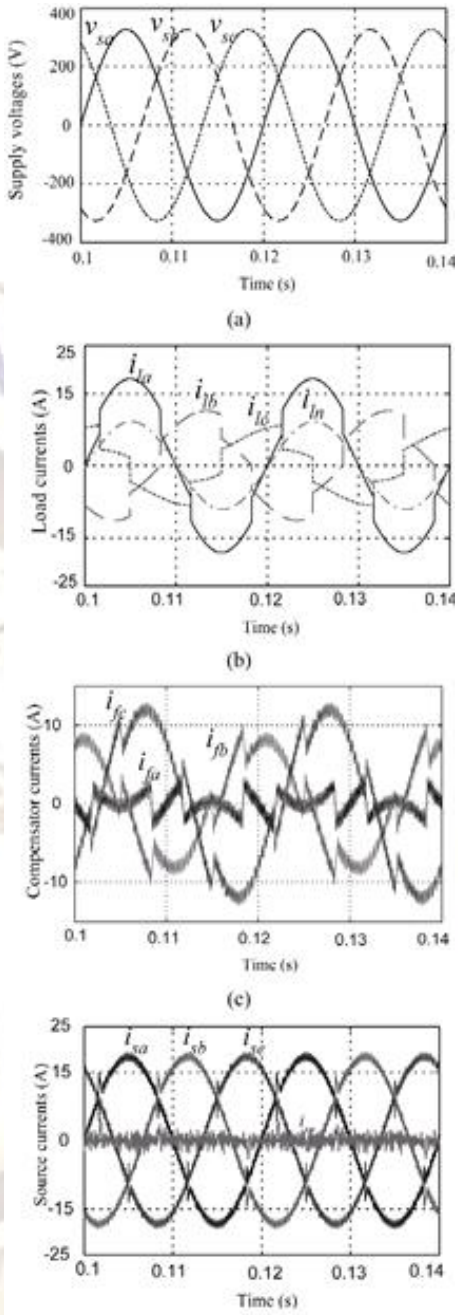


Fig. 4. (a) Supply voltages. (b) Load currents. (c) Compensator currents. (d) Compensated source currents

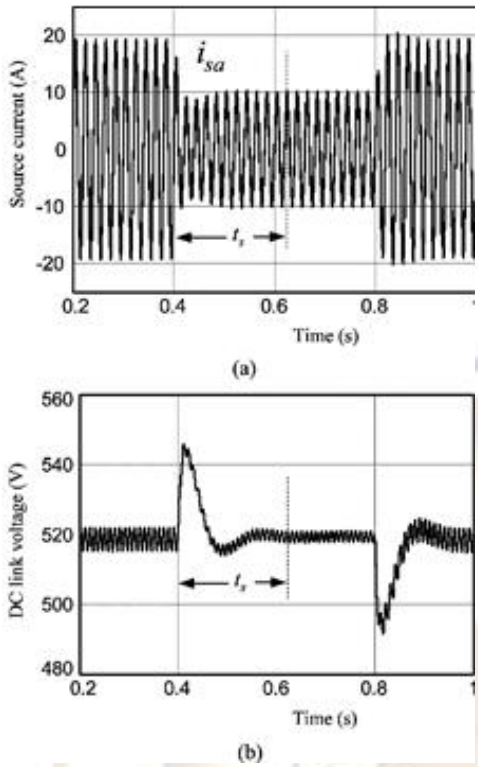


Fig. 5.Transient response of the conventional controller. (a) Compensated source current in phase a . (b) DC-link voltage.

7.2.Transient Performance of Fast-Acting DC-Link Voltage Controller.

The dc load power P_{dc} is computed by using the fast-acting dc-link voltage controller as given in (11). Transients in the load are considered the same as in the above simulation study Fig. 6(a) and (b) illustrates the phase *a* source current and dc-link capacitor voltage during the load transients.At the instant t = 0.4 s, the capacitor voltage increases due to the sudden removal of the load. The fast-acting dc-link voltage controller takes action at the instant t = 0.41 s. This is because the controller output is updated at every half cycle. It computes the dc load power needed to bring the capacitor voltage to the reference value in a half cycle. Therefore, the dc-link voltage reaches its reference voltage at the instant t = 0.42 s. When the dc-link voltage is more than the reference value, P_{dc} is less. Therefore, the source currents are less in magnitude. At the instant t = 0.8 s, the dc-link voltage falls below the reference voltage due to a sudden increase in load. As explained earlier, the fast-acting controller brings the dc-link voltage toits reference value at t = 0.82 s with almost the same rise in 0voltage as that of the conventional dc-link voltage as that

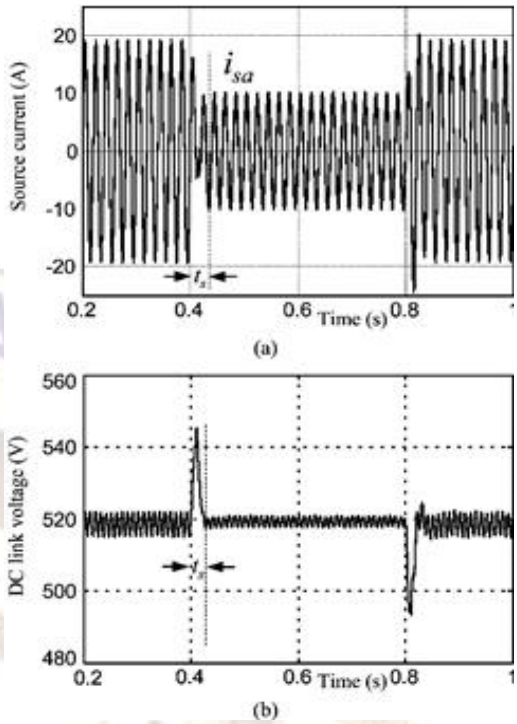


Fig. 6.Transient response of the fast-acting controller. (a) Compensated source current in phase a. (b) DC-link voltage.

of the conventional dc-link voltage controller can regulate the capacitor voltage with a half cycle period which is indicated by t_s.Owing to its good transient performance, it is preferred over the conventional dc-link voltage controller.

8. EXPERIMENTAL STUDIES

To verify the effectiveness of the proposed energy based dc link voltage controller for the DSTATCOM, a three-phase prototype model has been developed in the laboratory. The overall block diagram of the hardware set-up is shown in Fig. 7(a), the control hardware setup is shown in Fig. 7(b) and the power circuit of the DSTATCOM is shown in Fig.7(c). The three-phase power quantities (voltages and currents) are converted to low-level voltage signals using the Hall effect voltage and current transducers. These signals are further conditioned by using signal conditioning circuits and are given to the analog-to-digital converter (ADC) channels of the digital signal processor(DSP) TMS320F2812PGFA. The DSP also receives a signal from the synchronizing circuit to realize reference quantities in time domain. The DSP is connected to the host computer through a parallel port. The control algorithm in the DSP generates switching pulses to the VSI. These pulses are then passed through the blanking circuit to include dead time in order to prevent the short circuit of the capacitor through

switches in the same VSI leg. The blanking circuit also receives STOP signals from the protection circuit to ensure safe operation of the DSTATCOM in case of any abnormality in the system. The blanking circuit output pulses are given to the VSI through the optoisolator circuit to isolate the high-power network and the signal-level circuits.

The ac load consists of a three-phase unbalanced load and a three-phase diode bridge rectifier feeding a highly inductive R-L load. A resistance connected in the dc link is considered as dc load. The compensator consists of 12 IGBT switches each with antiparallel diodes in two intelligent power mod-ules (PM50RVA120), three isolation transformers, and three external interface inductors. The system parameters for the experimental setup are given in Table II.

The average load power is computed by taking the samples of the load currents and PCC voltages. The dc load power (Pdc) is generated by using the conventional dc-link voltage controller and fast-acting dc-link voltage controllers. Based on these values, reference compensator currents are obtained by using (1).

The VSI is then operated in the hysteresis band current control mode to synthesize the actual compensator currents. Accordingly, the switching commands are issued to control IGBT switches through proper interfacing circuits.

The source voltages and load currents are shown in Fig.8(a) and (b), respectively. The source voltages are balanced and sinusoidal but the load currents have both unbalance and distortions. The unbalance in load currents results in neutral current. The THDs of the load currents are 11.6%, 16.7%, and 24.2% in phases *a*, *b* and *c*, respectively. Compensator and compensated source currents are shown in Fig. 8(c) and (d) respectively. The source currents are balanced sinusoids with the THDs of 5.2%, 4.8%, and 4.7% in phases *a*, *b* and *c*, respectively.

8.1Transient Performance of the Conventional DC-Link Voltage Controller

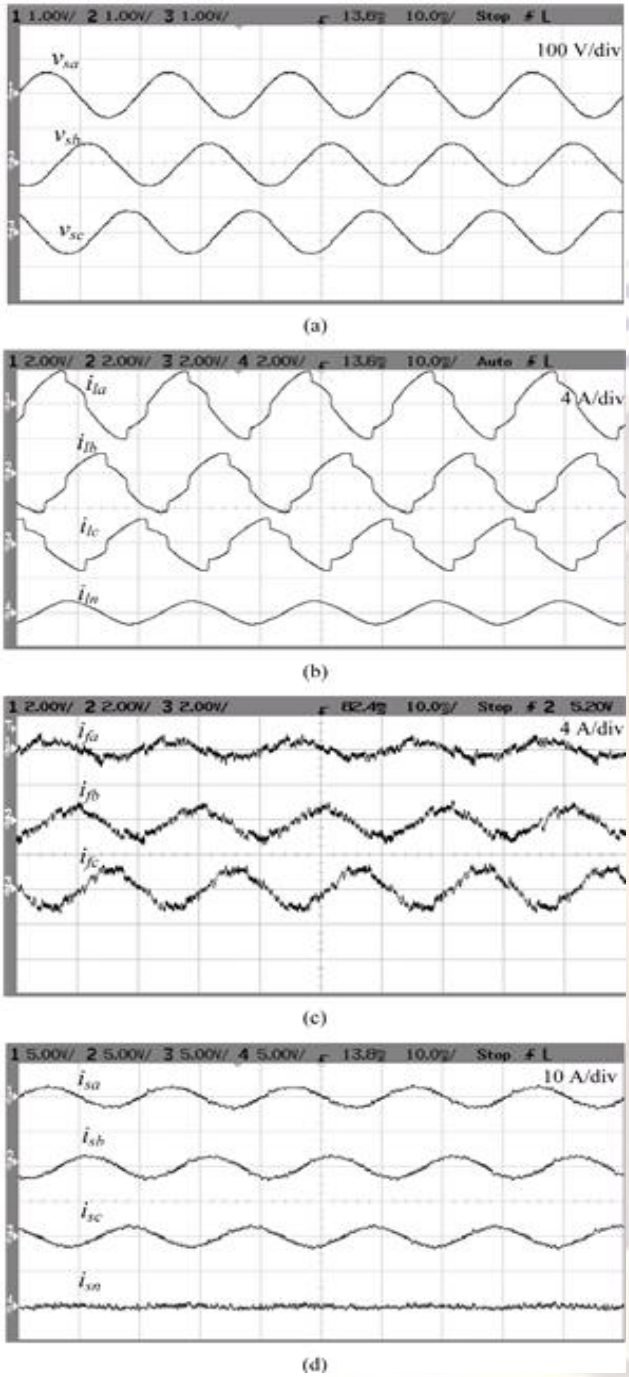
The transient performance with the conventional dc-link voltage controller is shown in Fig. 9. At an instant $t = t_1$, the unbalanced linear R-L load and a half dc load are removed. the unbalanced linear R-L load and a half dc load are removed. At $t = t_2$ the load is brought to its original value. The power P_{dc} required by the dc link is computed by using (8). Fig. 9 illustrates the compensated source currents and dc-link voltage. From this figure, it can be understood that the use of the conventional controller with an improper value of controller gains cannot bring the actual dc-link voltage to its reference value quickly. It takes around 40 cycles to regulate the dc-link voltage to its reference voltage.

8.2. Transient Performance of Fast-Acting DC-Link Voltage Controller

The performance of the fast-acting dc-link voltage controller is tested by using the transient load used in the previous section. Fig. 10 shows the source currents during the transients in load by using this fast-acting dc-link voltage controller as given in (11). From the close observation of the figure, it is found that the response time is very less compared to that of the conventional dc-link voltage controller. Though, in simulation studies, the fast-acting voltage controller corrects the actual dc-link voltage in a half cycle, the experimental results do not fully validate the same. This is due to the use of the mechanical switch for the change of load, which cannot connect/disconnect the load in all three phases simultaneously at the instants t_1 and t_2, and due to other nonidealities in the system.

10. CONCLUSION

A VSI topology for DSTATCOM compensating ac unbalanced and nonlinear loads and a dc load supplied by the dc link of the compensator is presented. The state-space modeling of the DSTATCOM is discussed for carrying out the simulation studies. An energy-based fast-acting dc-link voltage controller is suggested to ensure the fast transient response of the compensator. Mathematical equations are developed to compute the gains of this controller. The efficacy of the proposed controller over the conventional dc-link voltage controller is established through the digital simulation and experimental studies. It is observed from these studies that the proposed dc-link voltage controller gives fast transient response under load transients.



(a) (b) (c) (d)

Fig.8(a)Supply voltages.(b)Load currents.(c) Compensator currents.(d) Source currents after compensation

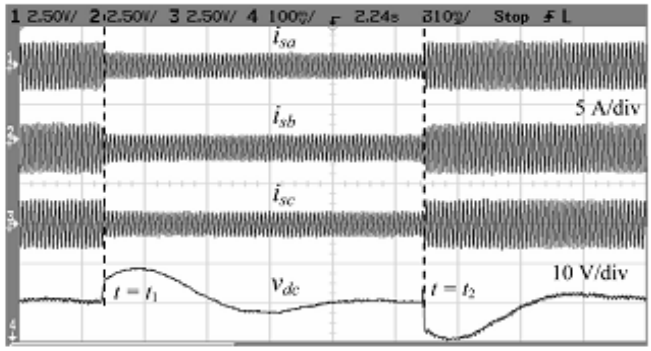


Fig. 9. Source currents and dc-link voltage with a conventional dc-link voltage controller.

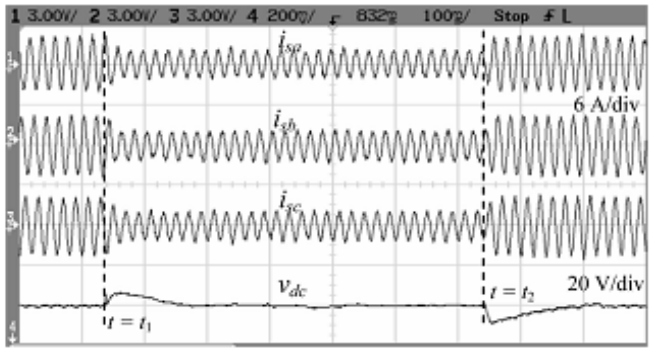


Fig. 10. Source currents and dc-link voltage with a fast-acting dc-link voltage controller.

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