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POWER FACTOR CORRECTION BY USING AC/DC CONVERTER WITH QUASI-ACTIVE SCHEME

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Abstract—*This letter presents a novel ac/dc converter based on a quasi-active power factor correction (PFC) scheme. In the proposed circuit, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc fly back converter. The auxiliary winding is placed between the input rectifier and the low-frequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since the dc/dc converter is operated at high-switching frequency, the auxiliary windings produce a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. It eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher efficiency. In order to achieve low harmonic content, the input inductor is designed to operate in discontinuous current mode. Operating principles, analysis, and experimental results of the proposed method are presented.*

Index Terms —AC/DC converter, power factor correction, single stage.

I. NTRODUCTION

CONVENTIONAL offline power converters with distorted input current waveforms with high harmonic contents. To solve these problems, so as to comply with the harmonic standards such as IEC 61000-3-2, several techniques have been proposed to shape the input current waveform of the power converter. A common approach to improving the power factor is a two-stage power conversion approach. The two-stage scheme results in high power factor and fast response output voltage by using two independent controllers and optimized power stages. The main drawbacks of this scheme are its relatively higher cost and larger size and particularly in low power applications. In order to reduce the cost, the single-stage approach, which integrates the PFC stage with a dc/dc converter into one stage, is developed [1]–[11].These integrated single-stage power factor correction (PFC) converters usually use a boost converter to achieve PFC with discontinuous current mode (DCM) operation.

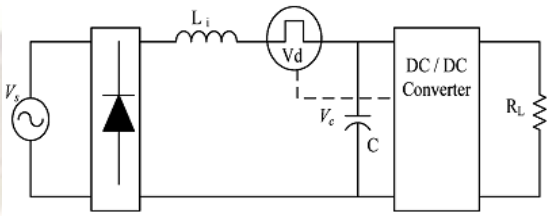


Fig1.General circuit diagram of dither rectifier with PFC cell.

operation gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode (CCM). However, the CCM operation yields s lightly higher efficiency compared to the DCM operation.

Generally, single-stage PFC converters meet the regulatory requirements regarding the input current harmonics, but they do not improve the power factor and reduce the THD as much as their conventional two-stage counterpart. The power factor could be as low as 0.8, however, they still meet the regulation. The single-stage scheme is especially attractive in low cost and low power applications due to its simplified power stage and control circuit [5], [6]. To overcome the disadvantages of the single-stage scheme, many converters with input current shaping have been presented [3]–[12]. Another technique based on parallel connection of this dither signal is presented in [13], however, the harmonic content can meet the regulatory standard by a small margin. A new concept of quasi-active PFC is proposed to improve the efficiency of a single-stage converter by preventing the input current or voltage stress due the PFC cell from being added to the active switch. In this circuit, the dc/dc cell operates in DCM so that a series of discontinuous pulses is used to shape the input inductor current and the PFC is achieved.

In this letter, a new technique of quasi-active PFC is proposed. As shown in Fig. 2, the PFC cell is formed by connecting the energy buffer (LB) and the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. an auxiliary winding (L3)coupled t the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter.

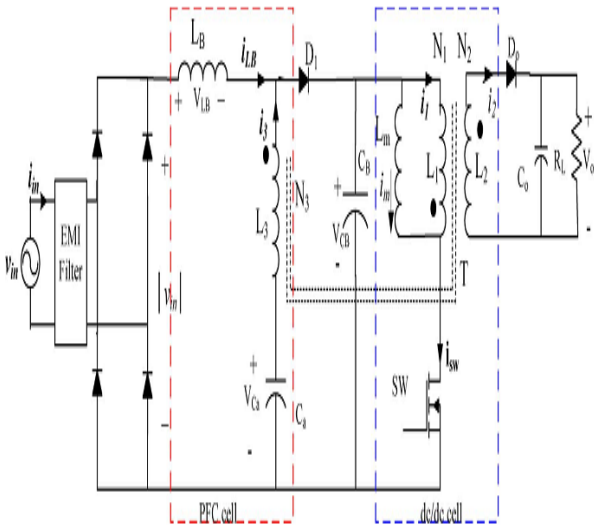


Fig. 2. Proposed quasi-active PFC circuit diagram. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. The input inductor LB operates in DCM such that a lower THD of the input current can be achieved. Design example and the experimental results are presented in Section III.

II. PROPOSED QUASI-ACTIVE PFC CIRCUIT

The proposed quasi-active PFC circuit is analyzed in this section. As shown in Fig. 2, the circuit comprised of a bridge rectifier, a boost inductor LB , a bulk capacitor Ca in series with the auxiliary windings L3 , an intermediate dc-bus voltage capacitor CB , and a discontinuous input current power load, such as fly-back converter. The fly back transformer (T) has three windings N1 ,N2 , and N3 . The secondary winding N2 =1 is assumed. In the proposed PFC scheme, the dc/dc converter section offers a driving power with high-frequency pulsating source. The quasi-active PFC cell can be considered one power stage but without an active switch.

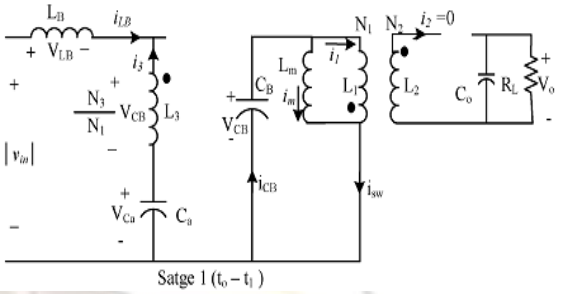
To simplify the analysis, the following assumptions have been made.

1) All semiconductors components are ideal. 2)The power transformer does not have the leakage inductances because of the ideal coupling.
3) All the capacitors are high enough so that the voltage across them is considered constant.
4) Finally, the input voltage of the converter is considered constant during as switching cycle because the switching frequency is much higher than the line frequency.

A. Principles of Operation of the Proposed Circuit

To facilitate the analysis of operation of stages and the key waveforms of the proposed circuit. It is assumed that both the input inductor LB and the magnetizing inductance of the fly back converter operate in DCM. Therefore, currents iLB ,im , and i2 are zero at the beginning of each switching period. It is also assumed that the average capacitor voltage VCa is greater than the average rectified input voltage |vin|. To ensure proper operation of the converter, the transformer's turns ratio should be (N1 /N3) ≥ 2 and the boost inductor LB <Lm .In steady-state operation, the topology can be divided into four operating stages.

1)Stage 1(to − t1):



When the s witch (SW) is turned on at t = to , diodes D1 and Do are OFF, therefore, the dc-bus voltage VCB is applied to the magnetizing inductor Lm , which causes the magnetizing current to linearly increases. This current can be expressed as

$$i_m = \frac{V_{CB}}{L_m}(t_o - t_1). \qquad (1)$$

And since diode D1 is OFF, the input inductor LB is charged by input voltage, therefore, the inductor current iLB is linearly increased from zero since it is assumed that the PFC cell operates in DCM. This current can be expressed as

$$i_{LB} = \frac{|V_{\text{in}}| + (N_3/N_1)V_{CB} - V_{Ca}}{L_B}(t_o - t_1) \qquad (2)$$

where, Vin = Vm | sin θ| is the rectified input voltage,(to − t1)= dTS is the ON-time of t he switch (SW), LB is the boost inductor and N1 , N3 are t he primary and auxiliary turns ratio, respectively. At this stage, iLB = −i3 and the capacitor Ca is in the charging mode. On the other hand, Do is reversed biased and there is no current flow through the secondary winding.

$$i_1 = \frac{N_3}{N_1}i_{LB} = -\frac{N_3}{N_1}i_3. \qquad (3)$$

Thus

$$i_m = i_{CB} - i_1 = i_{CB} + \frac{N_3}{N_1}i_3. \qquad (4)$$

Therefore, it can be seen that the magnetizing current im is supplied by the discharging current from the dc bus capacitor CB and the current i3 which is equal to input current iLB at this stage. The current through the main switch (SW) is given by

$$i_{\text{SW}} = i_{CB} = i_m - \frac{N_3}{N_1}i_3 = i_m + \frac{N_3}{N_1}i_{LB}. \qquad (5)$$

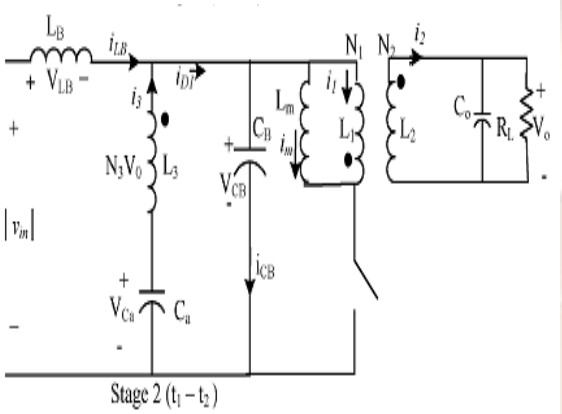
Therefore, the current stress of the switch can be reduced by selecting the turns ratio (N3 /N1), which is designed to be less than 1 to ensure proper operation of the transformer. Compared to the single-stage BIFRED converter [11], the switch current is given by

$$i_{SW} = i_m + i_{LB}. \quad (6)$$

Obviously, the proposed circuit has less switch current stress therefore, the conduction loss and switching losses are reduced and the efficiency is improved correspondingly.

2) Stage 2 (t1 − t2): When the switch is turned OFF at t=t1, output diode Do begins to be forward biased. Therefore, the energy stored in the transformer magnetizing inductor is delivered to the load through the secondary . Similarly, the diode D1 is also forward biased and the voltage across LB now Vin−VCB . Therefore, the current ILB is linearly decreased to zero at t = t2 (DCM operation), and the energy stored in LB is delivered to the dc bus capacitor CB.

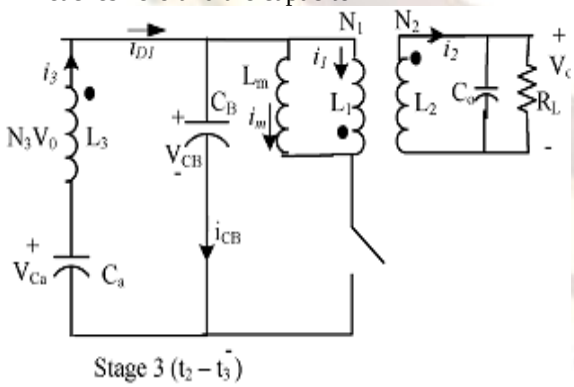
$$i_{LB} = \frac{|V_{in}| - V_{CB}}{L_B}(t_1 - t_2). \quad (7)$$



The capacitor (Ca) is also discharging its energy to the dc bus capacitor CB and the current i3 reverse its direction. Therefore, the capacitor current is given by

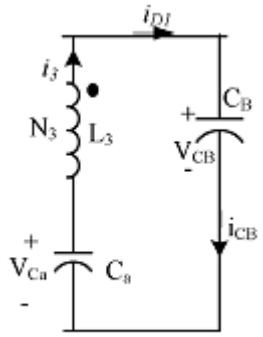
$$i_{D_1} = i_{CB} = i_{LB} + i_3. \quad (8)$$

3) Stage 3 (t2 − t3): At this stage, the input inductor current iLB reaches zero and the capacitor



Ca continues to discharge its energy to the dc bus capacitor CB . Therefore, iD1 = iCB = i3 . At t= t3, the magnetizing inductor releases all its energy to the load and the currents im and i2 reach to zero level because a DCM operation is assumed.

4) Stage 4 (t3 − t4): This stage starts when the currents im and i2 reach to zero. Diode D1 still forward biased, therefore, the capacitor Ca still releasing its energy to the dc bus capacitor CB .



This stage ends when the capacitor Ca is completely discharged and current i3 reaches zero. At t = t5 , the switch is turned on again to repeat the switching cycle.

B. Steady-State Analysis

The voltage conversion ratio of the proposed converter can be estimated from the volt-second balance on the inductors and the input–output power balance as explained in the following.

$$\left(V_{in} + \frac{N_3}{N_1}V_{CB} - V_{Ca}\right) dT_S = (V_{CB} - V_{in})\, d_1 T_S \quad (9)$$

where d1 is the OFF-time of the switch (SW). Therefore, d1 could be given by

$$d_1 = \frac{V_{in} + (N_3/N_1)\, V_{CB} - V_{Ca}}{V_{CB} - V_{in}} d. \quad (10)$$

From Fig. 3(a), the average current of the boost inductor in a switching cycle is given by

$$I_{in} = I_{LB,av} = \frac{i_{LB,peak}}{2}(d + d_1)\, T_S. \quad (11)$$

Substituting for iLB, peak given (12) and using(10),the average input current is given by

$$I_{in} = \frac{V_{in} + (N_3/N_1)\, V_{CB} - V_{Ca}}{2L_B} d^2 T_S \times \left(\frac{(1 + N_3/N_1)\, V_{CB} - V_{Ca}}{V_{CB} - V_{in}}\right). \quad (12)$$

Based on (12) for a given input voltage, Fig. 4(a) shows the normalized input current waveform in a half cycle for a change in the turns ratio N3 /N1 . It can be seen that to reduce the dead time and improve the power factor of the input current the turns ratio must be ≥0.5. Similarly, Fig. 4(b) shows the normalized input current waveform for a change in dc bus capacitor voltage VCB.The energy absorbed by the circuit from the source during a half switching cycle is given by

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} V_m \sin(t) I_{in}\, dt.$$

Substitution for Iin in given (12) yields

$$P_{in} = \frac{1}{\pi}\frac{V_m}{2L_B} d^2 T_S(A) \int_0^{\pi} \sin(t) B dt \quad (13)$$

Where

$$A = \left[\left(1 + \frac{N_3}{N_1}\right) V_{CB} - V_{Ca}\right],$$

$$B = \frac{V_m \sin(t) + (N_3/N_1)\, V_{CB} - V_{Ca}}{V_{CB} - V_m \sin(t)}.$$

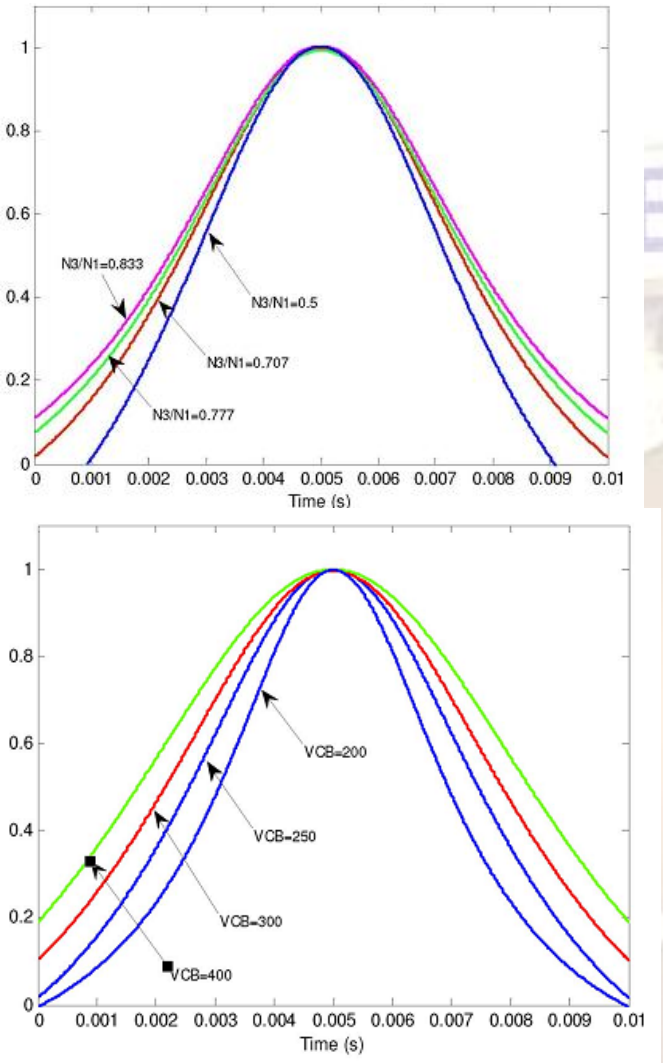


Fig. 4.Normalized input current waveform in half cycle for a change in (a)turns ratio N3 /N1 and (b) bus capacitor voltage VCB.

The average output power for a DCM fly back converter is given by

$$P_o = \frac{V_{CB}^2}{2L_m} d^2 T_S. \qquad (14)$$

Assume 100% efficiency, Pin = Po , yields

$$V_{CB}^2 = \frac{V_m}{\pi}\frac{L_m}{L_B}(A)\int_0^{\pi} \sin(t)\, B dt. \qquad (15)$$

Equation (15) shows that the dc bus capacitor is independent of load variation.

TABLE I
COMPARISON BETWEEN THE CONVENTIONAL BOOST + FLYBACK AND THE PROPOSED PFC CIRCUIT

	Boost+flyback (DCM+DCM)	Proposed converter(DCM+DCM)
Semiconductors	3 diodes, 1 switch, 1 bridge rectifier	2 diodes, 1 switch, 1 bridge rectifier
Passive components	1 inductor, 2 capacitors, 2-winding Transformer	1 inductor, 3 capacitors, 3-winding Transformer
Switch current	$I_{LB}+I_{Lm}$	$(N_3/N_1)I_{LB}+I_{Lm}$, where $N_3/N_1<1$
Efficiency (at full load)	70%	>90%
Capacitor voltage V_{CB} (for constant input voltage)	Controlled by the ratio L_m/L_B	Controlled by the ratio L_m/L_B and winding ratio N_3/N_1
THD of the input current	>20%	<10%

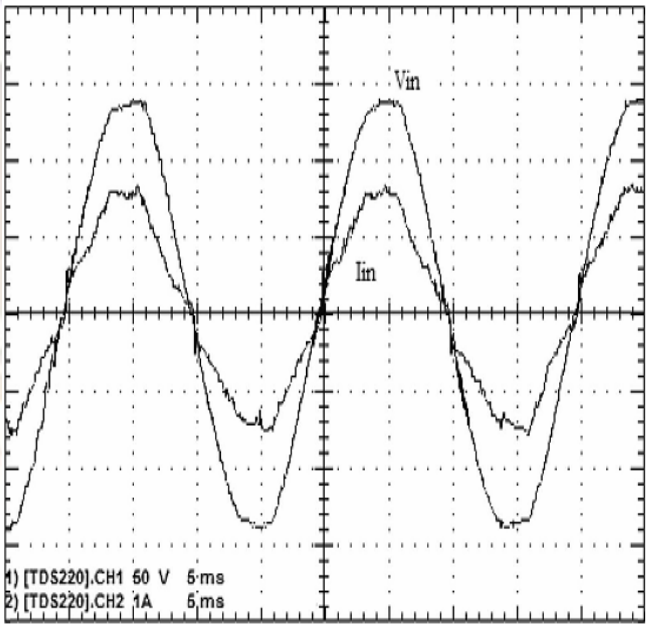


Fig. 5. Measured input voltage and filtered input current at full load (THD = 8.2%).

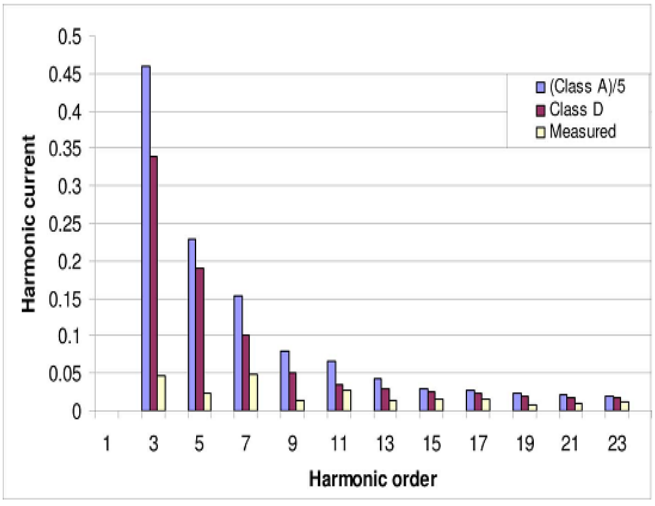


Fig. 6. Measured harmonics content of the input current.

IV. CONCLUSION

In this, a new ac/dc converter based on a quasi-active PFC scheme has been presented. The proposed method produces a

current with low harmonic content to meet the standard specifications as well as high efficiency. The input inductor can operates in DCM to achieve lower THD and high power factor. By properly designing the converter components, a tradeoff between efficiency and harmonic content can be established. Operating principles, analysis, and simulation results of the proposed method are presented.

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