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Design Of A Modified Ultra Low Power, High Precision CMOS Opamp based Comparator for Biomedical Applications

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ABSTRACT

In this paper we have represented an improved design of Two stage Opamp based Cmos Comparator having ultra low power consumption which is beneficial in many low power applications such as many biomedical applications. The proposed design is a modified design of two stage open loop comparator . We have designed a cascode version of An opamp based design. The Analysis and simulated results which have been obtained using .35µm CMOS TSMC parameters On Tanner V7 EDA tool with a power supply voltage of 3.3V with input voltage of 1V and Input Common Mode Range (ICMR)of 0.4-3V shows that comparator exhibits a high resolution of 13bit and an ultra low power consumption of 53uw at signal frequency of 100Khz having reference voltage of 0.4V. This proposed comparator also provides Gain of 80 db and Unity gain bandwidth of 10Mhz at which Phase Margin of 49 degree calculated . All these observations are made under 27 degree default temperature.

***Keywords*- OP-Amp, CMOS Logic, Power Consumption, Supply Voltage, Reference, Biomedical**

I. INTRODUCTION

Analog-to-Digital Converters are predominantly used in modern day devices to act as an interface between the real world and digital systems of these devices. The comparator, which is one of the integral building blocks of an Analog-to-Digital Converter, consumes lot of power The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic0.

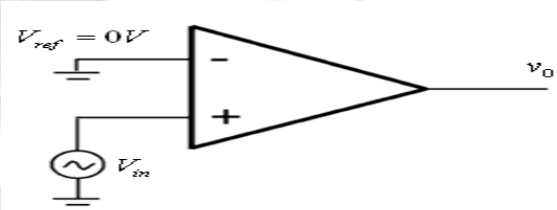


Fig 1: Schematic symbol of comparator[1]

The Organization of this paper is as follows. In section II we briefly describes the main power consideration in cmos circuits. Following this In section III various comparator architectures defined .In section IV our research work is defined. In section V design procedure is mentioned. In section VI and VII simulation results and conclusion are defined respectively.

II.POWER CONSIDERATION IN CMOS

Power is one of the vital resources. Hence, the designers try to save it when designing a system. Power dissipation is dependent on the switching activity, node capacitances (made up of gate, diffusion, and wire capacitances), and control circuit size. There are four source of power dissipation: dynamic switching power due to the charging and discharging of circuit capacitance, leakage current power from reverse biased diodes and sub-threshold conduction, short-circuit current power due to finite signal rise/fall times, and static biasing power found in some logic styles (i.e. pseudo-nMOS).

$$P_T = P_{D+} P_L + P_{SC} + Ps \quad [1]$$

Dynamic switching power is the major component of overall power dissipation, the low-power design methodology concentrates on minimizing total capacitance, supply voltage, and frequency of transistor.

$$P_{D=}CV^2F \quad [2]$$

For Analog circuits design power consumption is mainly depends upon the Signal to noise ratio(S/N) and frequency of operation also[14].

$$P=SNR\ 8Kt\ Vp\text{-}p/Vb \qquad [3]$$

For most CMOS circuit design, the short circuit power dissipation is approximately 5-10% of the total dynamic power. The sub-threshold current is proportional to the transistor device size (W/L) and an exponential function of the supply voltage. Thus, the current may be minimized by reducing the transistor sizes, and by reducing the supply voltage. Scaling in the supply voltage appears to be the most well-known means to reduce power consumption. However, the lower-supply voltage increases circuit delay and degrades the drivability of cells designed with certain logic style. One of the important obstacles in decreasing the supply voltage is the large transistor count and Vth loss problem. By selecting proper (W/L) ratio we can minimize the power dissipation without decreasing the supply voltage.In this paper we have achieved the W/l ratio to achieve lowest average power consumption in .35µm CMOS technology.

III.COMPARTORS ARCHITECTURE

Comparator is the basic unit for an analog to digital converters. There are different architectures of comparator employed to solve different purpose. They vary according to their characteristics like in two stage op-amp as comparator, no need for compensation capacitor as we are not concerned with stability, in preamplifier based comparator offset voltage is reduced at the loss of speed, in case of dynamic comparator the prime concern is speed and power. Thus all architecture has their specific characteristics. Different architectures of comparator are discussed in following section which is as follows:

- Two stage open loop comparator [1]
- Comparator with regenerative positive feedback [1]
- Fully differential comparator [1]
- Dynamic comparator[1]

IV OUR.RESEARCH WORK

At first a two stage open-loop comparator was designed to meet the desired specifications. However, due to speed and power limitations in two stage open loop architecture, we had to modified the two stage open loop comparator design which should be supportive to ultra low power operation and higher resolution. Therefore, an ultra-low power comparator was designed which is not only supportive to ultra-low power operation but also has higher resolution. So we have first designed the schematic of two stage opamp based open loop comparator on TANNER V7 EDA TOOL .After that we simulated the design and analysed the result which is not close to our desired ultra low power result.Then we try to modified this design by using combination of differential and current mirroe cascode circuit to achieve our desired result .We simulated the modified cascode circuit on TSMC .35um cmos Technology file and analysed the resutls which found to be better than previous ones.

Here below we have shown the schematic diagramme of proposed comparator .

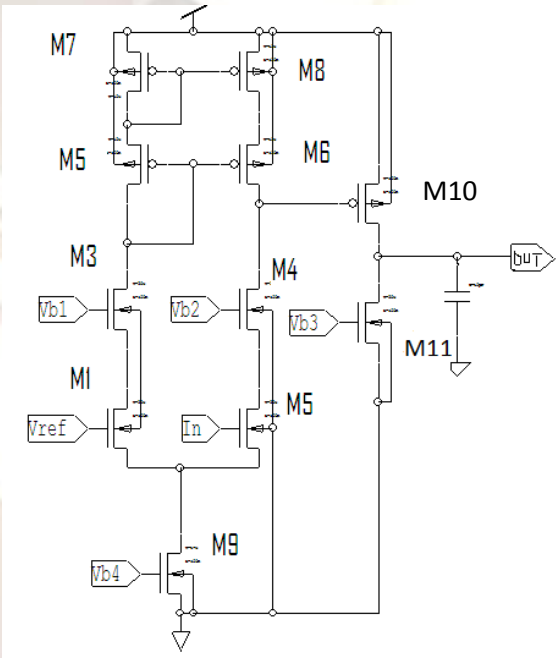


Fig2:Proposed Schematic Design

In this architecture (Fig.1) there are two stages first stage is composite cascode differential amplifier Nchannel input devices (M1-M4) in series with combination of cascode active Pmos based current mirror load such as (M5-M8) that compares the two input but provide smaller gain while the second stage is common source provide larger swing and greater gain similar to opamp based conventional two stage open loop comparator and one nchannel Mos is provided below which act as current sink for stabilization. . Amplifiers are usually employed to achieve linear operation in closed loop configuration which requires careful compensation to avoid unstable operation. On the contrary the comparator does not require stability criteria as in two stage amplifier so it eliminated need for compensation capacitor.

V. DESIGN EQUATIONS

The design of two-stage open-loop comparator is similar in many respects to the designing of two stage op-amp. The primary difference is that the comparator is not compensated. The typical desired specifications of comparator of Fig. 3.1 are shown in Table 3.1. The procedure is illustrated below:

Step1: Determine the value of gm1 by using given unity gain bandwidth.

$$Gm1= 2\pi *UGB *C \quad [4]$$

Step2: Calculate W/L of input transistors (M1, M2) by keeping length of each transistor constant.

$$(W/L)1=(W/L)2=Gm_1^2/2K_NI_9 \text{ where as } (I_9= V_{OH}-V_{OL}/t_p) \quad [5]$$

After finding this ratio we can also use the same ratio for W/L_3 AND W/L_4

Step4: Calculate the aspect ratio of transistor M5 and M6 which is current mirror. We can calculate it with the help of aspect ratio of input transistor.

$$W/L_5=W/L_{6=} I_9/ kp(V_{DD}-V_{INMAX}-V_{T\,o\,+}V_{T1})^2 \quad [6]$$

Step5: The last step is used to calculate the aspect ratio of transistor M10 &M11.

$$W/L_{10}=I_9*Gm_{10}/ \quad [7]$$

$$W/L_{11=}I_{10}/I_9*(W/L)_9 \quad [8]$$

Transistor	W	Transistor	W
M1	20µm	M7	10µm
M2	20µm	M8	10µm
M3	20µm	M9	20µm
M4	10µm	M10	17µm
M5	10µm	M11	0.4µm
M6	10µm		

For All Transistor L=.40µm

Table I:Aspect Ratio of Proposed Comparator

VI. SIMULATION RESULTS

The simulation of proposed architecture has been done to analyze the circuit performance for various parameters. In this section we have described and analyzed the simulation results of our proposed architecture of Ultra low power comparator . This designs is simulated on TANNER V7 EDA Tool with 0.35µm cmos process technology This design operates on 3.3 V power supply and consume only 36µw power. Simulated result on considerable increase of unity-gain bandwidth of 10Mhz an improved ac gain of 80.34 db and phase margin of 49 degree.

Fig 3 represent the simulated transient curve of proposed comparator. An inverting terminal is connected to reference voltage and non-inverting terminal is connected to varying sinusoidal input of 1v with 20 KHz of input frequency it shows comparison of an ac input voltage of 1v with dc reference .4v.it shows charge and discharge when ac sinusoidal input rise and fall at 0.4v

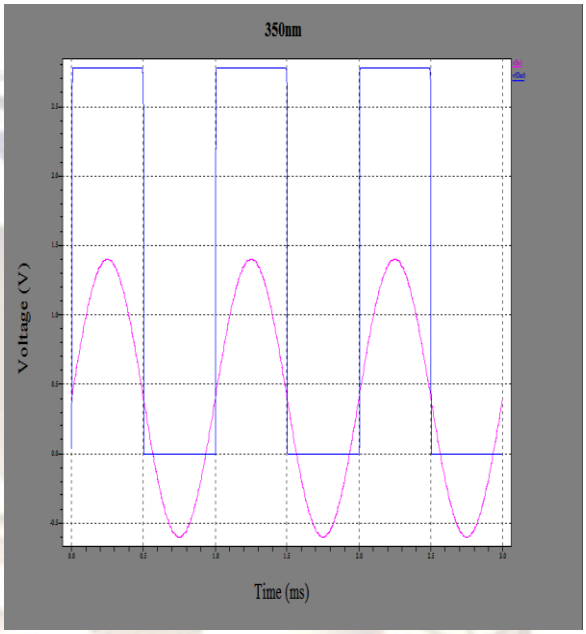


Fig 3: Transient waveform of proposed comparator

Fig 4 shows an improved ac small signal gain . fig 5 shows the phase margin of 49 degree at 10Mhz UGB. .figure 6 shows the dc transfer curve of proposed ultra low power comparator .It presents the input common mode range of proposed comparator.

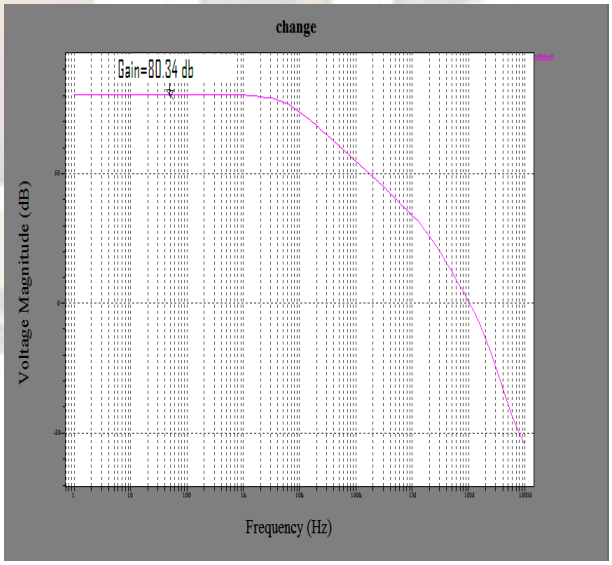


Fig 4:Simulated Ac gain

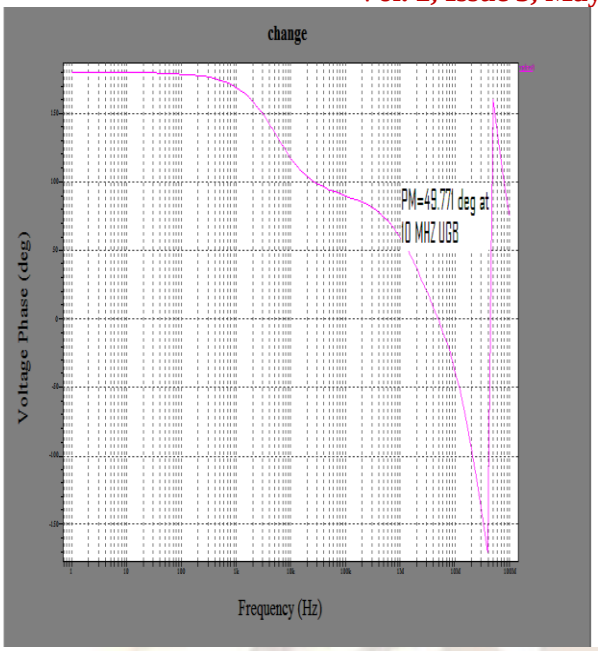


Fig 5: Simulated Phase Margin

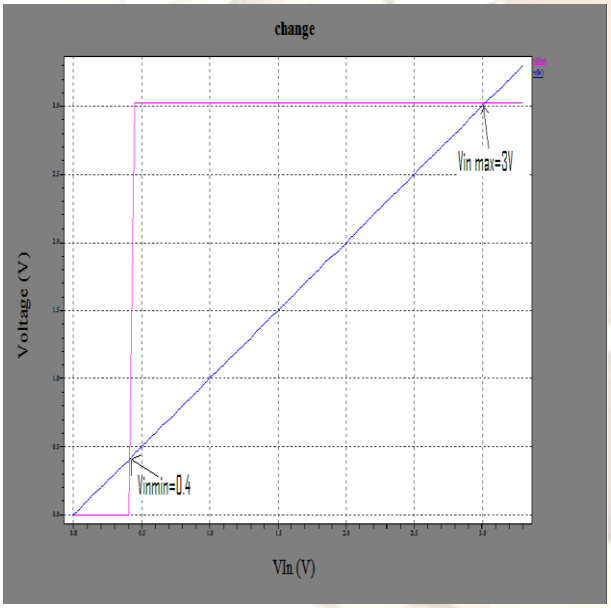


Fig 6: Dc transfer curve

After simulating the schematics we have achieved the average power consumption values .Then We have analyzed the result of Average power consumption on Following basis

First at different input frequencies for both conventional and proposed design at fixed power supply source represented in table given below at three reference points.

frequency(Hz)	Pow(µW)	Pow(µW)
1k	41.4	243
5k	42	244
10k	42.4	245
20k	43	246
50k	46	248
100k	53.9	255
500k	81.9	270
1000k	82	272

TableII.:Average power consumption(Pow) of Conventional & Proposed design at input frequency range from 1-1000khz

Secondly at different supply voltages for both conventional and proposed design at fixed frequency of 100KHZ.

Vdd	Pow(proposed)	Pow(conventional)
1.8v	14 µW	98 µW
2.1v	19 µW	120 µW
2.4v	25 µW	146 µW
2.7v	32 µW	174 µW
3v	41 µW	208 µW
3.3v	53.9 µW	255 µW

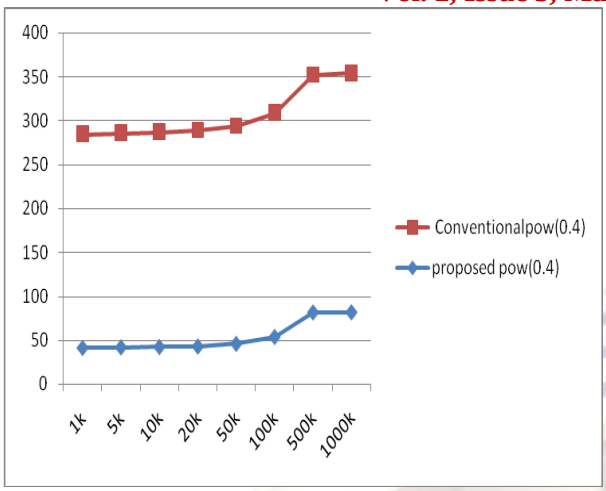
TableIII:Average power consumption(Pow) of Conventional & Proposed design at power supply of ranges 3.3-1.8V at some fixed frequency point

A.Graphical Analysis

After making result tables of both the design we want to do the graphical analysis .

Graph 1

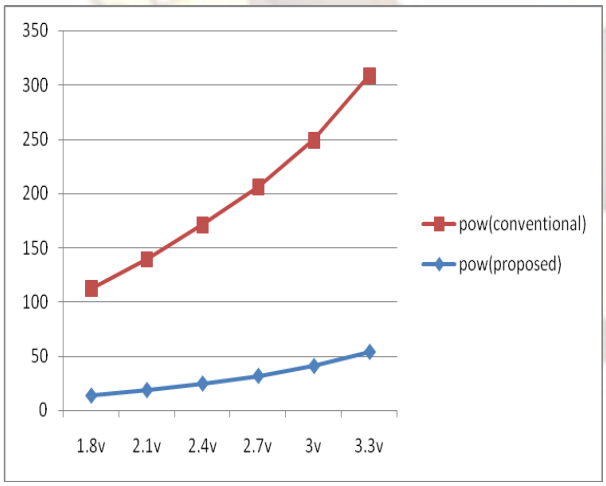
We have plotted this graph for comparing the values of average power consumption(pow) wrt frequencies(1k-1000khz) at same reference point for both conventional and proposed design. It shows we obtained an average power consumption values in ultra range which is quite lower than the conventional design values.



Graph 1: shows variation of the Pow wrt frequency at same reference points at fixed power supply voltage for conventional and modified design

Graph 2

We have plotted this graph by taking results from table III.it represent the variation in average power consumption at various power supply voltage ranges 3.3-1.8v with .3v separation at fixed frequency.It shows how with increase in voltage power consumption increase for both the conventional and modified design so it proves the direct relationship of voltage and power.But it also compare the values of average power consumption of both the design and aanalyzed that we achieved a very low amount of average power consumption (POW) in our proposed design than conventional.



Graph 2: shows variation of the Pow wrt vdd at same reference points at fixed frequency for conventional and modified design

Performance summary	**proposed**	**conventional**
Gain (DB)	80	41
UGB(MHZ)	10	20
PM(degree)	49	75
Power supply(V)	3.3	3.3
Power dissipation(µW)	41.4	241
Resolution(BITS)	13	6
ICMR(V)	0.4-3	0.4-3.3
Output Impedence(MΩ)	18	.007

Table IV:Performance specification comparison of proposed and conventional comparator

Performance summary	This work	[11]	[12]	[9]	[2]	[3]
Power consumption(µW)	41.4	2000	130	100	600	1000
Power supply(v)	3.3	3.3	1.8	1	3.3	3.3
Cmos technology(µm)	.35	.35	.35	.35	.35	.35
Input voltage(v)	1	1	----	0.7	1.6	1.6

Table V:Performance specification comparison of proposed and other type of comparators

Temp(degree)	**-20**	**0**	**27**	**100**
GAIN(DB)	55	67	80	12
UGB(MΩ)	1	3.2	10	.036
PM(degree0	115	97	49	189

Table V1:Comparison performance of comparator at different temperatures

VII.Conclusion

In this paper we have presented a Modified proposed design of conventional opamp based two stage open loop comparator design. By studying prior publications we are able to design a new type of ultra low power proposed cascode design from conventional one on TANNER V7 EDA at .35um TSMC cmos technology. The proposed ultra low power comparator is found to consuming 41.4-82 µW power at 3.3V supply voltage having input frequency of ranges 1-1000 KHz .The comparator is having very high resolution of 13-bit and high gain of 80db.. Therefore it could be very useful in portable and wireless biomedical sensors for ECG,

EEG, and blood pressure and in implanted medical devices where ultra energy-efficient operation and high resolution should be critical.

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