

Adiabatic Logic Gate for Low Power Application

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ABSTRACT

In this paper, the design of circuits using adiabatic logic and sequential circuits based on the newly proposed Energy efficient adiabatic Logic (EEAL) is presented. EEAL uses dual sinusoidal source as supply-clock. This paper proposes a positive feedback adiabatic logic (PFAL), two-phase clocked adiabatic static CMOS NOR logic (2PASCL) circuit that utilizes the principles of adiabatic switching and energy recovery compare than CMOS NOR. 2PASCL has switching activity that is lower than dynamic logic. The power consumption of 2PASCL becomes lower compare than CMOS NOR. Also design layout of the CMOS Inverter, NAND, NOR and 2PASCL logic circuit. Comparison has shown a significant power saving to the extent of 70% in case of proposed technique as compared to CMOS NOR logic gate in 10 to 200MHz transition frequency range. The simulation results are analyzed at 180nm and 90nm technology to show the technology independence of the design. The proposed design of CMOS NOR logic gate is better suitable for the low power VLSI applications.

Keywords- Adiabatic logic, adiabatic switching, Energy recovery, Low Power applications, Power Supply, Spice, two phase clocked.

1. INTRODUCTION

The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field. Nonetheless, the level of on-chip integration and clock frequency will continue to grow with increasing performance demands, and the power and energy dissipation of high-performance systems will be a critical design constraint [4].

Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power [5].

The idea behind the circuit is built upon the basic diode based circuit proposed in [12] and [1]. In this paper, we propose a two-phase clocked adiabatic static CMOS logic (2PASCL) [3]

circuit to achieve low power consumption; we also compare its power consumption with that of a conventional CMOS circuit. A novel method for reducing the power dissipation in a 2PASCL circuit involves the design of a charging path without diodes. In such a case, current flows only through the transistor during the charging. Thus, a 2PASCL circuit is different from other diode-based adiabatic circuits in which current flows through both the diode and transistor [9]. By using the aforementioned 2PASCL circuit, we can achieve high output amplitudes and reduce power dissipation. In addition, in order to minimize the dynamic power consumption in this circuit, we apply a split-level sinusoidal driving voltage.

Several adiabatic logic families based on energy recovery principle [8] where all charge recovered back to power supply without heat generation have been proposed & implemented earlier. The following mathematical analysis based on time period (T), Stored Charge ($C_L V_{dd}$), Load capacitance C_L and channel resistance R is sufficient to have a deeper look on it.

$$E_{diss} = (RC_L/T)C_L V_{dd}^2 \quad (1)$$

Theoretically, it is possible to reduce the power dissipation by extending the switching time.

The circuit uses a two phase clocked split-level sinusoidal power supply to reduce the voltage difference between the current-carrying electrodes to reduce the power consumption.

2. ADIABATIC SWITCHING

Adiabatic switching is commonly used to minimize energy loss during the charge/discharge cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation [7]. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time varying voltage source instead of a fixed voltage supply. Here, the load capacitance (C_L) is charged by a constant current source (I). In conventional CMOS logic we use constant voltage source to charge the load capacitance [1]. Here, R is the on-resistance of PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume the capacitor voltage zero initially.

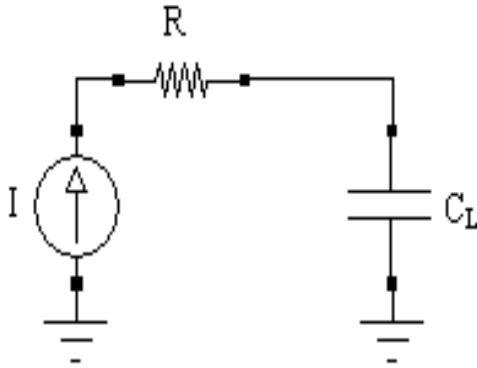


Fig1: Adiabatic logic circuit

The voltage across the switch = IR

$P(t)$ in the switch = I^2R

Energy during charge $E = (I^2R)T$

Also $Q = C_L V_{dd}$, $I = C_L V_{dd} / T$

$E = (I^2R)T = (RC_L/T)C_L V_{dd}^2$

Where, E [3] is the energy dissipated during charging time,

Q is the charge transferred to the load,

C is the value of the load capacitance,

R is the on-resistance of the PMOS switch,

V is the final value of the voltage at the load,

T is the charging time.

Theoretically, when driving voltage (V_a) switching time (T) from 0 V to V_{dd} is long, the energy dissipation is nearly zero.

When V_a changes from HIGH to LOW in the pull-down network, discharging via the NMOS transistor occurs. From equation (1), it is observed that when energy dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the load capacitor during the current subsequent computational steps. Systems based on above-mentioned technique for charge recovery is not necessarily reversible [2], [10].

3. CMOS NOR

The design and analysis of CMOS combinational logic circuits can be based on the basic principles developed for the NMOS depletion-load logic circuits. Fig2 shows the circuit diagram of a two input CMOS NOR gate. The circuit consists of a parallel-connected n-net and a series connected complementary p-net. The input voltages a and b are applied to the gates of NMOS and PMOS transistor.

The complementary nature of the operation can be summarized as follows:

When either one or both inputs are high, i.e., when the n-net creates a conducting path between the output node and the ground, the p-net is cut-off [12]. On the other hand, if both input voltages are low, i.e., the n-net is cut-off, then the p-net creates a conducting path between the output node and power supply voltage V_{DD} . Thus the dual or complementary circuit structure allows that, for any given input combination, the output is connected either to V_{DD} or to ground via a low-resistance path.

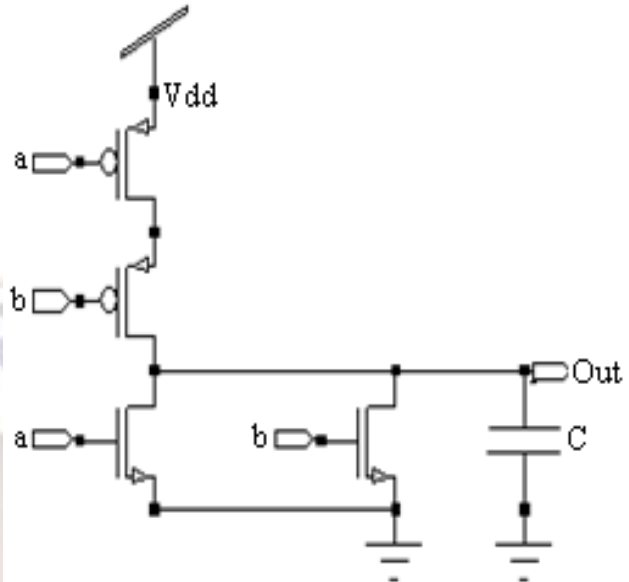


Fig2: Two input NOR gate

4. 2PASCL

Figure 3 shows a circuit diagram of Two-Phase Adiabatic Static Clocked Logic (2PASCL) inverter. A double diode circuit is used, where one diode is placed between the output node and power lock, and another diode is adjacent to the NMOS logic circuit and connected to the other power source [3]. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous if the signal nodes are preceded by a long chain of switches.

The circuit operation is divided into two phases: evaluation and hold. In the evaluation phase, V_a swing up and V_{aB} swings down. On the other hand, in the hold phase, V_{aB} swings up and V_a swings down. Let us consider the inverter's logical circuit demonstrated in Figure 3. The operation of the 2PASCL inverter is explained as follows.

1) Evaluation phase:

- When the output node Y is LOW and the PMOS tree is turned ON, C_L is charged through the PMOS transistor, and hence, the output is in the HIGH state.
- When node Y is LOW and NMOS is ON, no transition occurs.
- When the output node is HIGH and the PMOS is ON, no transition occurs.
- When node Y is HIGH and the NMOS is ON, discharging via NMOS and D_2 causes the logic state of the output to be "0" [6].

2) Hold phase:

- When node Y is LOW and the NMOS is ON, no transition occurs.
- At the point when the preliminary state of the output node is HIGH and the PMOS is ON, discharging via D_1 occurs.

Fig5 Power Consumption comparison of proposed NOR vs NOR at Power supply in 180nm technology

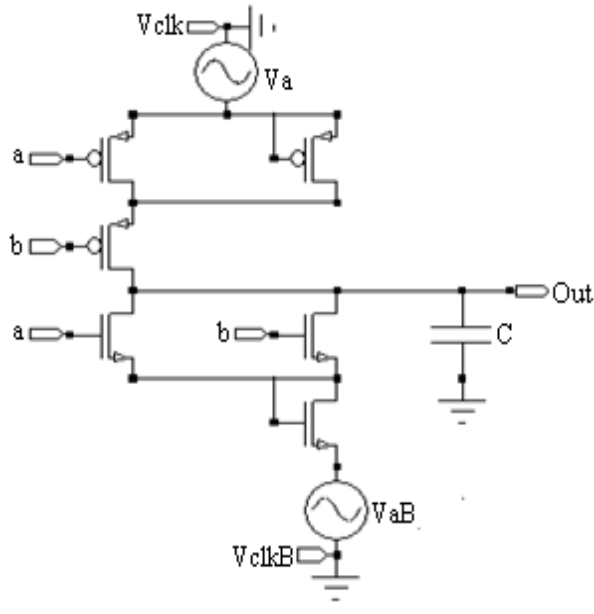


Fig3: 2PASCL NOR gate

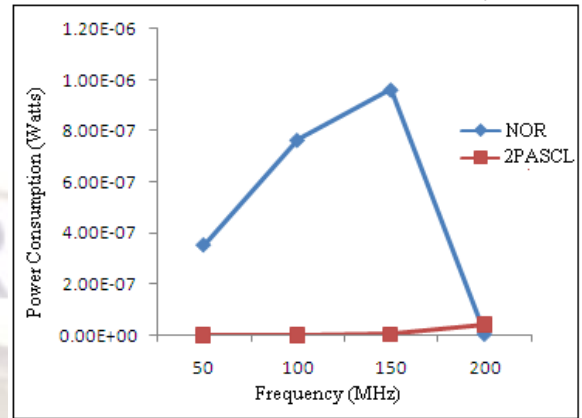


Fig6 Power Consumption comparison of proposed NOR vs NOR at frequency in 180nm technology

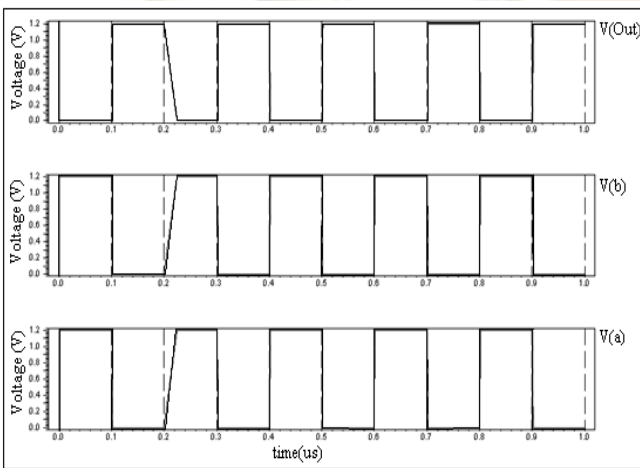


Fig4: Input and Output waveforms for CMOS NOR gate

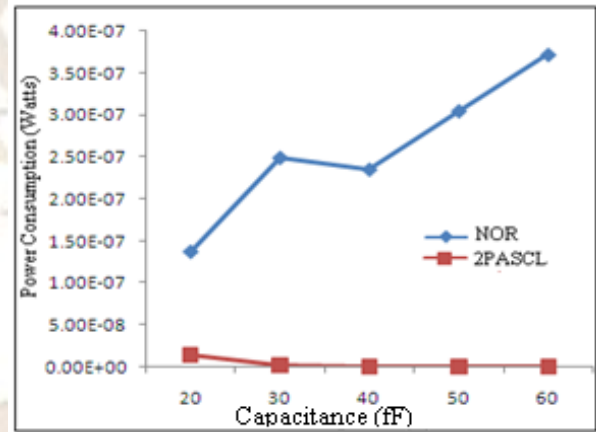


Fig7 Power Consumption comparison of proposed NOR vs NOR at capacitance in 180nm technology

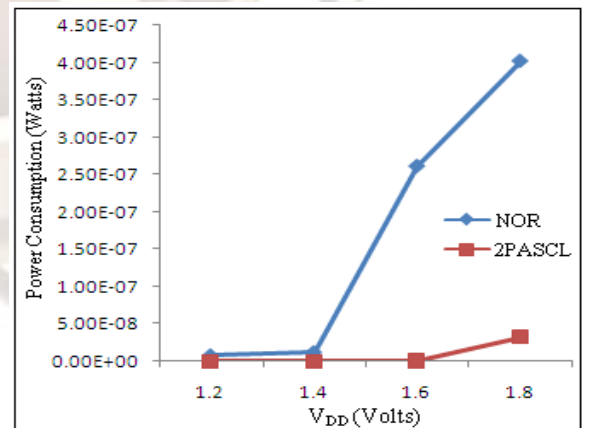
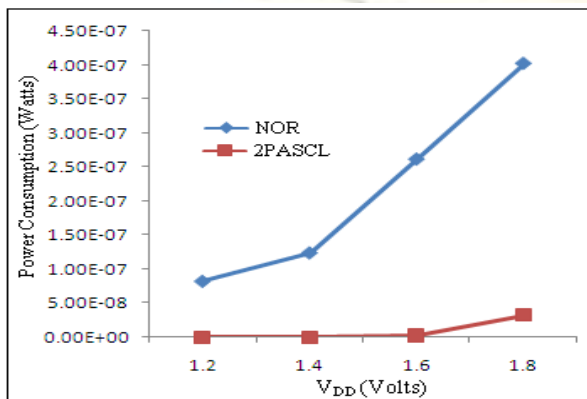


Fig8 Power Consumption comparison of proposed NOR vs NOR at Power supply in 90nm technology

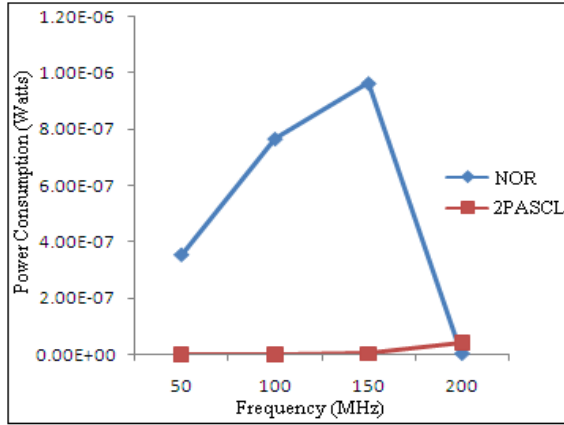


Fig 9 Power Consumption comparison of proposed NOR vs NOR at frequency in 90nm technology

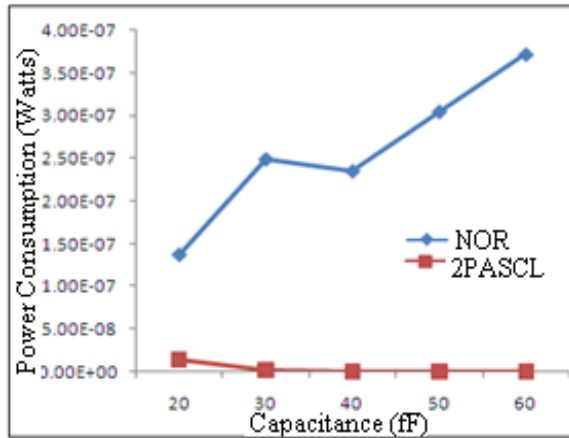


Fig10 Power Consumption comparison of proposed NOR vs NOR at capacitance in 90nm technology

The simulation is performed using a SPICE circuit simulator at 180nm and 90nm technology node & 1.8 V standard CMOS process. The Proposed circuit width W & L of the NMOS and PMOS logic gates were 600n and 180n respectively. Whereas the length and width of MOS diode D2 is 40 μm beside a load capacitance C_L of 0.05pF connected at the output node. Above figure shows the simulated waveforms of Proposed CMOS NOR and 2PASCL NOR logic gate.

5. PHYSICAL LAYOUT

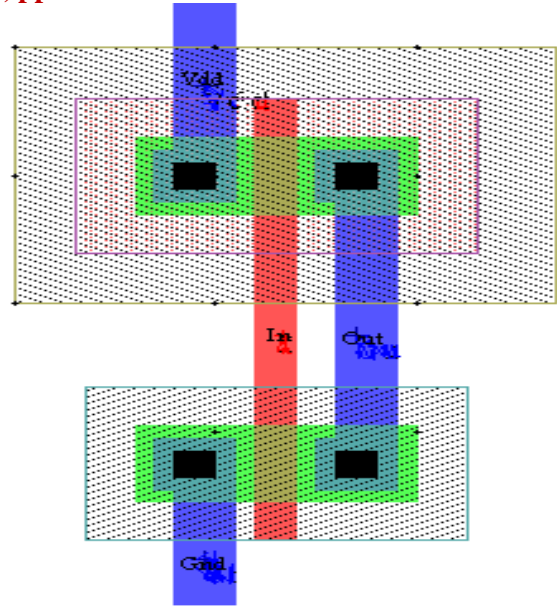


Fig11: layout of CMOS inverter

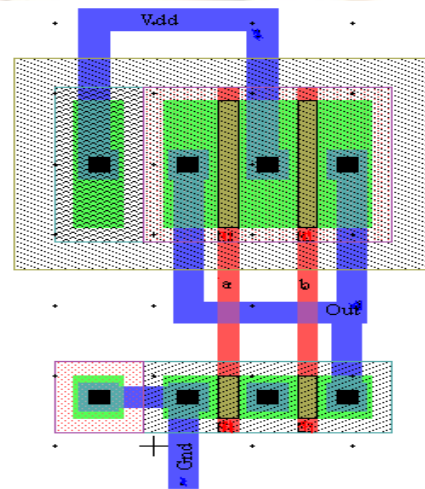


Fig12: layout of NAND gate

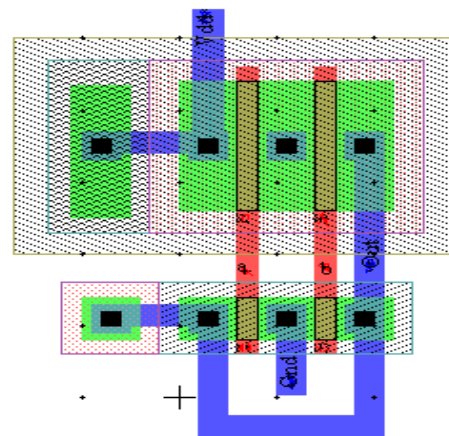


Fig13: layout of NOR gate

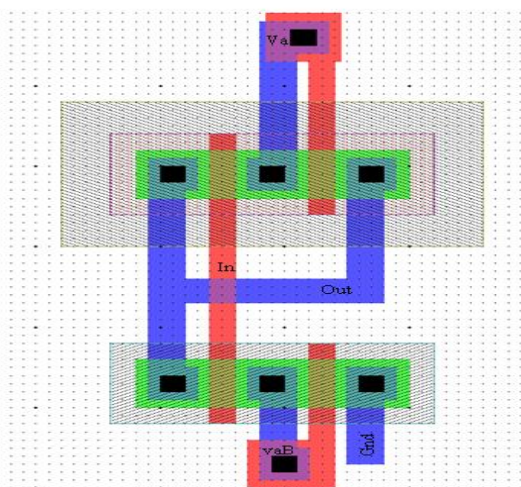


Fig14: layout of 2PASCL CMOS

6. CONCLUSION

Simulation results obtained from the CMOS NOR and 2PASCL NOR gate has wide acceptance in low power VLSI regime at low frequency. The comparison of the 2PASCL circuit with other traditional methodologies has proved that power consumption with the proposed logic is far less as compared to CMOS NOR based technique. The simulation result show that power consumption of 2PASCL NOR is less compare than CMOS NOR. From the results of simulation it has been observed that the replacement of diodes with switches controlled by power clock significantly reduces the power consumption of the adiabatic circuit. The simulation results are analyzed at 180nm and 90nm technology to show the technology independence of the design. Layout of CMOS, NAND, NOR and 2PASCL are shown in above fig.11-fig.14. The power consumption of Schematic is less than layout.

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