An Approach to Mitigate ^{10}B Generated Soft Error in SRAM

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ABSTRACT

The Soft Error problem from Alfa particles and terrestrial neutrons has been a big issue in Electronics industry. Measurement of Single Event Latch-up (SEL) and Soft Error (SER) are properly happened by a lot of research but efficient mitigation technique even required because of day by day shirking of the technology. Although the BPSG layer is totally removed in recent all technologies but in some technologies we can see the effect of thermal neutrons. As the miniaturization of the technology increases the multi upset phenomena also increases with it. Here we have emphasized on ^{10}B existence and place where it resides. We proposed a mitigation technique to mitigate multi cell upset Soft error by change in design (layout cell placement) and addition of two tri state inverter in 6T SRAM cell. We have also taken care of Access time, Setup time, Leakage and Power dissipation of SRAM so that these phenomena must remain optimized.

Keywords- **^{10}B, Multi cell Upset, SER, Soft Error, SRAM, Thermal Neutrons, MBU, MCU**

I. INTRODUCTION

THE Soft Error is an event in a microelectronics circuit that does not result in permanent damage or change in physical characteristics of the device. In Memory devices soft error caused by energetic particles that generate the enough free charge to upset the state of latch or memory cell.[1] The key contributors to Soft Error are: (i) High energy neutrons originating from cosmic rays in the natural environment; (ii) Alpha particles originating from trace radioactive material contamination in the IC package or wafer fabrication process; and (iii) Thermal neutrons originating from high energetic neutron after atmospheric filtration.[2]-[6]

The alpha particle (1Mev to 100Mev energy) came from radioactive decay of radioactive element like ^{238}U and ^{232}Th in plastic packaging and ^{210}Pb in flip chip contact bumps at wafer fabrication and chip packaging, which penetrate to device and collide with atom, consequently electron-hole pairs generate.

High energetic neutrons come into existence when cosmic rays strike to earth's upper atmosphere and generate a bulk of high energy atomic and sub atomic particles (energy range is 1Mev to 1 Gev). [4] The high energetic neutrons interact for nuclear fission with Si nucleus and generate secondary particles like energetic protons, neutrons, alpha particles, nuclei & residual atoms due to these particles high amount of electron-hole pairs generate. [3]

Thermal neutrons are the high energetic neutrons which lose their energy by environmental material scattering and reach equilibrium energy of around 25mev at room temperature. These low energy thermal neutrons do nuclear fission with Boron isotope ^{10}B. Although for smaller than 130nm technology BPSG is no longer in use in IC fabrication process but the ^{10}B can be present because of fabrication process. We will discuss in this paper how this ^{10}B come into existence. The nuclear fission happens with ^{10}B as:

$$n + {}^{10}B \longrightarrow {}^{7}Li\ (0.84Mev) + \alpha\ (1.47Mev) + \gamma\ (0.48Mev).$$ [3]

As SRAM cells scale down, the impact on SER in 65nm or below increase rapidly. As reduced distance between transistors makes multiple transistors vulnerable to a single particle strike, resulting multiple bit upset and multiple cell upset. [7]

In this paper we will move through discussing the fact of SRAM multi bit upset and multi cell upset with the miniaturization of the technology, then we will emphasize in this fact that the ^{10}B exist even BPSG layer is removed and we will also suggest the location of ^{10}B. After discussing that the ^{10}B still a very big problem, we will propose a mitigation technique in that we did two things. First we modify the design at that level of layout (flipped and placed horizontally SRAM) and secondly we add two tri state buffers in basic 6T SRAM cell with minimum area formed structure. At the last we put graph and values of Access time, Setup time, Leakage and Power dissipation of SRAM to show that these phenomena is remain optimized. Soft error is a major issue (especially in SRAM) in mission critical applications where reliability is a main concern on a par with performance, area and cost. Although we have done the work in the way that the area and basic phenomena do not get much change so that the industry can follow this mitigation technique.

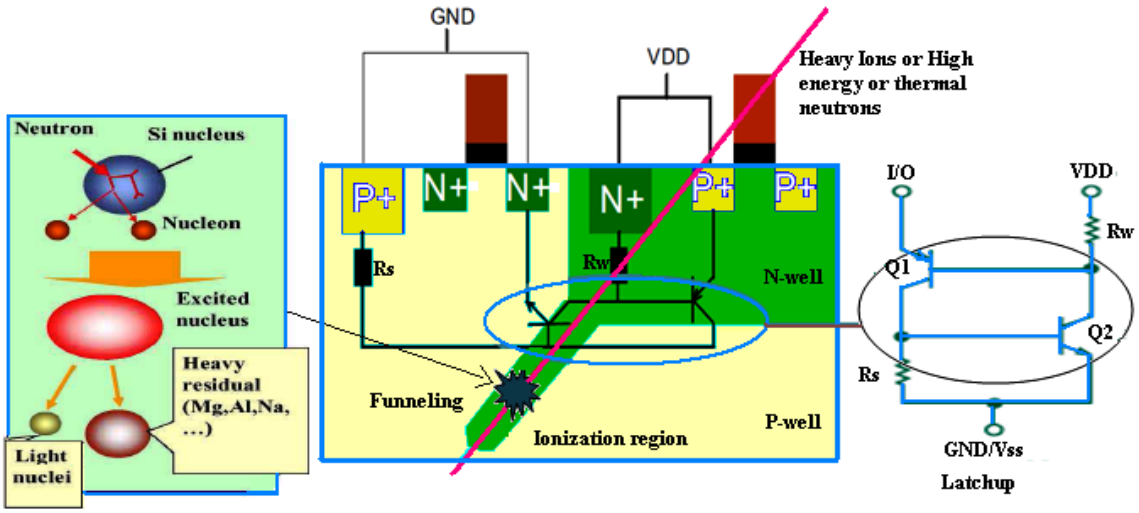


Figure 1. Single Event Latch up and Soft Error Occurring Phenomena

II. SRAM MULTI BIT UPSET WITH MINIATURIZATION OF TECHNOLOGY

The geometry of SRAM has lowest device geometry structure so design rule must be more aggressive and as the technology shrinks, the structure would be more compact. Consequently, critical charge reduces and the soft error increases rapidly. With the reference to [13] we can see that the trend is almost flat from 250nm down to 32nm (in fig. 2), it is happening because of two aspects. 1). The critical charge is scaling down so soft error will increase 2). As the cell area shrinks so decreasing the cross section for soft errors. So both effect is cancel out and graph is flat and this shows constant Soft error even with shrinking the technology. [13]

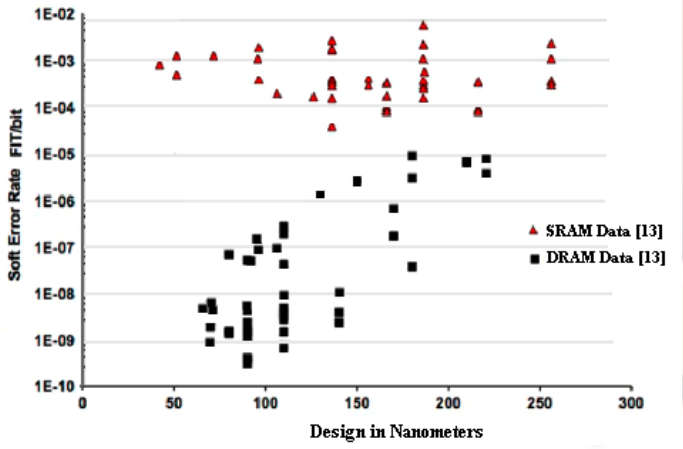


Figure 2. SRAM and DRAM soft error trend per bit with design rule

As compactness increases and critical charge drops so the probability of multiple bit upset will increase. In fig.3 we have compared multi bit upset for different technology with different aspects. We can say here that at 45nm technology, the chances of multi bit upset are more and least in 90nm. So it is following a trend to increment of multi bit upset as increment in miniaturization. Whereas for DRAM, soft error trend decreases as technology miniaturization increases (by fig. 2) so the Soft Error will not come at consideration level for DRAM.

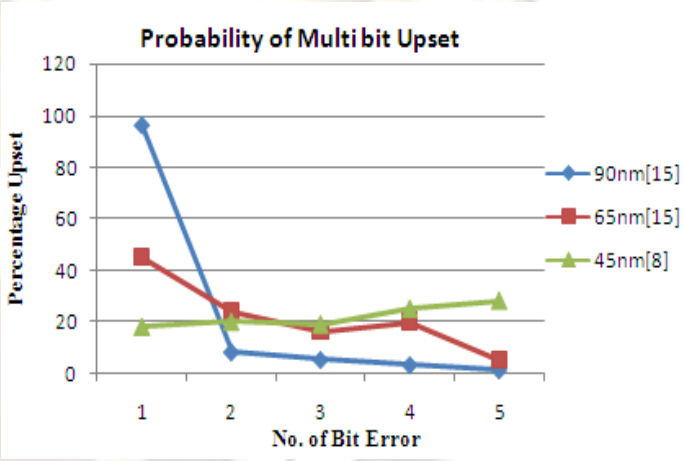


Figure 3. Single Bit and multiple bit upset Percentage

III. HOW THIS ^{10}B COME TO IN EXISTANCE

Thermal neutrons have only 25mev energy at room temperature and it performs nuclear fission with Boron isotope ^{10}B (because large cross section area 3848bars for thermal neutron capture). Although with the property of ^{10}B that the cross section for thermal neutron interaction reduced significantly at very low temperature. The neutron of any energy cannot directly ionize the atoms but it can perform nuclear reaction and consequently generate secondary elements as Alpha particles, ions and gamma particles. These particles generate the electron-hole pairs. By JEDEC JESD89A standard the soft error (the Energy x Differential Flux in cm $^{-2}$ s^{-1}) at 25mev (because of thermal neutrons) and 100MEV (high energy neutrons) are highest. [11], [12]
Earlier this ^{10}B could exist because of BPSG layer but BPSG layer has been eliminated since 130nm technology even

though we are getting the effect of thermal neutrons. This is happening because of high level of ^{10}B existence in advance Si technology chips. The ^{10}B exist in the layer right above the transistor. This could be the sensitive area of SRAM and DRAM for thermal neutron sensitivity. Although the sensitive area is not related only to this place, it can occur at different places depending on fabrication process and fabrication materials.

Actually in fabrication process maximally used B_2H_6 based material for W plug linear layer contains ^{10}B and ^{11}B. This B_2H_6 material was originally innovated in atomic layer deposition W nucleation layer enabling superior integration performance with as deposited MOCVD TiN and eliminating the need for further furnace anneal or rapid thermal anneal of the MOCVD TiN film. So by this B_2H_6, ^{10}B introduce during fabrication linear process. So we have to use purified B_2H_6. The fig. 4 shows the schematic structure W plug connection in B_2H_6 based system.

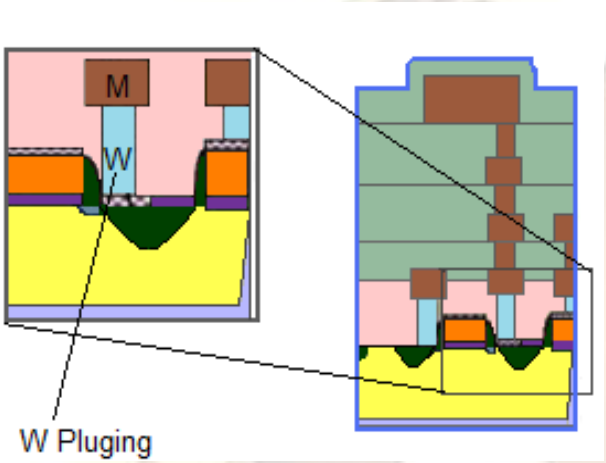


Figure 4. W Plug location in B2H6 based system

With the reference of [9] about ^{10}B finding that the two samples, first has no thermal neutron sensitivity of 90nm technology (Sample-1) and second of 55nm technology of thermal neutron sensitivity (Sample-2) has taken and analysis has done for each level for sample-1 and sample-2. The ^{11}B and ^{10}B ratio between metal layer slightly above the oxide and intermediate layer division for sample-1 is very high around 100 (in fig. 5a), whereas in Sample-2 the ratio between the metal layer slightly above the oxide and intermediate layer division adjacent layer is very less around 5 (in fig. 5b). So the ^{10}B is very high (we know naturally occurring ^{10}B to ^{11}B ratio is 4) and same as natural existence in Boron.

So overall we can say here that ^{10}B is highest near to Metal layer and Intermediate layer division junction i.e. right above the transistor and because of that 150FIT/Mbit thermal neutron soft error could occur.

This is not only the place where the ^{10}B and ^{11}B ratio is high, even in some technology it is extremely high because of fabrication process and strategies. Many research papers came till now which are giving the proof and location of this ^{10}B. In this we are bothering about all these places where this ^{10}B can occur and we can make our SRAM tolerant.

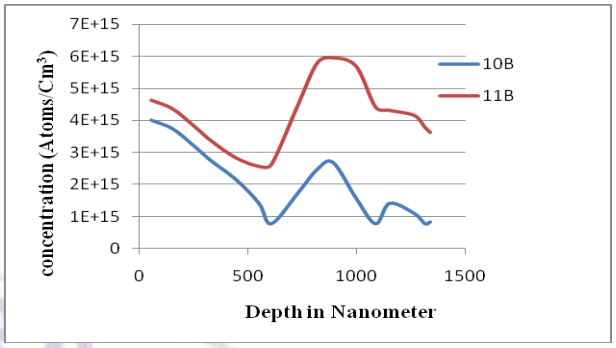


Figure 5.a. Simulation result of no thermal neutron sensitivity (Sample-1**)**

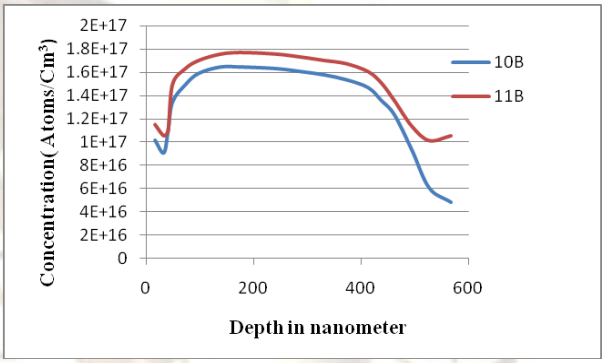


Figure 5.b. Simulation result of thermal neutron sensitivity (Sample-2)

IV. Mitigation Technique of Soft Error for SRAM

A. SRAM cell with two tri state inverter

The critical charge (minimum charge required to flip the bit stored in the cell) of memory cells significantly reduce as miniaturization increases and voltage supply downsizes in SRAM. This means low energy particles can flip memory cells, making memories sensitive to atmospheric neutrons as well as to alpha particles created from materials within the chip. [20], [21] As technology scales down, the charge stored at the sensitive nodes of the memory cell is reduced because $Q_{node} = C_{node} \times V_{dd}$ and if V_{dd} or C_{node} reduced then SRAM become more prone to soft errors. If we increase the V_{dd} to increase the critical charge it will increase the probability of Single Event Latch-up. [17]

Even if we increase C_{node} then we can increase the critical charge and for this the designers use a charge buffer (Capacitive-based SEU protection models) between the nodes Q and $\overline{Q}$ in SRAM cell (in fig.6). These capacitors keep the potential of the nodes remaining the same even if a SEU happens at one of these nodes and thus the cell state is not affected. But, the problem is large area overhead due to this extra capacitor. The major weakness of capacitor-based models is the increment in the write time to change the state of the cell and also, for low power applications they do not scale well with voltage.

We have proposed a scheme in that the low power consumption and no effect on write time. In this the basic SRAM cell consists of a regular SRAM cell with an addition two tri state inverters that are connected to WL as shown fig. 6. This design is able to provide lower power consumption due to on-demand protection structure, a tri-state device that is turned off during non-essential operating mode. The addition of the outer core tri-state inverters will strengthen the charge value of the inner core cell during the standby mode. Because of this the critical charge increases at the nodes, Q and $\overline{Q}$ and thus the tolerance level of the SRAM cell to Single Event Upset is greatly improved. The level of tolerance is dependent on the physical parameters and characteristics of the transistors in the outer core inverters. The impact of tri-state inverters on write performance is minimal due to the fact that they are turned off during writing. The turned off tri-state inverters introduce some minor input gate capacitance, which impacts the write time. Once the write mode is completed, the outer core is activated once again and the signal value in the SRAM cell is strengthened. The area penalty will not come in big deal because of structure and we can get increased protection level, operating Voltage Scale, performance and power consumption.

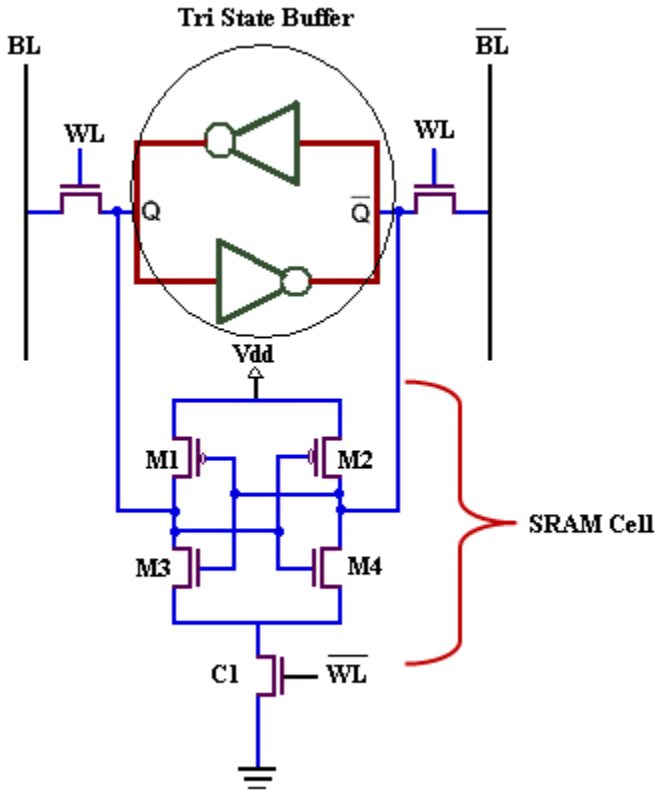


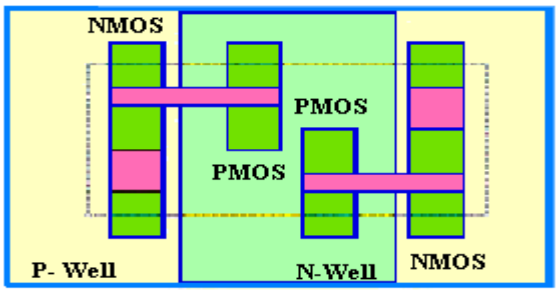
Figure 6. Basic SRAM cell with two Tri State Inverter

B. SRAM Cell Layout Placement

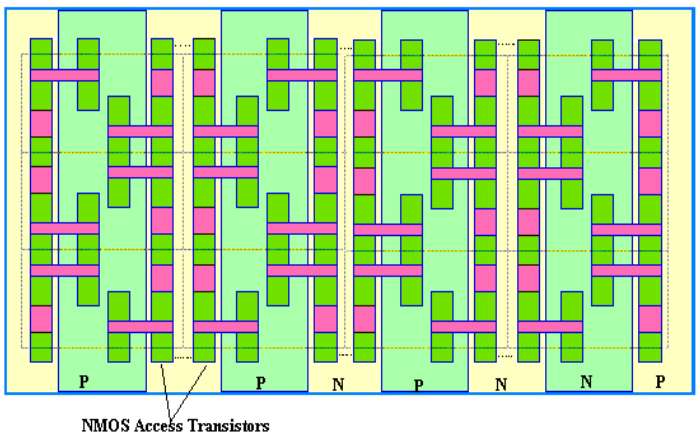
The multiple cell upset probability depends on the ion track and bipolar turn on mechanism and the NMOS parasitic bipolar turn on are the dominant mechanism for this upset. So for NMOS hardness mechanism modification is mandatory at layout level, the use of Dual well technology can reduce multi cell upset by half. The important thing is to understand the failure mechanisms and to analyze the appropriateness of the layout for Multi bit Upset (MBU) and Multi Cell Upset (MCU) patterns in the word-line and bit-line directions. The maximum MCU in the vertical (bit-line) direction is much higher than horizontal (word-line) direction. [8] This is the point where we have to look into layout placement. The thing we observed that the presence of smaller P-Well regions in Deep N-Well process resulting in charge confinement and turn-on of NMOS-based parasitic bipolar transistors. Since the PMOS transistors are fabricated in larger N-Wells this mechanism was not found to be dominant. Thus, NMOS transistor upsets dominate the overall Soft Error of the Deep N-Well SRAMs.

In a large percentage of the MCU events, the even number of cells involved because in SRAM design, the cells share a well in the vertical direction with transistors from two cells adjacent to each other. As a result, the biasing of the well will affect an even number of cells more often for any ion hit in the vertical direction.[8] So For MCU's, this will result in a higher probability for an even number of bit errors than an odd number of bit errors.

For this design, wells run in the vertical direction with well contacts placed 64 cells apart vertically. NMOS transistors of adjacent cells are placed in the same well. Within a word (in horizontal direction), two adjacent cells will have half of the NMOS transistors within one p-well. Thus, all PMOS transistors within a cell are placed in one n-well, while NMOS transistors are placed in two separate p-wells. PMOS (and NMOS) transistors from different rows share a common well in the vertical direction. The wells are oriented in long strips, top to bottom as shown in figure 7b.



(a)



(b)

Figure 7a. Representational of layout placement of transistors for Deep N-Well SRAMs; Figure 8b. SRAM cells flipped and placed horizontally

Since, the horizontal SRAM cell dimension is 3X longer than the vertical direction; an ion-hit in the horizontal direction will affect a smaller number of cells, but the affected SRAM cells belong to different words stored in memory. As a result, interleaved memory with a distance of 4 will work fine.

V. SRAM CELL WITH FLIPPED CELL LAYOUT AND TWO TRI-STATE INVERTER

Here we merged both mitigation techniques in SRAM cell of SRAM so that we can take the benefit of both and consequently withstand with all kind of Single Event Effects (We can see the layout structure in fig.8). By the tri state inverter we increase critical charge and by cell flipping we increase the robustness of the cell. So we have increased the tolerance level of soft error at node, path and SRAM cell. Now the turn is to check whether the required structure is feasible or not.

We have chosen the CMOS 65nm technology for SRAM Single Port register, Dual Port Register and Single Port high speed register of different memory size. We have used Nanosim simulator with different versions for different memory registers and sizes. The way of calculating this extra capacitance is by making the layout of 1µm NMOS device and did post layout extraction up to 100µm device to extract out the parasitic capacitance. We found that the capacitance is around 0.5pf for each 1µm area. For simulation we have added this calculated extra capacitance into spice. The basic concern of this simulation is to check that there must be no increment in Memory Access Time, Memory read and write Setup time, Leakage and Dynamic Power.

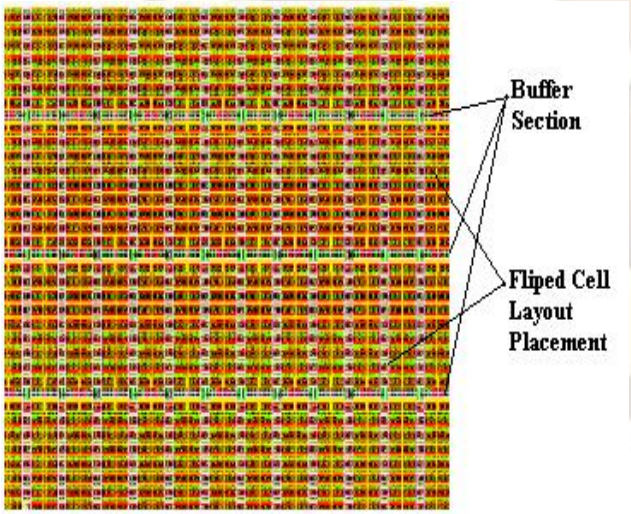


Figure 8. Layout Structure after addition of two Tri State Inverter and Cell Layout flipping

VI. RESULT AND SUMMARY

A. Timing Penalty for Memory Registers

In the timing penalty graph we are trying to compare the timing parameters of modified (mod) and non modify design simulation results. In the Single Port register simulation we have taken different memory size and different process voltage temperature combinations. But we saw the maximum impact on largest cut. The address setup time have no increment but in Access time and consequently Cycle time we can see a slight increment but it is not more than 1.6%. We can also observe in fig. 9 that the timing value has no big impact as the memory size increases.

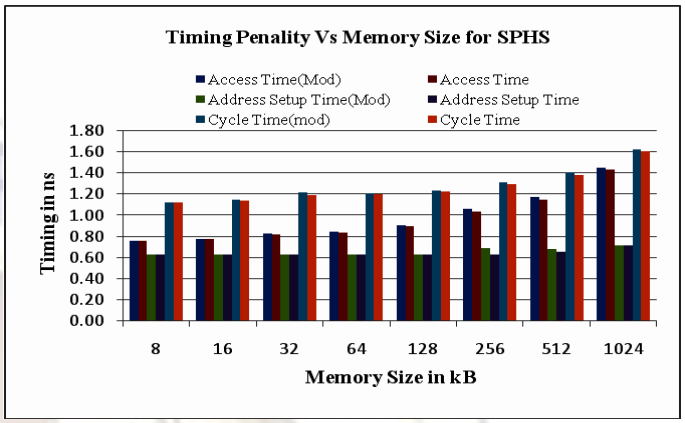


Figure 9. Graph shows the comparative structure of Timing Penalty of Access Time, Setup Time and Cycle Time for SPHS after modification

B. Dynamic Power Penalty for Memory Registers

Dynamic power is the sum of transient power consumption ($P_{transient}$) and capacitive load power (P_{cap}) consumption. Transient power represents the amount of power consumed when the device changes logic states, i.e. "0" bit to "1" bit or vice versa. Capacitive load power consumption represents the power used to charge the load capacitance. Together we find that

$$P_{dynamic} = P_{cap} + P_{transient} = (C_L + C)\, V_{dd}^2\, f\, N^3$$

Where C_L is the load capacitance, C is the internal capacitance of the IC, f is the frequency of operation, and N is the number of bits that are switching. We also see that dynamic power is data dependent and is in fact closely tied to the number of transistors that change states. So the Dynamic Power especially for our case is in much important. We observed after simulation that the maximum impact on SPHS that is around 4.5% for largest size 128kB.

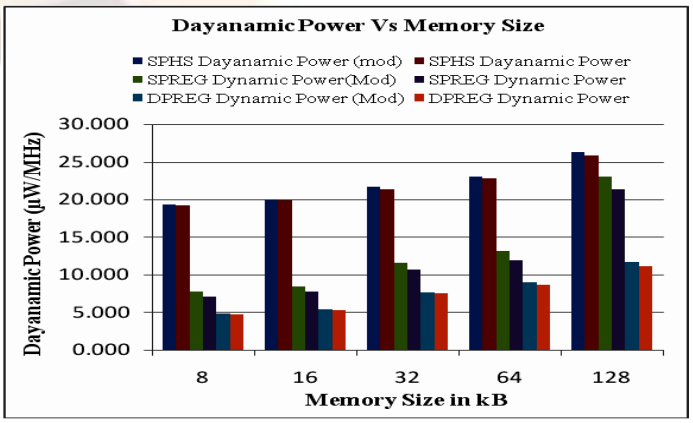


Figure 10. Graph shows the comparative structure of Dynamic Power for SPHS, SPREG and DPREG after modification

For the summary of whole thing we have shown table 1. We can see that no impact on Leakage and maximum impact on Dynamic power for write in the case of SPHS and all other timing parameters have not more than 3% impact.

S. No.	Parameters	Max Percentage Increment in Register for Tallest Cut		
		SPREG	SPHS	DPREG
1.	Access Time	3.00%	1.60%	2.70%
2.	Address Setup Time	3.20%	1.30%	1.40%
3.	Cycle Time	2.10%	1.60%	2.30%
4.	Power Read	2.20%	3.00%	1.40%
5.	Leakage Power	0.00%	0.00%	0.00%
6.	Power Write	2.40%	4.60%	1.70%

Table 1. Percentage increment in the parameters after addition of two Tri Stater Inverter and Cell Layout flipping.

VII. CONCLUSION

In this paper we want to aware industries that the ^{10}B can be exist in advance Si technology chips even though BPSG layer has been completely eliminated. The ^{10}B location is suggested right above the transistors between intermediate layer division and metal. We have proposed a mitigation technique which is having the advantage of increased node critical charge of SRAM Cell (By two tri State Inverters) and improved counteract of multi cell upset/multi bit upset soft errors (By SRAM cell flipping horizontal in layout). The SRAM becomes more thermal neutron tolerant even the ^{10}B exists in the device. The main virtue of this mitigation technique is to lead low power consumption, low timing penalty (Assess time, write time, setup time and read time) and low leakage power with high class of reliability.

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