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"An Implementation of WCDMA Rake Receiver on FPGA using VHDL Used In 3G Wireless Communications"

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Abstract
3G **mobile communications is advanced and emerging technology in the field of wireless communication also providing facilities like multimedia accessing, internet services, higher capacity of data rates and multiple services for same connection. The Rake receiver involves descrambling, dispreading, channel estimation and fading cancellation. The main principle behind Rake receiver is that they exploit multipath propagation by receiving the multipath components of the transmitted signal separately and combining their energies. The Rake receiver is used to tackle the problems of time dispersion (echoes) caused by multipath propagation in mobile communication. The above paper provides an introductory background on 3G communication and various objectives of 3G. To solve the above mention problems we have proposed architecture of WCDMA Rake receiver which is implemented in VHDL. The synthesis done by Xillling ISE 9.2i and simulation is done by ModelSim SE 6.3f.**

Keyword: **3G, multipath propagation, WCDMA, spreading, scrambling, fading cancellation.**

1. Introduction
The W-CDMA is a wideband Direct Sequence Code Division Multiple Access (DS-CDMA) system. This system provides very high bit rate (up to 2 Mbps) the use of variable spreading factor and multicode connections are supported. User information bits are spread over wide bandwidth by multiplying the user data with quasi-random bits (called chips) derived from CDMA spreading code. The chip rate of 3.84 Mcps and each channel bandwidth is approximately 5 MHz [1].

Table: 1 Comparisons of Data Rates of different Technology

Serial Number	Technology	Data Rate
FIRST	IS-95B	115.2 Kbps
SECOND	GPRS	171.0 Kbps
THIRD	EDGE	473.0 Kbps
FOURTH	WCDMA	2072.0 Kbps

The WCDMA supports highly variable user data rates (called Bandwidth on Demand) [1]. WCDMA supports Frequency Division Duplex (FDD) and Time Division Duplex (TDD). In FDD mode separate 5 MHz carrier frequencies are used for uplink and downlink respectively. WCDMA employs coherent detection on uplink and downlink based on the use of pilot symbols or common pilot. The WCDMA air interface has been crafted in such a way that advanced CDMA receiver concepts, such as multiuser detection and smart adaptive antennas, can be deployed by the network operator as a system option to increase capacity and/or coverage. This facility is not provided in second generation communication system. This 3G uses the technology called Code Division Multiple Access (CDMA).CDMA is used because of higher capacity, improved performance in multipath diversity and capable of handling high peak data rates (2Mbps). WCDMA is the enhanced technology of CDMA. In WCDMA in which for fading cancellation RAKE receiver is used.

The complete design to improve multipath propagation, can be segmented into distinct stages or blocks based on their functionality. The incoming data is fed to different fingers after different delays. In each finger the data is descrambled through descrambler and then despreaded through a matched filter. For descrambling, a Gold code generator also has been implemented, which can be initialized by external controls. For despreading the OVSF code sequence is taken as input to the chip. From matched filter outputs, we separate the information and pilot symbols. The pilot symbols are used to estimate the channel. After the channel characteristics are estimated, finally the outputs of all the fingers are combined together through a fading cancellation block. Rake receiver handles QPSK data and processes the in-phase and quadrature components of the data. The main objective of using a RAKE receiver is to combine the energies of all the multipath signals that reach the receiver within a Reasonable time window. The multipath propagation problems in mobile communication are improved using rake Receiver. Here we design the register block in asynchronous reset but synchronous output fashion that is very helpful to reduce the delay problem [3].

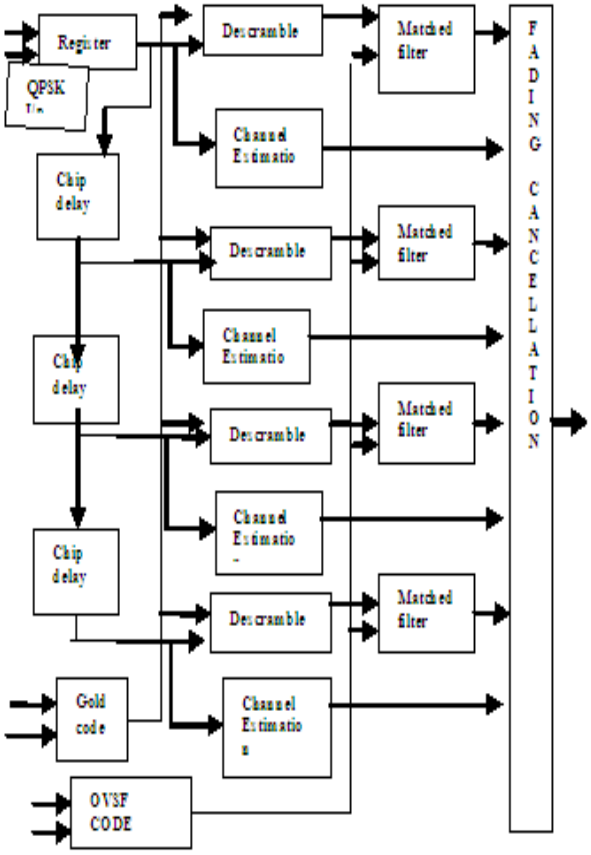

Fig. 1 Block diagram of the rake receiver

2. Problem Domain

A RAKE receiver is used to tackle the problems of time dispersion (echoes) caused by multipath propagation in mobile communications, where we most often don't have any line-of-sight between the transmitter and the receiver. Instead the signal reaches the receiver through a number of different paths, undergoing different and varying amounts of delay and attenuation [3]. This phenomenon is termed as fading and is observed as rapid fluctuations of the amplitude of a radio signal over a short period of time or travel distance. Fading is caused by interference between two or more versions of the transmitted signal, which arrive at the receiver at slightly different times. The physical factors influencing fading are [4]

- Multipath Propagation
- Speed of mobile
- Speed of surrounding objects
- The transmission bandwidth of the signal.

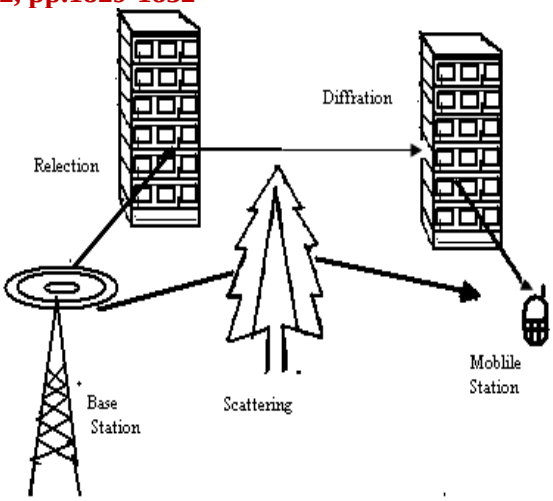

Fig. 2: Multipath propagation in mobile communications [3]

3. Solution Domain

Overview of the Design

The main principle of Rake receivers is that they exploit multipath propagation by receiving the multipath components of the transmitted signal separately and combining their energies. The complete design, for this purpose, can be segmented into distinct stages or blocks based on their functionality. The incoming data is fed to different fingers after different delays. In each finger the data is descrambled and then despreaded through a matched filter. For descrambling, a Gold code generator has also been implemented, which can be initialized by external controls. For despreading the OVSF code sequence is taken as an input to the chip. From matched filter outputs and channel estimation outputs, we separate the information and pilot symbols. The pilot symbols are used to estimate the channel. After the channel characteristics are estimated, finally, the outputs of all the fingers are combined together through a fading cancellation block. It should be noted that the design handles QPSK data and hence contains two parallel blocks, which interact with each other only in the 'Descrambler' & 'Fading Cancellation' blocks, to process the in-phase and quadrature components of the data. Here we design register block in such a manner to reduce delay, for that we design Register in a Asynchronous Reset but Synchronous Output fashion instead of Asynchronous Reset but Asynchronous Output .The waveform representation of register block are shown below:

4. Introduction of Function Block

The above diagram shows the major functional blocks of the design. The functions of all these blocks are mentioned below.

4.1 Register: We define two flip-flops – 'toggle' and 'follow' and configure them to realize edge-triggered-reset registers. In this design, at few places, registers have been used which can be cleared at the positive transition of the Reset input. A standard library component for this purpose is not available. Hence it was realized in the following way, using D flip-flops, which are very standard library components. The same block has been used wherever we needed edge-triggered-reset flip-flops/registers. Following are the benefits of such a scheme.

1. Better timing control: This removes the necessity of generating a reset pulse of accurate widths, which can be very demanding.
2. Increased testability: Not using the asynchronous control inputs of the flip-flops increases the controllability, and hence the testability, of the chip

4.1.1 Problem: Register is designed on the basis of asynchronous reset with asynchronous output. It will introduce more delay & unable to pass data at output until the reset pulse is not going down.

4.1.2 Solution: To solve this problem rregister are designed on the basis of asynchronous reset with synchronous output. Using this design of register we can pass data at the output on next rising edge of the clock. It will not wait for reset pulse goes down. This reduces the delay time rather than asynchronous reset with asynchronous output.

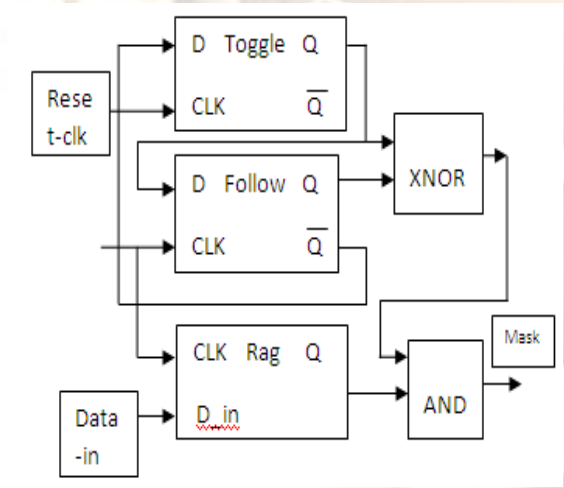

Fig. 3 Block diagram of the register block

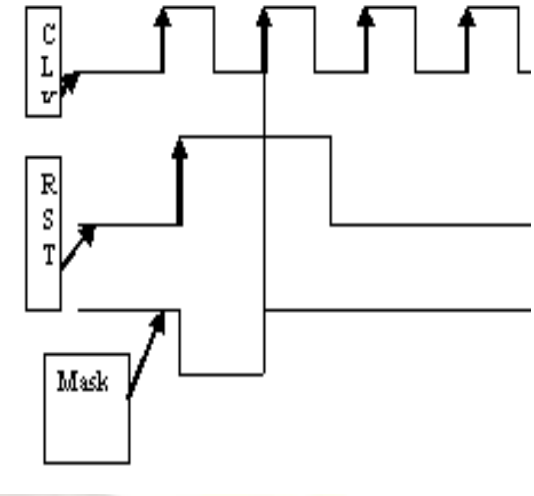

Fig. 4 **Wave form representation of register block**

4.2 Chip delay: The chip delay is used to introduce one chip period delay. This is implemented using a register.

4.3 Descrambler: It multiplies the incoming QPSK data by a complex code sequence, which is the complex conjugate of a Gold code sequence at transmitter end.

4.3 Gold code Generator: This block generates the Gold code whose complex conjugate is used as the 'Descrambling code' [8].

4.5 Matched Filter: This block performs the function of dispreading the incoming data, by multiplying it by the same OVSF code that is used at the transmitter to spread the information symbols, and accumulating the result over each information symbol period.

4.6 Channel estimation: This block finds the characteristics of the channel by processing the received values of the 'Pilot symbols' whose original sequence is known in advance at the receiver. The channel is estimated once for every slot of data.[9]

4.7 Fading Cancellation: This block is used to neutralize the channel effects and combine the signal in each of the fingers so as to increase SNR. This is done by multiplying the outputs of each finger by the complex conjugates of the corresponding channel characteristics and then adding their results. So we have to perform four complex multiplications for each information symbol. However, for this purpose, we have used a single multiplier.

5. Implemented Result Using Vhdl

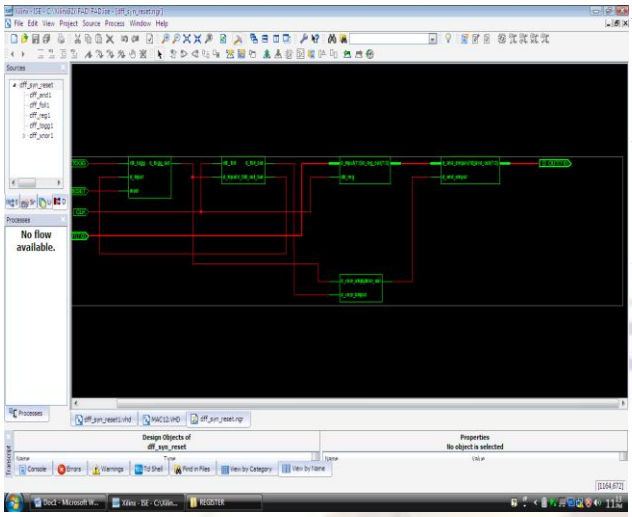

Fig. 5: Implementation of REGISTER BLOCK

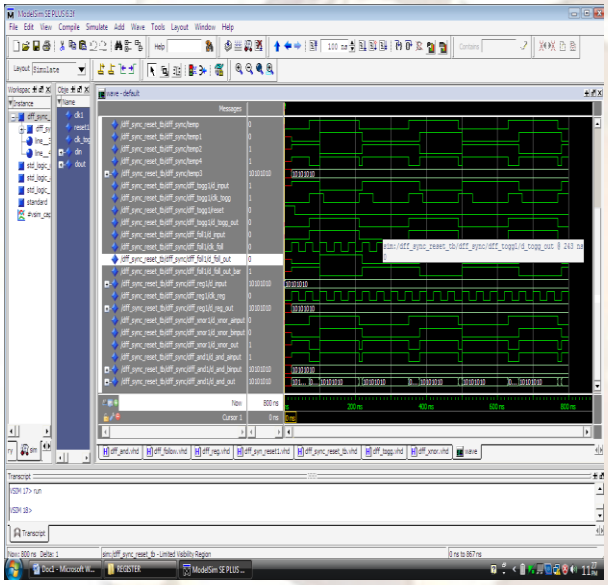

Fig. 6: Waveform results of REGISTER BLOCK

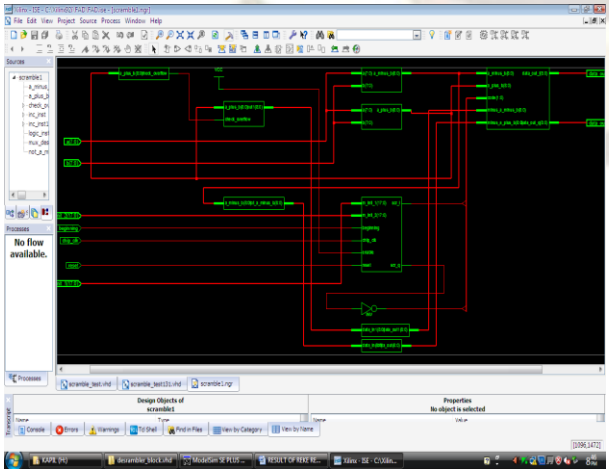

Fig. 7: Implementation of DESCRAMBLER BLOCK

7. Conclusion

Design the fading cancellation rake receiver that is very helpful to improve multipath propagation problems in 3G wireless communication. Here I have designed the register block in asynchronous reset but synchronous output fashion that is helpful to reduce the delay. It also provides better timing control and increase the testability. Because there are four figures in rake receiver that's why we are using QPSK modulation technique. So we can increase data rate up to certain limit. It is used in 3G mobile communication.

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