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Digital Implementation of 16-bit Synchronous Counter with SoC Encounter for Placement And Routing

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ABSTRACT
A synchronous counter, in contrast to an asynchronous counter, is one whose output bits change state simultaneously, with no ripple. A simple way of implementing the logic for each bit of an ascending counter is for each bit to toggle when all of the least significant bits are at a logic high state. In this paper we aim for the timing driven placement and routing of 16-bit synchronous counter aiming for the better setup and hold slack margins with out any design rule violations and observe the density of design at each and every step in the place and route flow. For placement and routing of the design we use SoC Encounter version 9.1 at 130nm technology.

Keywords – **Placement, Routing, Synchronous counter, SoC Encounter**

I. INTRODUCTION
The SoC Encounter System supports all implementation styles—from flat or hierarchical to single or multi-VDD. The system's fast automatic power grid design and optimization, global routing, in-place optimization, and global timing debug capabilities provide a robust infrastructure to implement any methodology. Full-chip flat prototyping delivers complete and accurate physical, timing, clock, and power data, thereby eliminating the guesswork associated with traditional block-based approaches.
SoC Encounter hierarchical support further helps physical designers to assess how best to partition the logical hierarchy in to physical modules by analyzing the optimal pin assignments; quick time budgeting; accurately predicting the clock distribution networks; analyzing the power grids; and eventually generating complete timing and physical constraints for each of the physical modules.

II. PLACEMENT AND ROUTING
The files that will be imported into the SOC Encounter tool to start Place and Route are the netlist file, timing constraint file, technology files and input-output pin assignment file.

After Importing the above files in to SoC Encounter we start placement and routing.

In floor planning step we decide how much area will be required for our design to place in the core area so that minimum wire length will be used to make connectivity between standard cells. We also create the power stripes and input output pins.

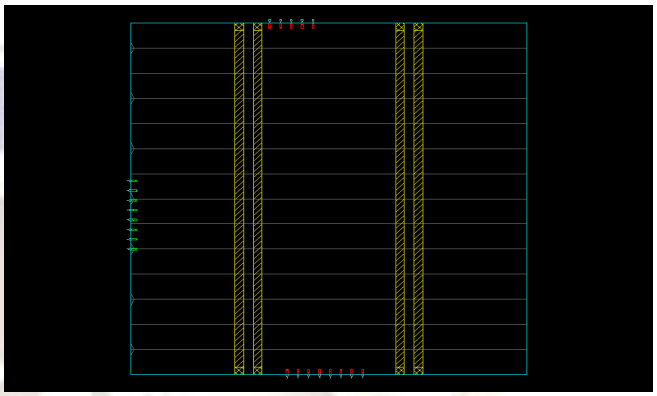

Fig.1: Floor Plan of counter

We allocated only 60% of area for the placement of standard cells during floor plan. Therefore the density of design before placement of standard cells is 60%.

The next step is placement. In this step we place the standard cells . Before the placement of standard cells we place the endcap cells to the left and right of the core so as to avoid process antenna violations and spacing violations. The simple idea is to minimize the length of wires, but, for example, in a timing-driven placement the intention is to decrease as much as possible the delay on the critical paths. So that timing will be met very easily.

The density of the design after placement is 68.85%. Now if we check for timing the tool will do a trail route automatically and gives the report. The term WNS indicates Worst Negative Slack on a particular path and TNS indicates Total Negative Slack.

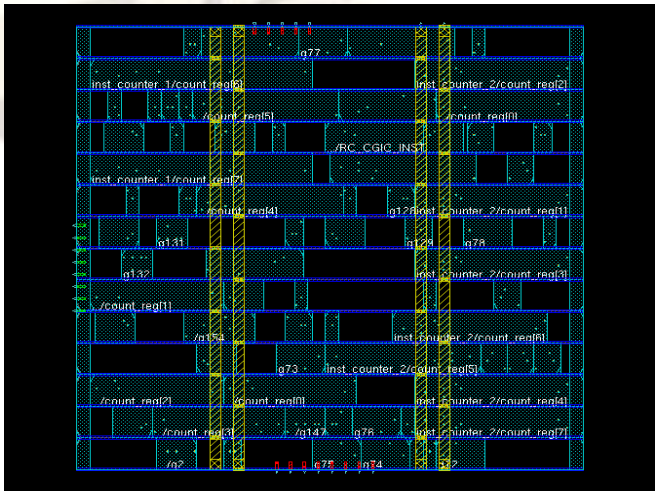

Fig.2: Placement

The timing report shown for this design at this stage is

Setup mode:
WNS: -0.112ns on input to register path
TNS: -0.305ns
Violating paths: 3

So the negative setup slack seen above is the worst slack reported among the three violating paths which is because of the nets that are routed by the tool as a trail route and this slack can be eliminated by optimizing the design. Optimization at this stage is referred to as Post-placement Optimization or Pre-CTS optimization.

After optimizing the design for removal of negative slack the density of the design has changed to 71.362%. The timing report shows that:

Setup mode:
WNS: 0.158ns on input to register path
TNS: 0.000ns
Violating paths: 0

Now the timing violation has been eliminated on the input to register path after optimization and setup slack has become positive.

The next step is generation of clock tree. It is termed as Clock Tree Synthesis (CTS). How the clock is distributed in a design is one of the most limiting factors in order to achieve high frequency circuits. The clock signal has to get all the clocked components at the same time in order to achieve a correct operation, and the more the frequency is increased, the more clock inaccuracy we have. The generated clock tree is highlighted in white lines as shown in Figure 4. The density of the design after clock tree synthesis is 79.034%.

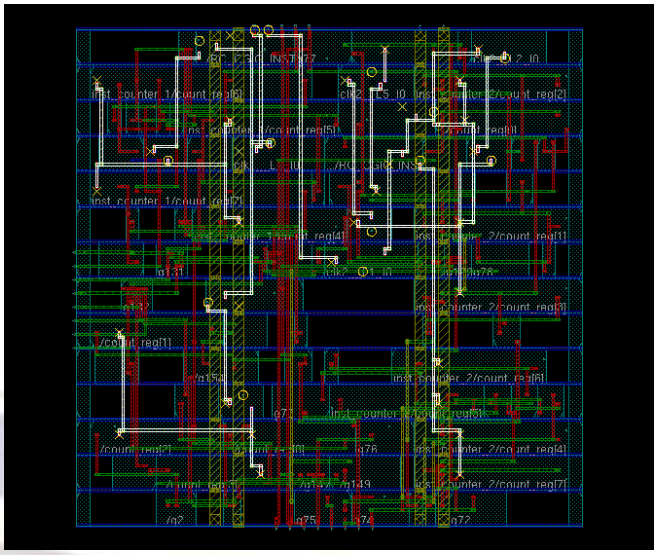

Fig.4: Clock Tree Synthesis

The timing report at this stage is:

Setup mode:
WNS: -0.182ns on register to output path
TNS: -0.328ns
Violating paths: 2

The negative setup slack seen in the report is mainly because during clock tree generation tool adds buffers to all the clock nets. This increases the path delay. So to eliminate this negative slack we optimize the design. This step is referred to as the Post-CTS optimization. After CTS we can also check for the hold violations. But in most of the cases we perform hold check after detailed routing only. Even if hold check is done at CTS stage we can easily fix the hold violations during Post-CTS optimization.

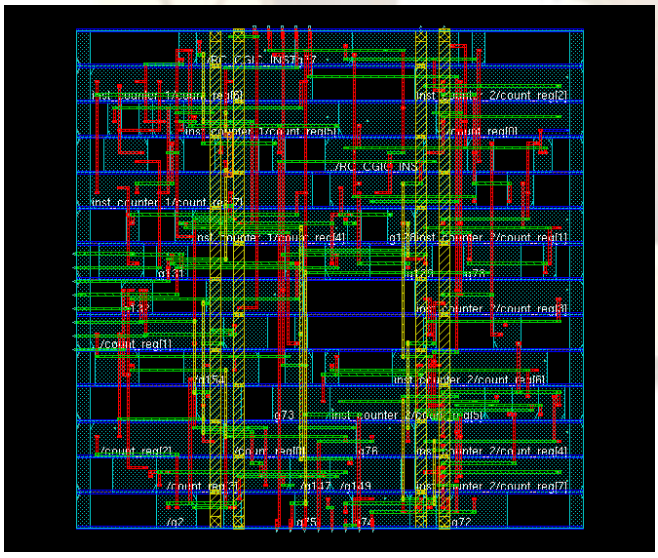

Fig.3: Pre-CTS Optimization

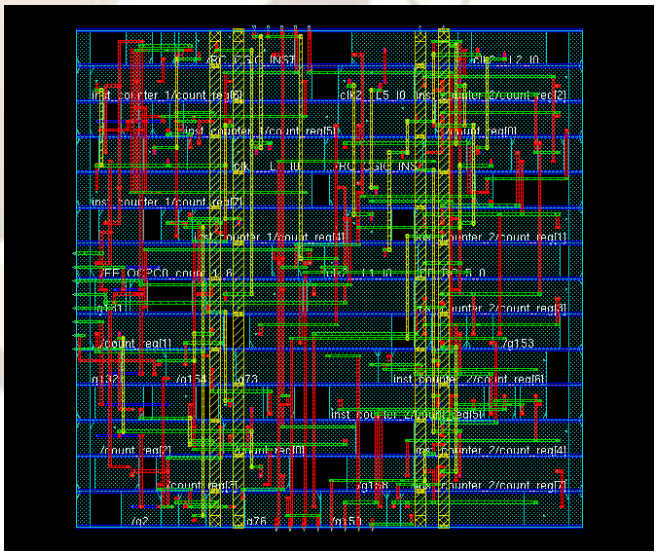

Fig.5: Post-CTS optimization

The Density of the design has become 88.69%. The timing report is shown below:

Setup mode:
WNS: 0.101ns on register to output path

TNS: 0.000ns
Violating paths: 0

After Post-CTS optimization it is clear that the setup violation on register to output path is eliminated and there are no violations on any other paths .

The next step is detailed routing. Here the tool does the actual timing driven sign-off routing. The trail route between the standard cells is removed.

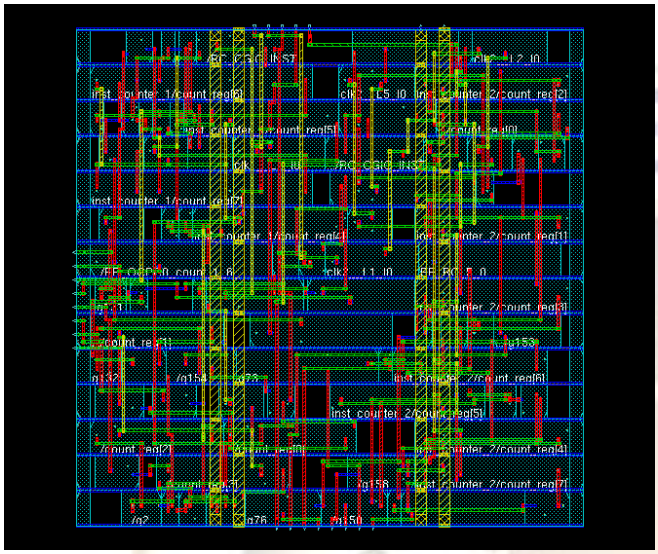

Fig.6: Detailed Routing

The density of the design has become 88.70%. The timing is checked for both setup and hold requirements. There is no need of fixing hold time at early stages of the design.

The timing report is shown below:

Setup mode:
WNS: 0.034ns on register to output path
TNS: 0.000ns
Violating paths: 0

Hold mode:
WNS: -0.163ns on register to register path
TNS: -0.338ns
Violating paths: 4

The hold violations are always fixed at post route optimization because the skews seen are real and to fix them tool can easily add buffers. Before detailed routing we only give priority for fixing the setup timing violations.

During Post-route optimization the tool optimizes the design by upsizing or downsizing the cells or by adding some buffers.

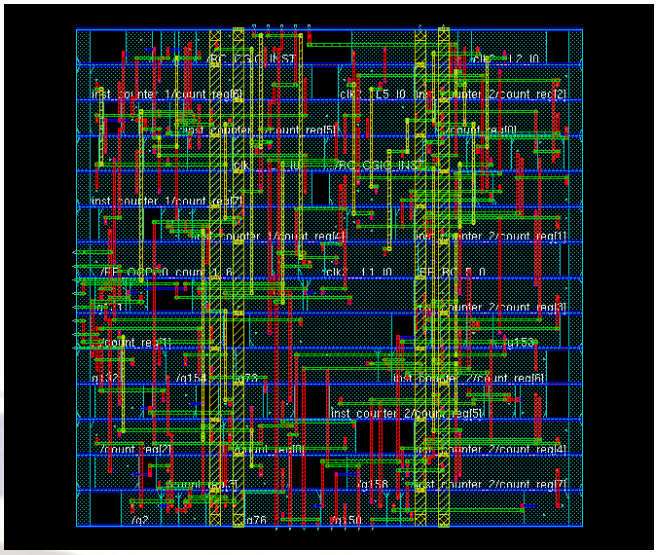

Fig.7: Post-route Optimization

The density of the design is 90.079%.The timing report is shown below:

Setup mode:
WNS: 0.034ns on register to output path
TNS: 0.000ns
Violating Paths: 0

Hold mode:
WNS: 0.016ns on register to register path
TNS: 0.000ns
Violating Paths: 0

It is clearly seen that the hold violations on all the four paths are removed after Post-route optimization. After this step we can fill the spaces in our design with the filler cells for the continuity of N-well regions to avoid any DRC violations.

III. CONCLUSION

Placement and routing of 16-bit synchronous counter is done at 130nm technology using SoC Encounter tool version 9.1. The timing reports at each and every step of the design are observed and if any violations they are removed and from the reports finally the setup slack is 0.034ns and the hold slack is 0.016ns. The density of the design is finally reported as 90.079%. The increase in density of the design at each and every step is mainly because of the increment in net lengths ,upsizing of the cells, addition of buffers.

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