P.SURENDRA BABU, Dr.BV. SANKER RAM / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 3, May-Jun 2012, pp.725-732

Design, Modeling and Simulation of Dynamic Voltage Restorer for Voltage Swell/Sag Mitigation

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Abstract:
While early FACTS devices consisted mainly of thyristor-controlled/switched RLC/transformer components, the newer generation is based on the self-commutated voltage-source power converter. Different shunt FACTS devices, namely Static VAR compensator (SVC) and Static Synchronous Compensator (STATCOM), Dynamic voltage restorer (DVR) in transmission line using the actual line model. This paper describes the problem of voltage sags and swells and its severe impact on non linear loads or sensitive loads. The dynamic voltage restorer (DVR) has become popular as a cost effective solution for the protection of sensitive loads from voltage sags and swells. The design procedure for various components of DVR is presented. Finally Matlab/Simulink based model is developed and simulation results are presented.

Keywords: SVC; D-Statcom; DVR; voltage dip, voltage swell ;

1. Introduction

The voltage generated by power stations has a sinusoidal waveform with a constant frequency. Any disturbances to voltage waveform can result in problems related with the operation of electrical and electronic devices. Users need constant sine wave shape, constant frequency and symmetrical voltage with a constant rms value to continue the production. This increasing interest to improve overall efficiency and eliminate variations in the industry have resulted more complex instruments that are sensitive to voltage disturbances. The typical power quality disturbances are voltage sags, voltage swells, interruptions, phase shifts, harmonics and transients. Among the disturbances, voltage sag is considered the most severe since the sensitive loads are very susceptible to temporary changes in the voltage. Voltage sag (dip) is a short duration reduction in voltage magnitude between 10% to 90% compared to nominal voltage from half a cycle to a few seconds [1-4].

Voltage swells are not as important as voltage sags because they are less common in distribution systems. Voltage sag and swell can cause sensitive equipment (such as found in semiconductor or chemical plants) to fail, or shutdown, as well as create a large current unbalance that could blow fuses or trip breakers. These effects can be very expensive for the customer, ranging from minor quality variations to production downtime and equipment damage [5-7]. There are many different methods to mitigate voltage sags and swells, but the use of a custom Power device is considered to be the most efficient method. Switching off a large inductive load or Energizing a large capacitor bank is a typical system event that causes swells [1].

2. Dynamic Voltage Restorer (DVR)

The main function of a DVR is the protection of sensitive loads from voltage sags/swells coming from the network. Therefore as shown in Figure 1 the DVR is located on approach of sensitive loads. If a fault occurs on other lines, DVR inserts series voltage VDVR and compesates load voltage to pre fault value. The momentary amplitudes of the three injected phase voltages are controlled such as to eliminate any detrimental effects of a bus fault to the load voltage *VL*. This means that any differential voltages caused by transient disturbances in the ac feeder will be compensated by an equivalent voltage generated by the converter and injected on the medium voltage level through the booster transformer.

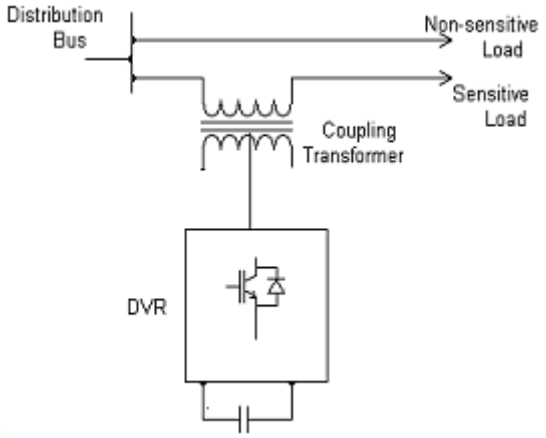

Fig.1 Basic Configuration of DVR

The DVR works independently of the type of fault or any event that happens in the system, provided that the whole system remains connected to the supply grid, i.e. the line breaker does not trip. For most practical cases, a more economical design can be achieved by only compensating the positive and negative sequence components of the voltage disturbance seen at the input of the DVR. This option is Reasonable because for a typical distribution bus configuration, the zero sequence part of a disturbance will not pass through the step down transformer because of infinite impedance for this component. The DVR has two modes of operation which are: standby mode and boost mode. In standby mode (*VDVR*=0), the booster transformer's low voltage winding is shorted through the converter. No switching of semiconductors occurs in this mode of operation, because the individual onverter legs are triggered such as to establish a short-circuit path for the transformer connection. Therefore, only the comparatively low conduction losses of the semiconductors in this current loop contribute to the losses. The DVR will be most of the time in this mode. In boost mode (*VDVR*>0), the DVR is injecting a compensation voltage through the booster transformer due to a detection of a supply voltage disturbance [4].

3. Design of various components of DVR

3.1 Device Currents Selection

The IGBT and DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles. Duty cycle, d = ½(1+Kmsinωt).

Where, m = modulation index K = +1 for IGBT, -1 for Diode.

$$i_{ph} = \sqrt{2}\, I \sin(\omega t - \text{o})$$

Where i = RMS value of the load (output) current,
Ø = Phase angle between load voltage and current.

Then the device current can be written as follows.

$$\therefore\ i_{device} = \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) * (1 + km \sin \omega t)$$

The average value of the device current over a cycle is calculated as

$$i_{avg} = \frac{1}{2\pi} \int_{\phi}^{\pi+\phi} \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) * (1 + k\, m \sin\omega t)\, d\omega t$$

$$= \sqrt{2}\, I \left[\frac{1}{2\pi} + \frac{K\, m}{8} \cos\phi\right]$$

The device RMS current can be written as

$$i_{rms} = \sqrt{\int_{\phi}^{\pi+\phi} \frac{1}{2\pi} \left(\sqrt{2}\, I \sin(\omega t - \phi)\right)^2 * \frac{1}{2} * \left((I + k\, m \sin\omega t)\, d\omega t\right)}$$

$$= \sqrt{2}\, I \sqrt{\left[\frac{1}{8} + \frac{K\, m}{3\pi} \cos\phi\right]}$$

3.2 IGBT Loss Calculation

IGBT loss can be calculated by the sum of switching loss +conduction loss. Where conduction loss can be calculated $P_{on\,(IGBT)} = V_{ceo} * I_{avg\,(igbt)} + I^2_{rms\,(igbt)} * r_{ceo}$

$$I_{avg(igbt)} = \sqrt{2}\, I \left[\frac{1}{2\pi} + \frac{m}{8} \cos\phi\right]$$

$$I_{rms(igbt)} = \sqrt{2}\, I \sqrt{\left[\frac{1}{8} + \frac{m}{3\pi} \cos\phi\right]}$$

Values of V_{ceo} and r_{ceo} at any junction temperature can be obtained from the output characteristics (Ic vs. Vce) of the IGBT as shown in fig 2.

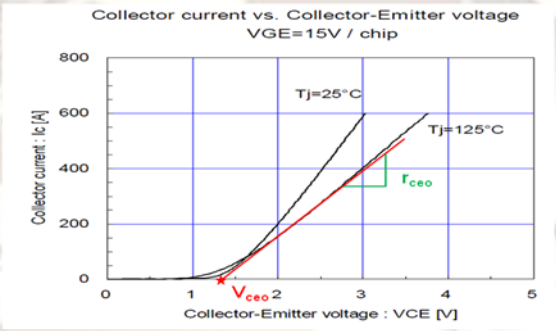

Fig 2:IGBT output characteristics

The switching losses are the sum of all turn-on and turn-off energies at the switching events

$$E_{sw} = E_{on} + E_{off} = a + b\, I + c\, I^2$$

Assuming the linear dependence, switching energy Here V_{DC} is the actual DC-Link voltage and V_{nom} is the DC-Link Voltage at which E_{sw} is given.

$$E_{sw} = (a + b\, I + c\, I^2) * \frac{V_{DC}}{V_{nom}}$$

Switching losses are calculated by summing up the switching energies.

$$P_{sw} = \frac{1}{T_o} \sum_{n} E_{sw}\,(i)$$

Here 'n' depends on the switching frequency.

$$P_{sw} = \frac{1}{T_o} \sum_{n} (a + b\, I + c\, I^2)$$

$$= \frac{1}{T_o} \left[\frac{a}{2} + \frac{b\, I}{\pi} + \frac{c\, I^2}{4}\right]$$

After considering the DC-Link voltage variations switching losses of the IGBT can be written as follows.

$$P_{sw\,(IGBT)} = f_{sw} \left[\frac{a}{2} + \frac{b\, I}{\pi} + \frac{c\, I^2}{4}\right] * \frac{V_{DC}}{V_{nom}}$$

So, the sum of conduction and switching losses gives the total losses.

$$P_{T\,(IGBT)} = P_{on\,(IGBT)} + P_{sw\,(IGBT)}$$

3.3 Diode Loss Calculation

The DIODE switching losses consists of its reverse recovery losses and the turn-on losses are negligible.

$$E_{rec} = a + b\,I + c\,I^2$$

$$P_{sw\,(DIODE)} = f_{sw}\left[\frac{a}{2} + \frac{b\,I}{\pi} + \frac{c\,I^2}{4}\right] * \frac{V_{DC}}{V_{nom}}$$

So, the sum of conduction and switching losses gives the total DIODE looses.

$$P_{T\,(DIODE)} = P_{on\,(DIODE)} + P_{sw\,(DIODE)}$$

The total loss per one switch (IGBT+DIODE) is the sum of one IGBT and DIODE loss.

$$P_T = P_{T\,(IGBT)} + P_{T\,(DIODE)}$$

3.4 Average Thermal Calculation

The junction temperatures of the IGBT and DIODE are calculated based on the device power losses and thermal resistances. The thermal resistance equivalent circuit for a module is shown in Fig 3. In this design the thermal calculations are started with heat sink temperature as the reference temperature. So, the case temperature from the model can be written as follows.

$$T_c = P_T\,R_{th(c-h)} + T_h$$

Here $R_{th(c-h)}$ = Thermal resistance between case and heat sink

P_T = Total Power Loss (IGBT+DIODE)

IGBT junction temperature is the sum of the case temperature and temperature raise due to the power losses in the IGBT.

$$T_{j(IGBT)} = P_{T\,(IGBT)}\,R_{th(j-c)IGBT} + T_c$$

DIODE junction temperature is the sum of the case temperature and temperature raise due to the power losses in the DIODE.

$$T_{j(DIODE)} = P_{T\,(DIODE)}\,R_{th(j-c)DIODE} + T_c$$

The above calculations are done based on the average power losses computed over a cycle. So, the corresponding thermal calculation gives the average junction temperatures. In order to make the calculated values close to the actual values, transient temperature values are to be added to the average junction temperatures.

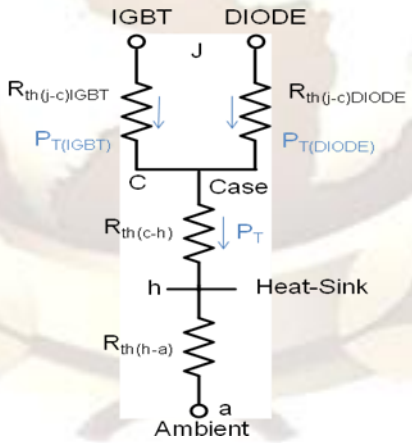

Fig. 3 Thermal resistance equivalent circuit

2.1. DC capacitor Selection

The required capacitance for each cell depends on the allowable ripple voltage and the load current. The rms ripple current flowing into the capacitor can be written as follows and the ripple current frequency is 6 times the load current frequency.

$$I_c = -\frac{I}{V_{dc}}\,\frac{1}{2}\,(|U_{ac}| * K + I\omega L)\,\sin(2\omega t)$$

Since the value of 'L' is very small, the above equation can be written as below.

$$I_c = -\frac{I}{V_{dc}}\frac{1}{2}\left(|U_{ac}| * K\right)\ \sin(2\omega t)$$

$$I_C = -K\frac{1}{2}\frac{|U_{ac}|}{V_{dc}} * \sin(2\omega t) = -K\frac{m}{2}\ \sin(2\omega t)$$

Here 'm' is the modulation index.

Here $I_{cp} = C\ \frac{du_{pp}}{dt}$

$$\frac{m}{2}\ I\sqrt{2} = \mathrm{C}\ 2\omega * \Delta V\ V_{dc}$$

$$\mathrm{C} = \frac{m}{4\omega}\frac{1}{\Delta V\ V_{dc}}\sqrt{2}\ I$$

4. Matlab/Simulink Modeling of DVR

The Matlab/Simulink model of DVR is shown in Fig.4. This Three main blocks named as source block, sag/swell creation block and inverter block.

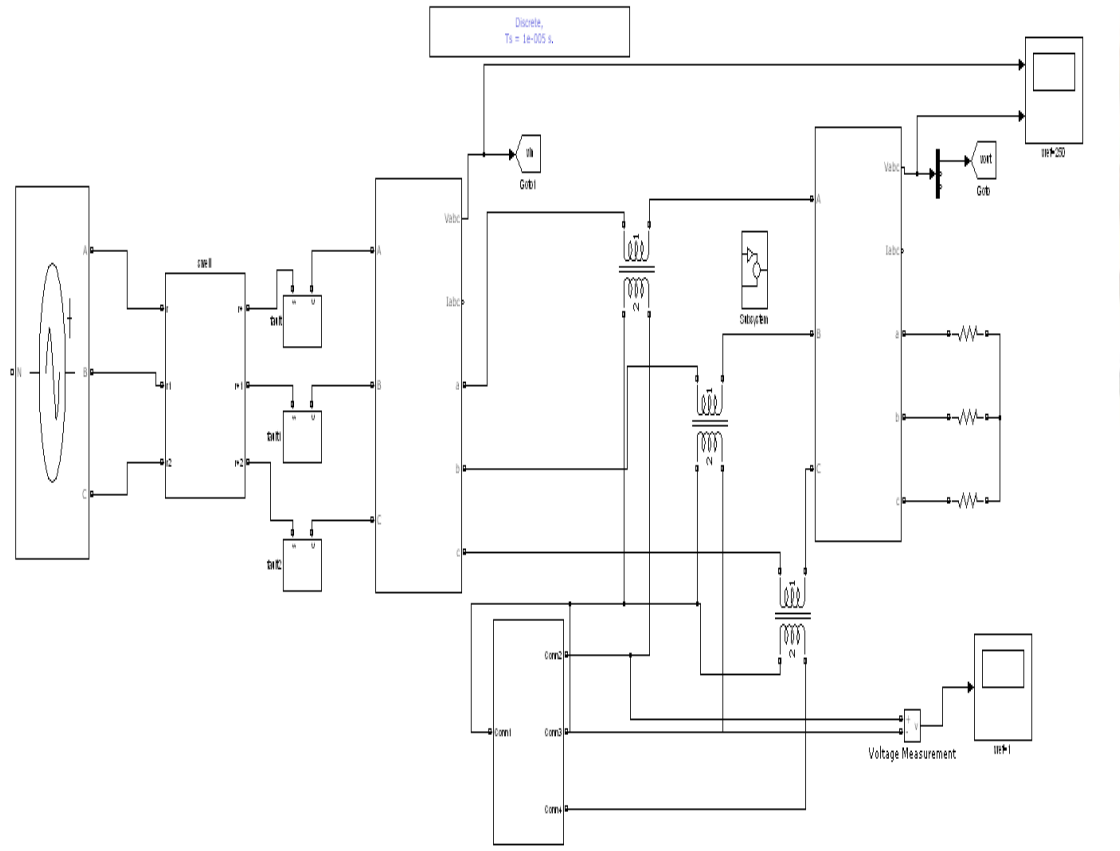

Fig.4 Control Scheme and test system implemented in MATLAB/SIMULINK to carry out DVR simulation

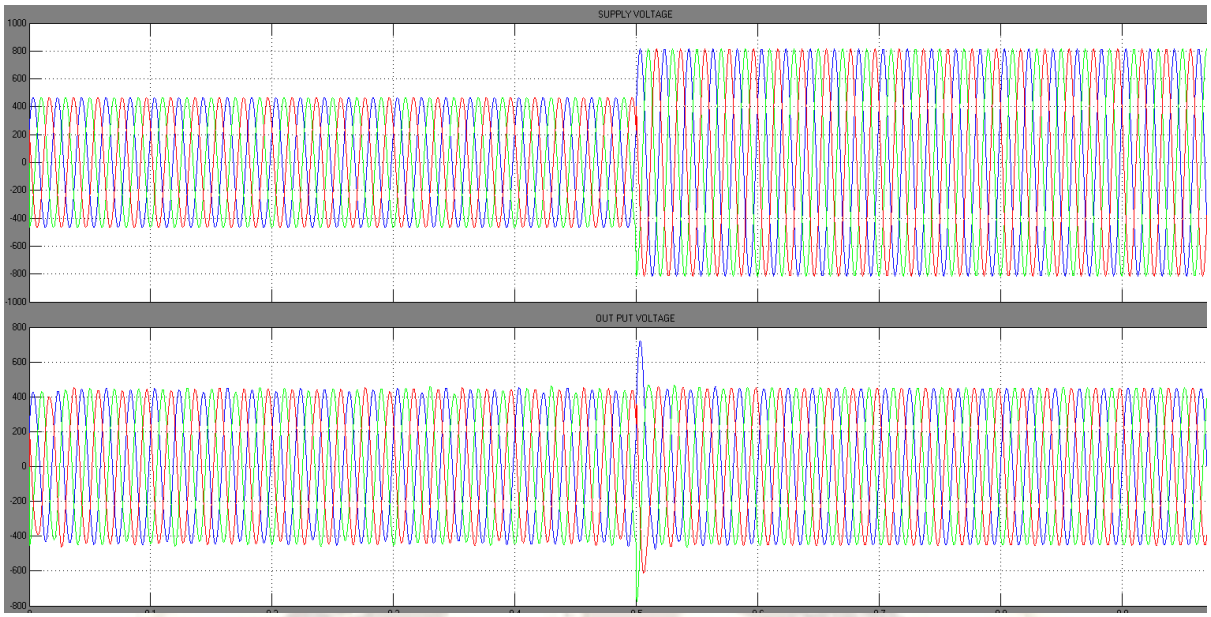

Fig. 5 Source voltage and Load voltage during Voltage Swell

Fig.5 shows simulation results for voltage swell compensation. It is clear that even though there is increase in supply voltage the output voltage is almost constant.

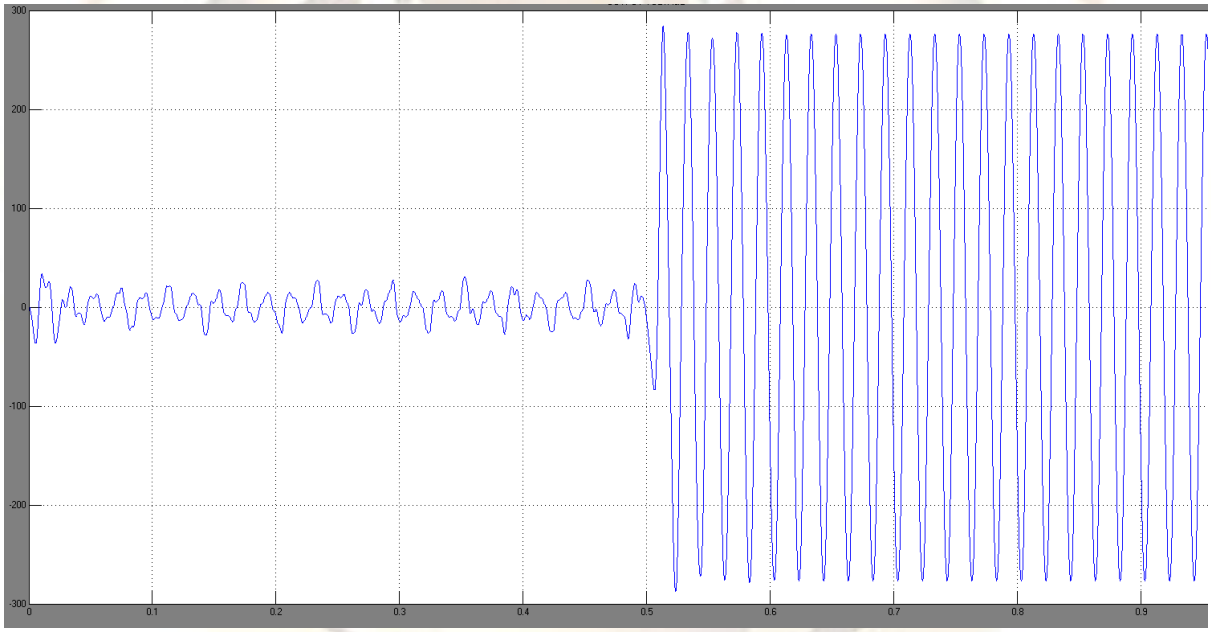

Fig. 6 Inverter output voltage during voltage swell mitigation

Fig.6 shows the inverter output voltage. It is clear that under normal condition inverter output voltage is zero, but during swell inverter is producing equal and opposite voltage to swell.

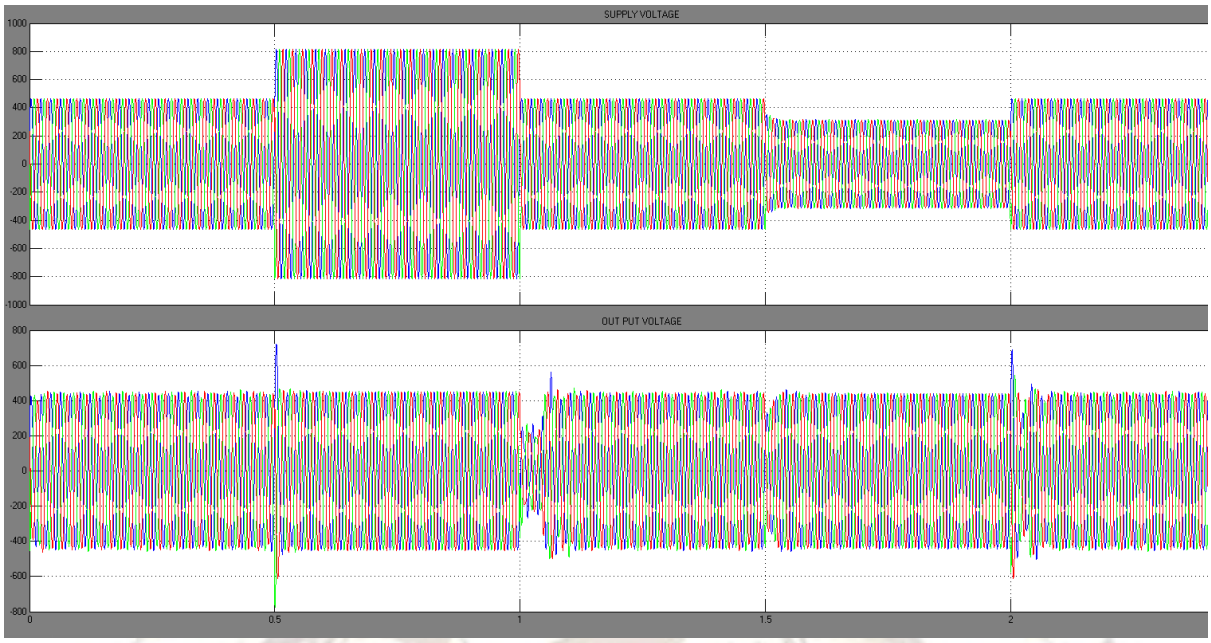

Fig. 7 Source voltage and Load voltage during Voltage Swell and Sag

Fig.7shows simulation results for voltage swell and sag compensation. From the simulation result it is clear that even through there is swell and sag in the supply voltage, output voltage is almost constant.

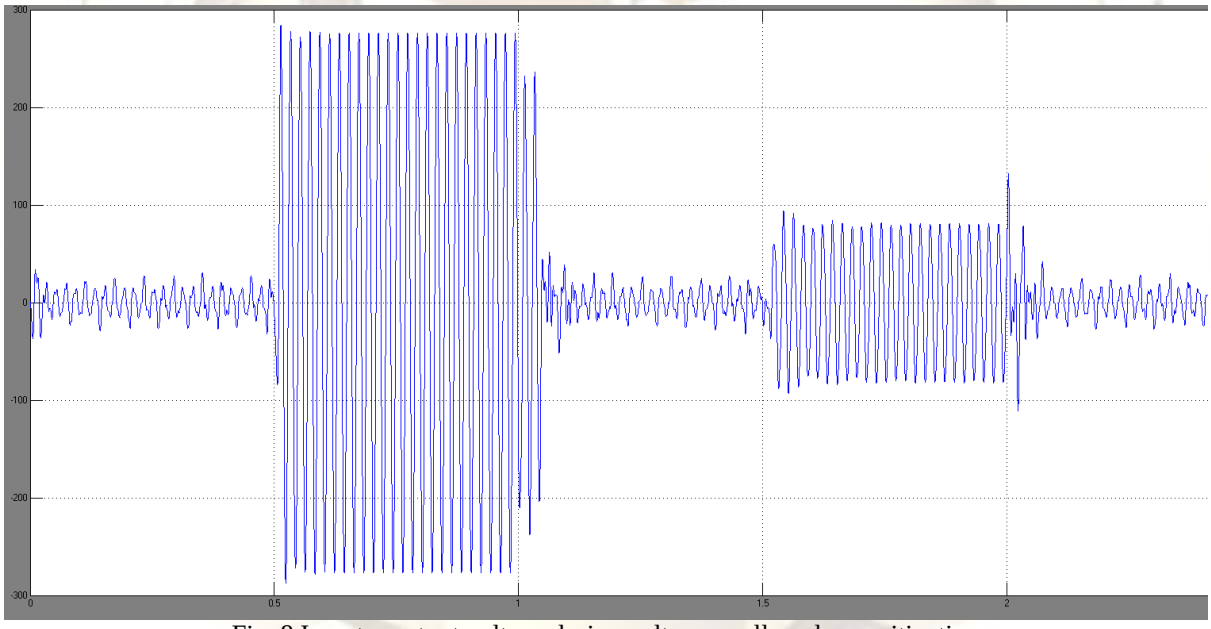

Fig. 8 Inverter output voltage during voltage swell and sag mitigation

Fig.8 shows the inverter output voltage. It is clear that under normal condition inverter output voltage is zero, but during swell inverter is producing equal and opposite voltage to swell and sag

6.Conclusion

This paper describes the problem of voltage sags and swells and its severe impact on non linear loads or sensitive loads. The dynamic voltage restorer (DVR) has become popular as a cost effective solution for the protection of sensitive loads from voltage sags and swells. The design procedure for various components of DVR is presented. Finally Matlab/Simulink based model is developed and simulation results are presented.

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