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A Novel Simplified Single-Phase and Three phase Multi string Multilevel Inverter Topology for Distributed Energy Resources

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Abstract-The concept of multilevel inverters, introduced about 20 years ago entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. The benefits are especially clear for medium-voltage drives in industrial applications and are being considered for future naval ship propulsion systems. Several topologies for multilevel inverters have been proposed over the years; the most popular cascaded H-bridge apart from other multilevel inverters is the capability of utilizing different dc voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher-frequency inverters. Considering the cascaded inverter to be one unit, it can be seen that a higher number of voltage levels are available for a given number of semiconductor devices. The simplified multilevel inverter requires only six active switches instead of the eight required in the conventional cascaded H-bridge multilevel inverter. In addition, two active switches are operated at the line frequency. The studied multistring inverter topology offers strong advantages such as improved output waveforms, smaller filter size, and lower electromagnetic interference and total harmonics distortion. Finally an asymmetrical configuration is proposed with this we are getting seven levels with six switches.

***Index items-Multistring inverter,* DC/AC power conversion**

I. INTRODUCTION

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. Among the multilevel Converters [1-4], the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels.

Additionally, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than alternative multilevel converters. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [5-11]. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems voltage clamping requirement, circuit layout, and packaging constraints.

A single-phase multi string five-level inverter integrated with an auxiliary circuit was recently proposed for dc/ac power conversion [12], [13]. This topology used in the power stage offers an important improvement in terms of lower component count and reduced output harmonics. Unfortunately, high switching losses in the additional auxiliary circuit caused the efficiency of the multi string five-level inverter to be approximately 4% less than that of the conventional multi string three-level inverter [13]. In [14], a novel isolated single-phase inverter with generalized zero vectors (GZV) modulation scheme was first presented to simplify the configuration. However, this circuit can still only operate in a limited voltage range for practical applications and suffer degradation in the overall efficiency as the duty cycle of the dc-side switch of the front-end conventional boost converter approaches unity [6], [14]. Furthermore, the use of isolated transformer with multi windings of the GZV based inverter results in the larger size, weight, and additional expense [14]. The newly constructed inverter topology offer strong advantages such as improved output waveforms, smaller filter size, and lower EMI and total harmonics distortion (THD). In this letter, the operating principle of the developed system is described, and a prototype is constructed for verifying the effectiveness of the topology.

II. SYSTEM CONFIGURATION OF OPERATION PRINCIPLES

A general overview of different types of PV modules or fuel cell inverters is given in [9] and [17]. This letter presents a multi string multilevel inverter for DERs application. The multi string inverter shown in Fig. 1 is a further development of the string inverter, whereby several strings are interfaced with their own dc/dc converter to a common inverter [18]. This centralized system is beneficial because each string can be controlled individually. Thus, the operator may start his own PV/fuel cell power plant with a few modules. Further enlargements are easily achieved because a new string with a dc/dc converter can be plugged into the existing platform, enabling a flexible design with high efficiency [9]. The single-phase multi string multilevel inverter topology used in this study is shown in Fig. 2.

This topology configuration consists of two high step-up dc/dc converters connected to their individual dc-bus capacitor and a simplified multilevel inverter. Input sources, DER module 1, and DER module 2 are connected to the inverter followed a linear resistive load through the high step-up dc/dc converters. The studied simplified five-level inverter is used instead of a conventional cascaded pulse width-modulated (PWM) inverter because it offers strong advantages such as improved output waveforms, smaller filter size, and lower EMI and THD [19]–[25]. It should be noted that, by using the independent voltage regulation control of the individual high step-up converter, voltage balance control for the two bus capacitors Cbus1, Cbus2 can be achieved naturally.

A Full H-Bridge

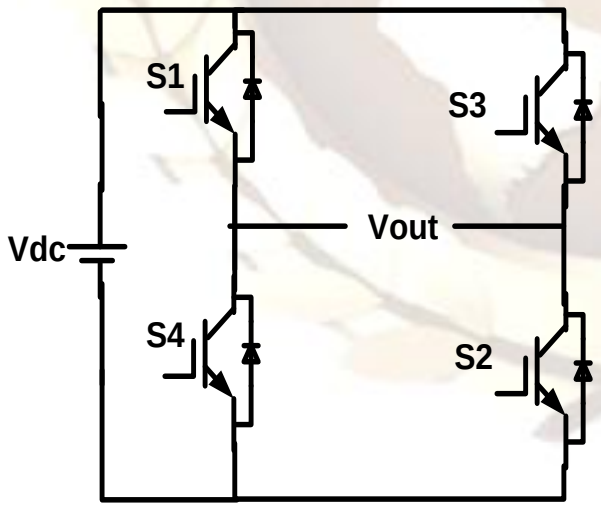

Figure. 1 Full H-Bridge

Fig.1 shows the Full H-Bridge Configuration. By using single H-Bridge we can get 3 voltage levels. The number output voltage levels of cascaded Full H-Bridge are given by 2n+1 and voltage step of each level is given by Vdc/n. Where n is number of H-bridges connected in cascaded. The switching table is given in Table 1.

Table 1. Switching table for Full H-Bridge

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

B. Simplified Multilevel Inverter Stage

A new single-phase multi string topology, presented as a new basic circuitry in Fig. 2. Referring to Fig. 2, it should be assumed that, in this configuration, the two capacitors in the capacitive voltage divider are connected directly across the dc bus, and all switching combinations are activated in an output cycle. The dynamic voltage balance between the two capacitors is automatically controlled by the preceding high step-up converter stage. Then, we can

Assume $Vs1 = Vs2 = Vs$

This topology includes six power switches—two fewer than the CCHB inverter with eight power switches—which drastically reduces the power circuit complexity and simplifies modulator circuit design and implementation. The phase disposition (PD) PWM control scheme is introduced to generate switching signals and to produce five output-voltage levels: 0, VS, $2VS$, $-VS$, and $-2VS$.

This inverter topology uses two carrier signals and one reference to generate PWM signals for the switches. The modulation strategy and its implemented logic scheme in Fig. 3(a) and (b) are a widely used alternative for PD modulation .With the exception of an offset value equivalent to the carrier signal amplitude, two comparators are used in this scheme with identical carrier signals $Vtri1$ and $Vtri2$ to provide high-frequency switching signals for switches $Sa1$, $Sb1$, $Sa3$, and $Sb3$. Another comparator is used for zero-crossing detection to provide line-frequency switching signals for switches $Sa2$ and $Sb2$.

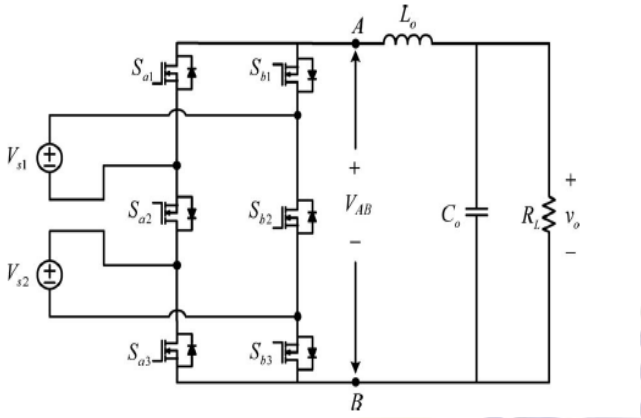

Figure. 2 Basic five-level inverter circuitry

For convenient illustration, the switching function of the switch in Fig. 2 is defined as follows:

$$S_{aj} = \begin{cases} 1, & S_{aj}\ \text{ON} \\ 0, & S_{aj}\ \text{OFF} \end{cases}, \quad j = 1, 2, 3$$

$$S_{bj} = \begin{cases} 1, & S_{bj}\ \text{ON} \\ 0, & S_{bj}\ \text{OFF} \end{cases}, \quad j = 1, 2, 3.$$

The required five output levels and the corresponding operation modes of the multi level inverter stage are described clearly as follows.

1) Maximum positive output, 2*VS* : Active switches *Sa* 2, *Sb* 1 , and *Sb* 3 are ON; the voltage applied to the *LC* output filter is 2*VS* .

2) Half-level positive output, +*Vs* : This output condition can be induced by two different switching combinations. One switching combination is such that active switches *Sa* 2, *Sb* 1, and *Sa* 3 are ON; the other is such that active switches *Sa* 2 , *Sa* 1 , and *Sb* 3 are ON. During this operating stage, the voltage applied to the *LC* output filter is +*Vs* .

3) Zero output, 0: This output condition can be formed by either of the two switching structures. Once the left orright switching leg is ON, the load will be short-circuited, and the voltage applied to the load terminals

4) Half-level negative output,−*Vs* : This output condition can be induced by either of the two different switching combinations. One switching combination is such that active switches *Sa* 1 , *Sb* 2 , and *Sb* 3 are ON; the other is such that active switches *Sa* 3 , *Sb* 1 , and *Sb* 2 are ON.

5) Maximum negative output,−2*Vs* : During this stage, active switches *Sa* 1 ,*Sa* 3 , and *Sb* 2 are ON, and the voltage applied to the *LC* output filter is −2*Vs* .

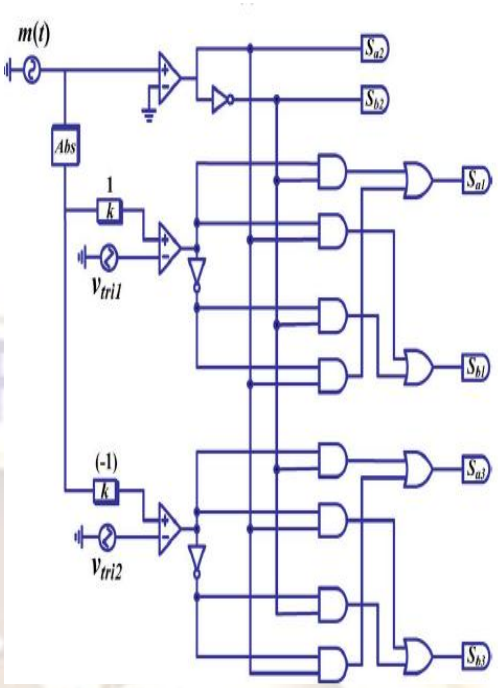

Figure.3 Modulation strategy: (a) carrier/reference signals; (b) modulation logic

III. MATLAB/SIMULINK MODEL & SIMULATION RESULTS

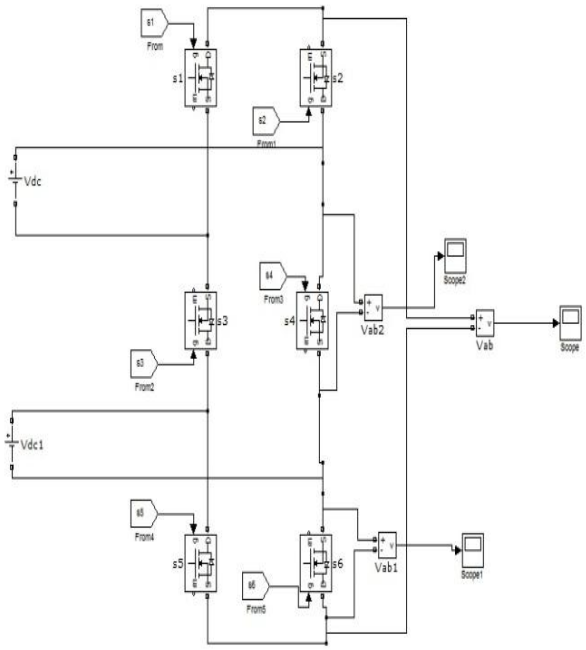

Figure.4 Simulation circuit

The basic simulation circuit, Figure.4 is a multi string inverter with combination six switches. Based on the selection of switches in the circuit output voltage are obtained.

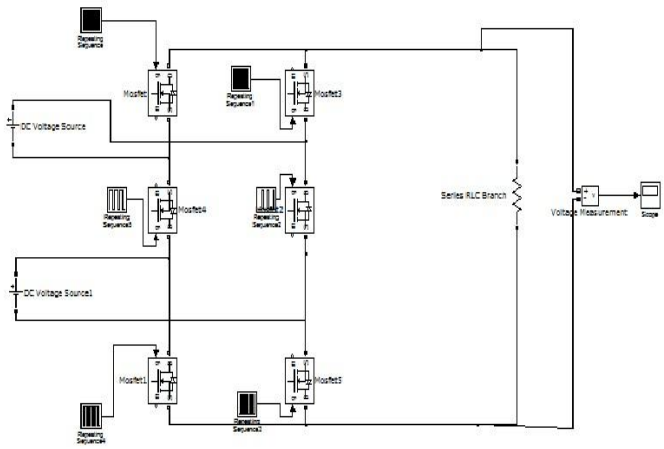

Figure.5 The simulation circuit of 7level inverter

Figure.5 shows the 7 level multi string inverter which is having the same 5 level circuit but obtaining the 7 level output voltages

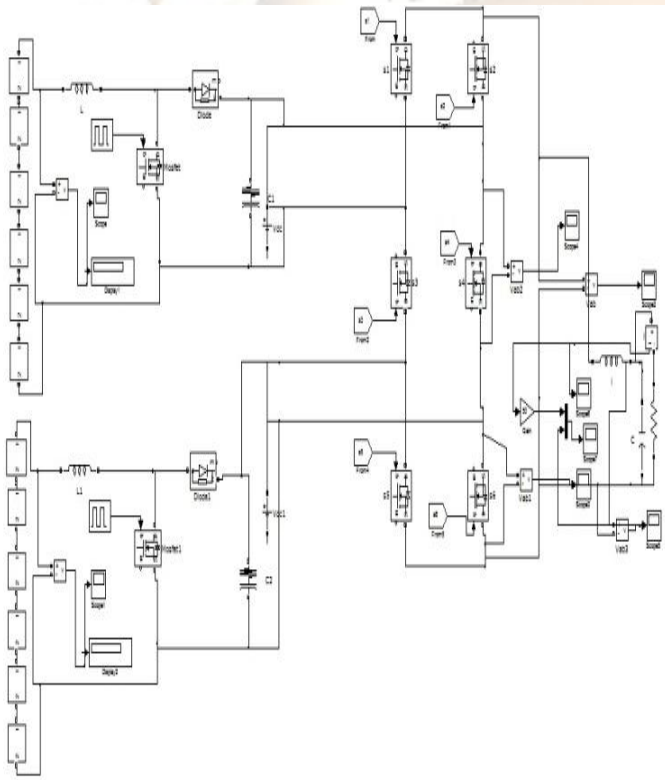

Figure.6 Simulation circuit of multi string inverter with photo voltaic

Figure.6 is a multi string inverter with a photo voltaic array, such that a group of photo voltaic cells together forms as an energy source.

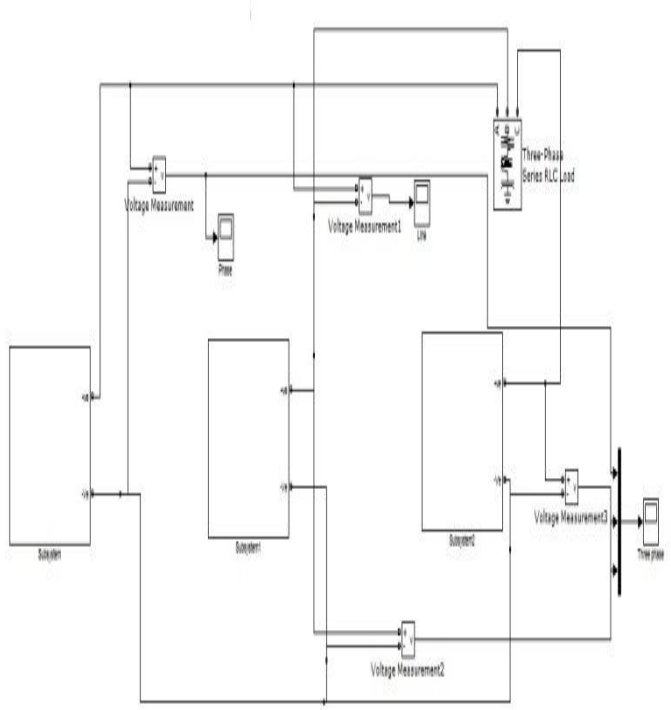

Figure.7 Simulation circuit of three phase multi string inverter

Figure.7 is a three phase multi string inverter, which is a combination three single phase multi string inverters.

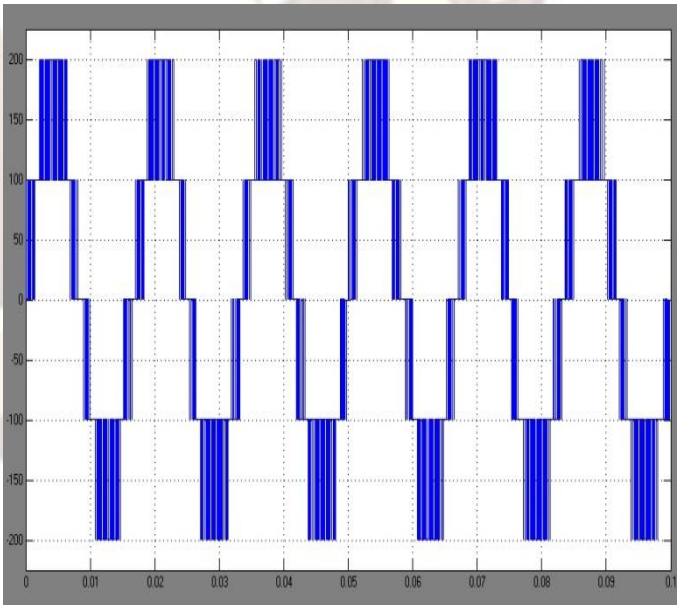

Figure.8 Output voltage waveform of 5 level multi sting inverter using PWM

Figure.8 shows the output voltages which are obtained by the multi string inverter of 5 level using PWM

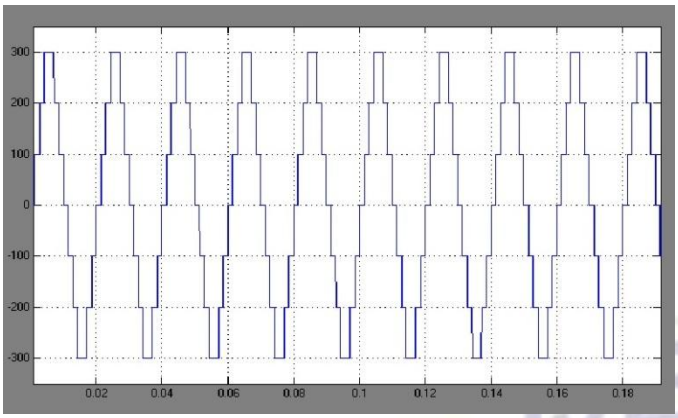

Figure.9 Output voltage waveform of 7level multi string inverter

Figure.9 shows the 7 level output voltage waveform of multi string inverter.

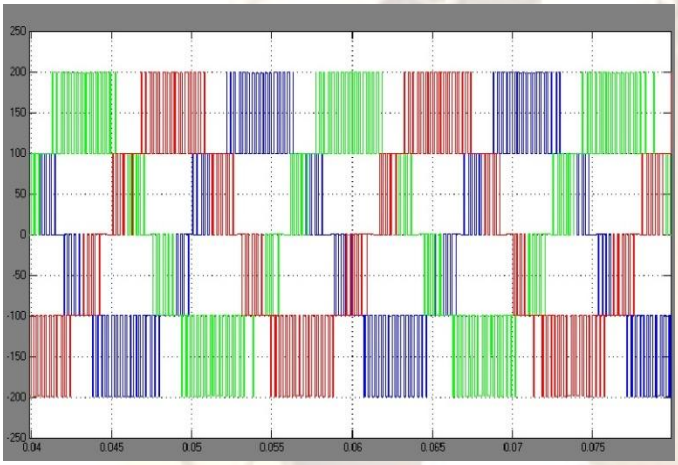

Figure. 10 Three phase output voltage of three phase multi string inverter

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IV.CONCLUSION

This paper presents Novel Asymetrical multistring multilevel converter. The proposed converter produces more voltage levels with less number of switches compared to H- bridge configuration. This will reduce number of gate drivers and protection circuits which in turn reduces the cost and complexity of the circuit. Finally a three phase model of the proposed circuit is shown and simulation results are presented.