COMPARISON AMONG DIFFERENT CMOS INVERTER WITH STACK KEEPER APPROACH IN VLSI DESIGN

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ABSTRACT

For the most recent CMOS feature sizes (e.g. , 90 nm and 65 nm) , leakage power dissipation has become an overriding concern for VLSI circuit designers. Leakage power consumption of current CMOS technology is already a great challenge. International Technology Roadmap for Semiconductors projects that leakage power consumption may come to dominate total chip power consumption as the technology feature size shrinks. This directly affects portable battery operated devices such as cellular phones and PDAs since they have long idle times. Several techniques used to efficiently minimize this leakage power loss. Stack keeper is a leakage reduction technique. Leakage is a serious problem particularly for CMOS circuits in nanoscale technology. We propose a novel ultra-low leakage CMOS circuit structure which we call "stack keeper." Unlike many other previous approaches, stack keeper can retain logic state during sleep mode while achieving ultra-low leakage power consumption. We apply the stack keeper to generic logic circuits. Although the stack keeper incurs some delay and area overhead, the stack keeper technique achieves the lowest leakage power consumption among known state-saving leakage reduction techniques, thus, providing circuit designers with new choices to handle the leakage power problem.

Keywords— **CMOS inverter, Low-leakage power dissipation, Sleepy stack, Stack keeper, Transistor stacking.**

I. INTRODUCTION

Power consumption is one of the top concerns of VLSI circuit design, for which CMOS is the primary technology. Today's focus on low power is not only because of the recent growing demands of mobile applications. Even before the mobile era, power consumption has been a fundamental problem. To solve the power dissipation problem, many researchers have proposed different ideas from the device level to the architectural level and above. However, there is no universal way to avoid tradeoffs between power, delay, and area, and thus, designers are required to choose appropriate techniques that satisfy application and product needs. Power consumption of CMOS consists of dynamic and static components. Dynamic power is consumed when transistors are switching and static power is consumed regardless of transistor switching. Dynamic power consumption was previously (at 0.18- m technology and above) the single largest concern for low-power chip designers since dynamic

power accounted for 90% or more of the total chip power. Therefore, many previously proposed techniques, such as voltage and frequency scaling, focused on dynamic power reduction. However, as the feature size shrinks, e.g., to 0.09 and 0.065 m, static power has become a great challenge for current and future technologies. Based on the International Technology Roadmap for Semiconductors (ITRS) [3], Kim *et al.* report that sub-threshold leakage power dissipation of a chip may exceed dynamic power dissipation at the 65-nm feature size.

II. PROPOSED APPROACH

One of the main reasons causing the leakage power increase is the increase of sub-threshold leakage power. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device decreases the threshold voltage even lower. In addition to sub-threshold leakage, another contributor to leakage power is gate-oxide leakage power due to the tunneling current through the gate-oxide insulator. Since gate oxide thickness may reduce as the channel length decreases, in sub 0.1- m technology, gate-oxide leakage power may be comparable to sub-threshold leakage power if not handled properly. However, we assume other techniques will address gate-oxide leakage; for example, high-dielectric gate insulators may provide a solution to reduce gate-leakage [4]. Therefore, this paper focuses on reducing
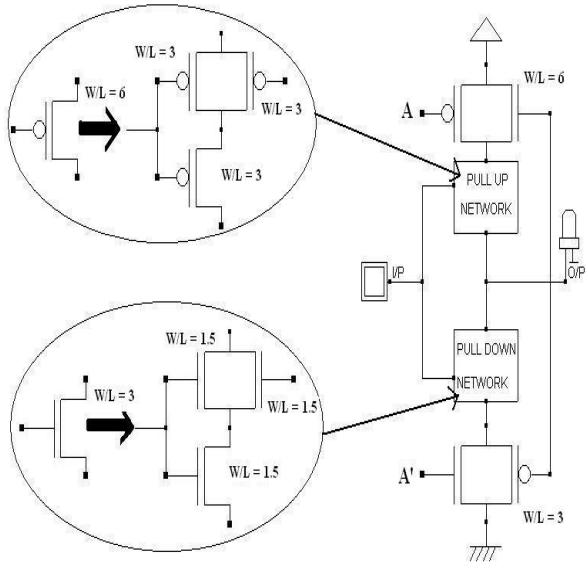
Fig 1 :- SLEEPY STACK KEEPER

sub-threshold leakage power consumption. In this paper, we provide a new circuit structure named "stack keeper" as a remedy for static power consumption. The stack keeper has a novel structure that uniquely combines the advantages of two major prior approaches, the sleep transistor technique and the forced stack technique. However, unlike the sleep transistor technique, the stack keeper technique retains the original state; furthermore, unlike the forced stack technique, the stack keeper technique can utilize high- to achieve up to two orders of magnitude leakage power reduction compared to the forced stack. Unfortunately, the stack keeper technique comes with delay and area overheads. Therefore, the stack keeper technique provides new Pareto points [5] to designers who require ultra-low leakage power consumption and are willing to pay some area and delay cost. The main contributions of this paper are as follows: 1) introduction of a stack keeper structure that can save leakage power up to two orders of magnitude for circuits that require extremely low leakage power consumption and 2) analysis of example stack keeper logic circuits in terms of various ways (transistor scaling, threshold voltage, and transistor width) circuit design engineers can employ to adopt the stack keeper technique as necessary. This paper is organized as follows. In Section II, prior work about low-leakage logic design is discussed. In Section III, the stack keeper structure is explained and an analytical delay model is discussed. In Section IV, an empirical methodology applying the stack keeper to generic logic is explained. In Section V, the experimental results of the stack keeper for generic logic is presented. In Section VI, conclusions are given.

As technology scales down, the size of transistors has been shrinking. The number of transistors on chip has

thus increased to improve the performance of circuits. The supply voltage, being one of the critical parameters, has also been reduced accordingly in order to maintain the characteristics of an MOS device. Therefore in order to maintain the transistor switching speed, the threshold voltage is also scaled down at the same rate as the supply voltage. As a result, leakage currents increase dramatically with each technology generation [2,6]. As the leakage current increases faster, it will become more and more proportional to the total power dissipation.

$$P_{leak} = I_{leak} * V_{dd} \dots\dots\dots\dots\dots\dots\dots\dots\dots (1)$$

Designers need to develop new low power techniques to reduce total leakage in nanoscale circuits, especially for chips that are used in power constrained portable systems. The leakage current consists of reverse bias diode currents and sub threshold current. The former is due to the stored charge between the drain and bulk of active transistors while the later is due to the carrier diffusion between the source and drain of the off transistors. The sub threshold current is given as:

$$I_{ds} = \mu_o \, C_{ox} \, \frac{w}{L} (m-1)(V_t)^2 \, e^{(V_{gs} - V_{th})/mVt} * (1 - e^{-V_{ds}/V_t})$$
$$\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots (2)$$

Where,
$$m = 1 + \frac{Cdm}{Cox} - 1 + 3\frac{tox}{Wdm} \dots\dots\dots\dots\dots\dots(3)$$

V_{th} = The threshold voltage
V_t = The thermal voltage
Cox = Gate oxide capacitance
μ_0 = Zero bias mobility
m = The sub threshold swing coefficient (also called body effect coefficient)
W_{dm}= The maximum depletion layer width
t_{ox} = The gate oxide thickness
C_{dm} = The capacitance of the depletion layer

In order to facilitate voltage scaling without affecting the performance, threshold voltage has to be reduced. This also leads to better noise margins and helps to avoid the hot carrier effects in short channel devices. Scaling down of threshold voltage results in exponential increase of the sub threshold leakage current. So, before going to in nanometer regime we need some techniques applied for CMOS logic to minimize the leakage power. Stacking is such technique used for minimize the leakage power.

SLEEPY STACK
The sleepy stack approach combines the sleep and stack approaches. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to

one of the divided transistors. Figure 4 shows its structure.

During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so

delay is decreased during active mode. However, area penalty is a significant matter for this approach since every

transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals.
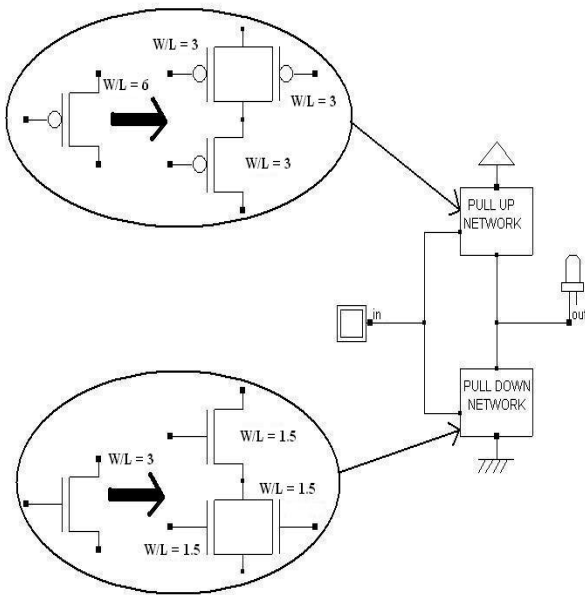

Fig 3 :- STACK METHOD

In conventional cmos inverter if input is given low as compared to threshold voltage, then at the same time pmos turns on and nmos turns off. And if input is given high at the gate terminal as compared to threshold voltage, then at the same time pmos turns off and nmos turns on.

Fig 2 :- SLEEPY STACK

STACK APPROACH

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [7]. Figure 3 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in subthreshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach.
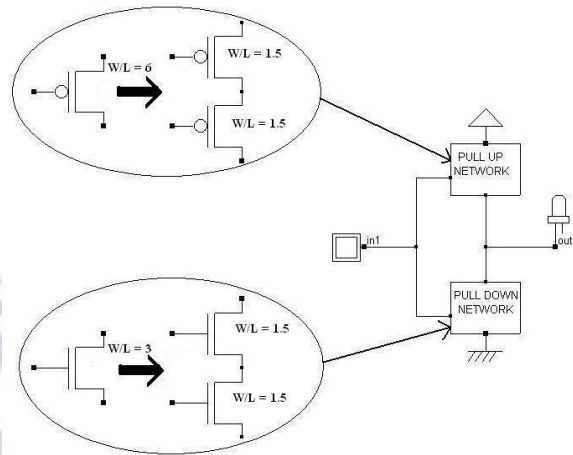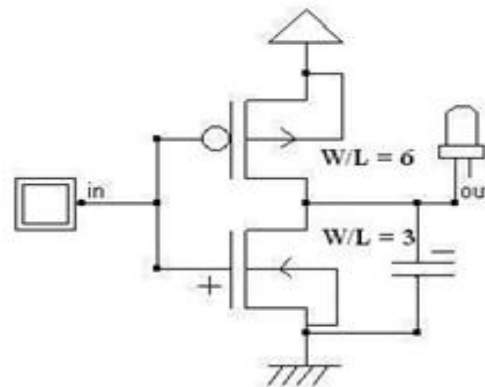

Fig :-4

Conventional CMOS

In this case there are three types of power dissipation that take place :-

1. Static power dissipation
2. Dynamic
3. Short circuit power

Static power dissipation are take place due to the leakage current and leakage current occur due to the off transistor because some minutely current are flow in off transistor whether is Pmos or Nmos.

Expression for leakage power :-

$$P = V_{dd} * I_{leakage}$$

Dynamic power dissipation takes place due to the charging and discharging of capacitor .

$$P = ACV^2F$$

P is the power consumed, A is the activity factor, i.e., the fraction of the circuit that is switching, C is the switched capacitance, V is the supply voltage, and F is the clock frequency.

In forced pmos inverter if input is given low as compared to threshold voltage., then at the same time pmos turns on and nmos turns off and if input is given high at the gate terminal as compared to threshold voltage, then at the same time pmos turns off and nmos turn on. Here the addition of two pmos transistors increases the delay in the flow of the current which ultimately decreases the leakage power in the circuit.
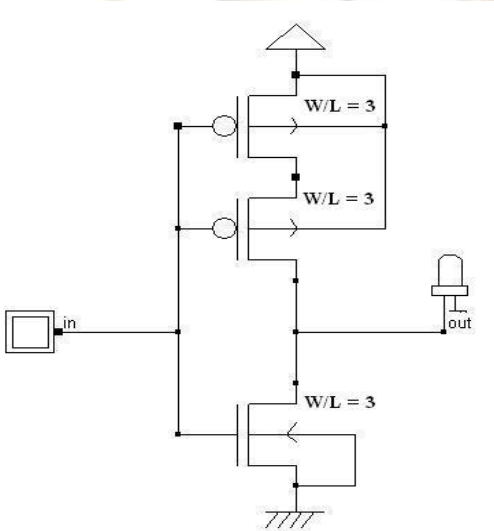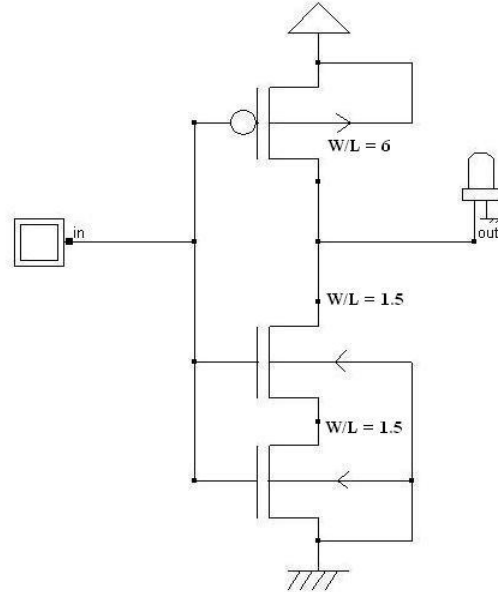
Fig 5 :- Forced P-MOS Transistor Inverter

In forced n-mos inverter if input is given low as compared to threshold voltage., then at the same time p-mos turns on and n-mos turns off and if input is given high at the gate terminal as compared to threshold voltage, then at the same time p-mos turns off and n-mos turn on.
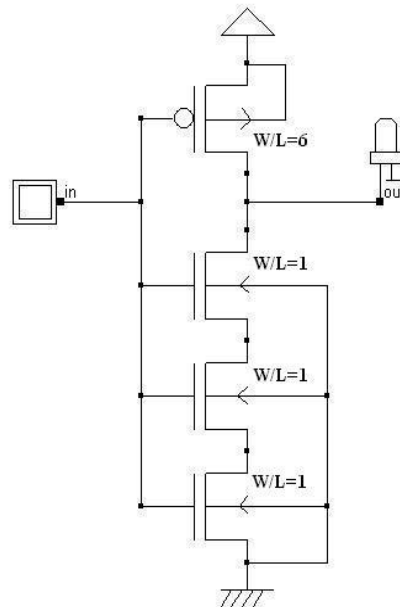Here, the two n-mos transistors which increases the delay in the flow of the current which ultimately decreases the leakage power in the circuit.

In forced 2- nmos inverter if input is given low as compared to threshold voltage., then at the same time pmos turns on and nmos turns off and if input is given high at the gate terminal as compared to threshold voltage, then at the same time pmos turns off and nmos

turn on. Here the addition of three nmos transistors

Fig 6 :- Forced N-MOS Transistor Inverter

increases the delay in the flow of the current which ultimately decreases the leakage power in the circuit.
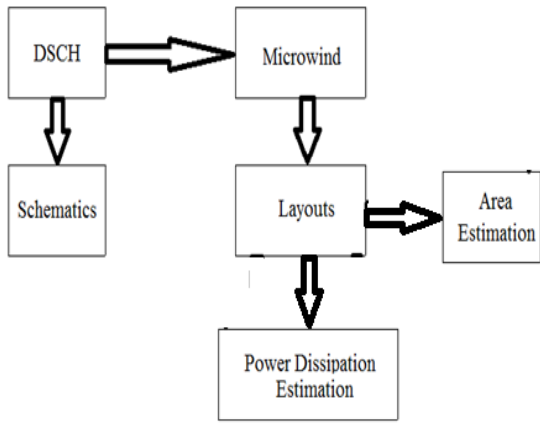**Fig 7 :- Forced 2- NMOS Transistor Inverter**

III. METHODOLOGY

We describe the experimental method. First, we describe how to make a schematic and create a layout by using the tools. Secondly, we describe how to obtain the results in term of power dissipation and layout area.

Experimental Methodology

Two type of window are involved in this tool. Schematic called DSCH and MICROWIND where layouts are design. Schematic and layout are design for all type of approach. Schematic are used for to make a different type of digital and analogue circuit and all the parameter are estimated with the help of microwind

window where the layout are design .These parameter are power dissipation and layout area at different technology of all considering approach.

Experiments include all the techniques namely are Conventional CMOS inverter, force NMOS transistor inverter, Forced PMOS transistor CMOS transistors, and Forced 2-NMOS CMOS inverter approaches. In addition, we consider a base case and the newly proposed novel approaches named "sleepy stack keeper". Schematics are designed for all considered techniques using schematics editor i.e. DSCH Window in MICOWIND software tool targeting TSMC are used to obtain net lists of the circuits and the net lists are used to simulating purpose. Schematics are created based on TSMC process parameters. Net lists of the circuits for different techniques are extracted from the schematics.

Fig :- The Supply voltages used by the Technologies

IV.SIMULATION RESULTS

We estimates only the power dissipation and Layout area for design approaches i.e. they are Conventional NMOS inverter, force NMOS transistor inverter, Forced PMOS transistor CMOS transistors, and Forced 2-NMOS CMOS inverter approaches . The simulations table for Power Dissipation and Layout Area is shown below in

Simulation results for power dissipation:

Techniques	45nm	65nm	90nm	120nm
Conventional CMOS	0.075μw	0.421 μw	1.582 μw	2.843 μw
Forced NMOS transistor inverter,	0.064 μw	0.342 μw	1.248 μw	2.439 μw
Forced PMOS transistor CMOS transistors	0.058 μw	0.312 μw	1.196 μw	2.387 μw
Forced 2-NMOS CMOS inverter	0.046 μw	0.258 μw	1.091 μw	2.179 μw
Stack	0.043 μw	0.198 μw	0.962 μw	1.39 μw
Sleepy stack keeper	0.034 μw	0.187 μw	0.613 μw	1.008 μw

Power Dissipation (μw) in Among Various Approaches

We are showing the simulations results of circuit with four different technology at a given standard power supply generations for all above discussed i.e. Conventional NMOS inverter, force NMOS transistor inverter, Forced PMOS transistor CMOS transistors, and Forced 2-NMOS CMOS inverter approaches with newly proposed approaches.
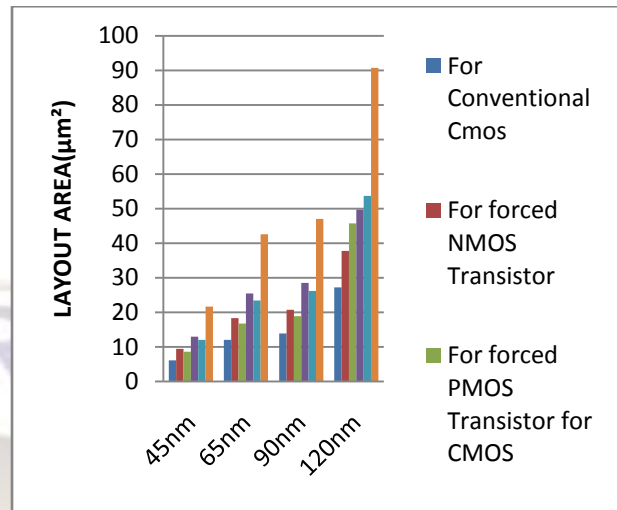
Simulation results for Layout Area:

Techniques	45nm	65nm	90nm	120nm
Conventional CMOS	6.3 μm²	12.0 μm²	13.9 μm²	27.2 μm²
force NMOS transistor inverter,	8.9 μm²	18.3 μm²	20.7 μm²	37.8 μm²
Technology	**45nm**	**65nm**	**90nm**	**120nm**
V_{dd}	**0.40v**	**0.70v**	**1.20v**	**1.20v**
Forced PMOS transistor CMOS transistors	8.1 μm²	16.8 μm²	18.9 μm²	45.7 μm²

Forced 2-NMOS CMOS inverter	12.8 µm²	25.5µm²	28.5 µm²	49.7µm²
Stack	11.8 µm²	23.5µm²	26.2µm²	53.7µm²
Sleepy stack keeper	21.2 µm²	23.5µm²	47.0µm²	97.7µm²

Layout Area (µm²) in Among Various Approaches

We are showing the simulations results of circuit with six different technologies at a given standard power supply generations for all above discussed six techniques i.e. The above the table after the simulation latest approach having the Layout area penalty as compare to all considering approach. The Layout Area is decreasing according to decreasing the feature size technologies. We explain from the graph given below .In this graph first we are showing Layout area of all considering approach.

Power Dissipation Chart for All Technology

Layout Area Chart for All Technique
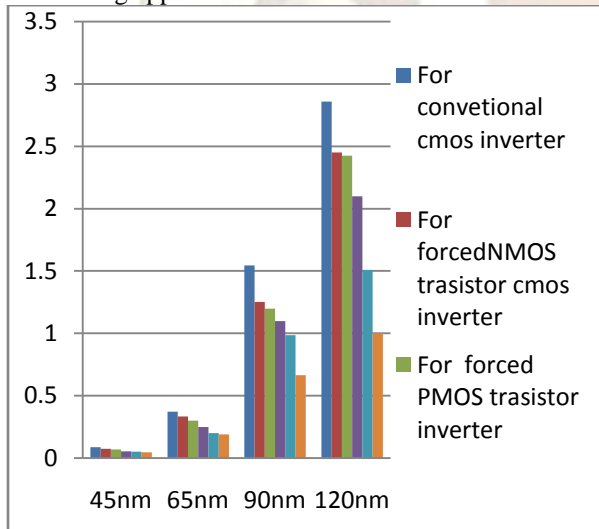
V. CONCLUSION

Scaling down of device dimensions, supply voltage and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. We have presented an efficient design methodology for reducing the leakage power in CMOS inverter circuit. Implications of technology scaling on the choice of techniques to mitigate total leakage are examined.

The proposed technique in the thesis is "SLEEPY STACK KEEPER" and comparing the power consumption with other existing techniques. The proposed technique is more effective in reducing power consumption. The result is simulated with MICROWIND software and compare at different technology 45nm, 65nm, 90nm and 120nm.

VI. FUTURE SCOPE

The advent of a mobile computing era has become a major motivation for low power design because the operation time of a mobile device is heavily restricted by its battery life. The growing complexity of mobile devices, such as a cell phone with a digital camera or a personal digital assistant (PDA) with global positioning system (GPS), makes the power problem more challenging.

The proposed technique can be implemented in low power VLSI circuit and save the power consumption of the chip which leads to increase battery life.

VII. REFRENCES

[1] Se Hun Kim, Vincent J. Mooney III   "*Sleepy Keeper: a New Approach to Low-leakage Power VLSI Design*",IEEE VLSI., 10.1109/VLSISOC.2006.313263.

[2] Jun Cheol Park and Vincent J. Mooney III*, Senior Member, IEEE,* "Sleepy Stack Leakage Reduction", Volume: 14 , Issue: 11 , 2006 , Page(s): 1250 – 1263.

[3] *"International Technology Roadmap for Semiconductors,"* Semiconductor Industry Association, 2005. [Online]. Available: http://public.itrs.net

[4] N. Kim, T. Austin, D. Bauw, T. Mudge, K. Flautner, J. Hu, M. Irwin, M. Kandemir, and V. Narayanan, "Leakage current: Moore's Law meets static power," *IEEE Computer.*, vol. 36, no. 12, pp. 68–75, Dec. 2003.

[5] G. D. Micheli*, Synthesis and Optimization of Digital Circuits*. New York: McGraw-Hill, 1994.

[6] Johnson, M.C., D. Somasekhar, L.Y. Chiou and K. Roy, 2002. Leakage control with efficient use of transistor stacks in single threshold CMOS. IEEE TVLSI, 10: pp 15.

[7] Kim, N.S. *et al.*, 2003. Leakage current: Moore's law meets static power. IEEE Computer,36: pp 6875.

[8] Kuroda, T. and T. Sakurai 1996. Threshold voltage control schemes through substrate bias for lowpower high speed CMOS LSI design. J. VLSI Signal Proc. Syst., 13: pp 191201.

[9] Narendra, S., V.D.S. Broker, D. Antoniadis and A. Chandrakasan, 2001. Scaling of stack effect and its application for leakage reduction. Proceeding of the International Symposium Low Power Electron. Des., pp195200.

[10] Powell, M.D., S.H. Yang, B. Falsafi, K. Roy and T.N. Vijaykumar, 2000. GatedVdd: A circuit technique to reduce leakage in deep submicron cache memories. Proc. Of ISLPED, pp9095.

[11] Roy, K., S. Mukhopadhaya and H. Mahmoodi Meimand, 2003. Leakage current mechanisms and leakage reduction techniques in deep submicrometer CMOS circuits. Proc. IEEE, 91: pp 305327.

[12] S. Mutoh et al., "1-V Power Supply High-speed Digital Circuit Technology with Multi-threshold-Voltage CMOS," IEEE Journal of Solis-State Circuits, Vol. 30, No. 8, pp. 847-854, August 1995.