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VLSI Implementation of Densely Packed Decimal Converter to and from Binary Coded Decimal using Reversible Logic Gates

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***Abstract*— The Binary Coded Decimal encoding has always dominated decimal arithmetic algorithms and their hardware implementation by virtue is ease of conversion between machine- and human-readable formats, as well as a more precise machine-format representation of decimal quantities. As compared to typical binary formats, BCD's principal drawbacks are a small increase in the complexity of the circuits needed to implement basic mathematical operations and less efficient usage of storage facilities. Due to importance such pro's and con's of BCD it is needed to convert them to decimal format and floating point decimal play important role present day arithmetic. This paper uses densely packed decimal encoding to store significant part of the decimal floating point number. And present day VLSI, low power is the major consideration for the Design. The reversible logic gates are the main source for designing the low power CMOS circuits, as it is not possible to realize quantum computing without them where the quantum computing the speed is the main parameter. This paper derives the reversible implementation of DPD converter to and from conventional BCD format. This conversion is implemented to the adder circuits where they follow BCD code for the arithmetic addition such that converting them to DPD (Densely packed Decimal) will result in the better storage capacity by decreasing the less density of storage devices for faster access to memory. The implementation of the adder circuit is carried in low power technique by using reversible logic gates in order to go for the complete low power design of the implementation.**

***Keywords*—** BCD, DPD, Reversible logic gates, VHDL.

I. INTRODUCTION

Several reversible gates have been proposed over the years, e.g., the Toffoli gate, the Fredkin gate etc. The truth tables for three input and three output Toffoli and Fredkin gates are shown in Tables I and II, respectively. In a Toffoli gate, all inputs from 1 to $(n - 1)$ are passed as output. The nth output is controlled by 1 to $(n - 1)$ inputs. When all the inputs from 1 to $(n - 1)$ are 1s, the nth input is inverted and passed as output; otherwise, the original signal is passed. The Toffoli gate shown in Fig. 1 has three inputs and three outputs. The inputs "*a*" and "*b*" are passed as the first and second output, respectively. The third output is controlled by *a* and *b* to invert "*c*". The Fredkin

gate is shown in Fig. 2. Here, the input *a* is passed as the first output. Inputs *b* and *c* are swapped to get the second and third
outputs, which are controlled by *a*. Thus, two inputs can be swapped by controlling the swap using another input in the Fredkin Gate. A new three-input and three-output reversible-logic gate *R* [Fig. 3(a)]. The truth table of the gate is shown in Table III. Arithmetic circuits such as Adders, Subtractors, Multipliers and Dividers are the essential blocks of a Computing system. Dedicated Adder/Subtractor circuits are required in a number of Digital Signal Processing applications. Several designs for binary Adders and Subtractors are investigated based on Reversible logic. Minimization of the number of Reversible gates, Quantum cost and garbage inputs/outputs are the focus of research in Reversible logic.

TABLE I

TRUTH TABLE OF THE TOFFOLI GATE

A	B	C		X	Y	Z
0	0	0		0	0	0
0	0	1		0	0	1
0	1	0		0	1	0
0	1	1		0	1	1
1	0	0		1	0	0
1	0	1		1	0	1
1	1	0		1	1	1
1	1	1		1	1	0

TABLE II

TRUTH TABLE OF THE FREDKIN GATE

A	B	C		X	Y	Z
0	0	0		0	0	0
0	0	1		0	1	0
0	1	0		0	0	1
0	1	1		0	1	1
1	0	0		1	0	0
1	0	1		1	0	1
1	1	0		1	1	0
1	1	1		1	1	1

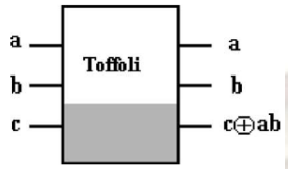

Fig. 1. Toffoli gate.

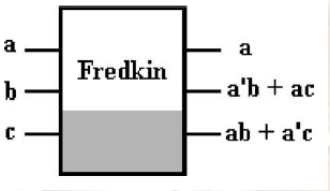

Fig. 2. Fredkin gate.

The AND function is obtained by connecting the input *c* to 0, the output is obtained at the terminal *n*, as shown in Fig. 3(c). The implementation of a NAND gate is shown in Fig. 3(d). An OR gate is realized by connecting two new reversible gates, as shown in the Fig. 3(e). From the truth table, it can be verified that the input pattern corresponding to a particular output pattern can be uniquely determined. The new gate can be used both to invert and duplicate a signal. The signal duplication function can be obtained by setting the input *b* to 0, as shown in Fig. 3(b). The EXOR function is available at the output "*l*" of the new gate.

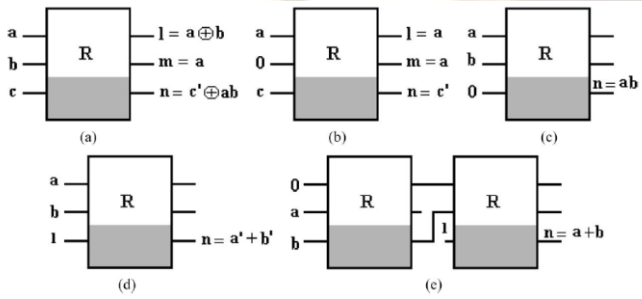

Fig. 3. (a) New reversible-logic gate *R*. (b) Signal duplication. (c) AND gate. (d) NAND gate. (e) OR gate.

Table III

TRUTH TABLE OF THE NEW REVERSIBLE-LOGIC GATE

A	B	C		X	Y	Z
0	0	0		0	0	1
0	0	1		0	0	0
0	1	0		1	0	1
0	1	1		1	0	0
1	0	0		1	1	1
1	0	1		1	1	0
1	1	0		0	1	0
1	1	1		0	1	1

II. CONSERVATIVE REVERSIBLE LOGIC

A gate is reversible if the gate's inputs and outputs have a one-to-one correspondence, i.e. there is a distinct output assignment for each distinct input. Therefore, a reversible gate's inputs can be uniquely determined from its outputs. A ramification of this definition is that reversible logic gates must have an equal number of inputs and outputs. If logic gates are classified according to the number of inputs and outputs, a g ate with m inputs and n outputs is (m,n) a logic gate, where reversible gates must have m=n . Furthermore, a (n,n) reversible gate's output vector is a permutation of the numbers 0 to 2^n-1 .

A gate is balanced if its output equals one for exactly one-half of its inputs. If a gate is not balanced, it is said to be unbalanced. Reversible gates are balanced. The only nontrivial reversible logic gate in classical digital logic is the (1,1) reversible gate, i.e. the inverter. The gate not possessing the reversibility characteristic is said to be irreversible. All multiple-input single output logic gates in classical digital logic are irreversible, e.g. AND, OR, XOR, etc. circuit without constants on inputs which includes only reversible gates realizes on all outputs only balanced functions, therefore it can realize non-balanced functions only with garbage outputs. An additional constraint of reversible logic is that the fanout of every signal, including primary inputs, must be one. In the classical paper [3], Fredkin and Toffoli formulate the synthesis problem for reversible logic. Classical logic synthesis methods cannot be directly applied to design reversible logic circuits, and reversible logic specific synthesis methods do not yet exist. Currently, logic functions constructed with reversible logic gates are designed in an ad hoc fashion.

By definition, all reversible gates have an inverse, i.e. a gate that "undoes" the logic function. A logic gate is said to be self-invertible if the gate is equal to its own inverse. In some works, the terms symmetric or dual are used, and the ambiguous term invertible is also common. For

example, a gate is self-invertible if, for every input , , or, equivalently, . Obviously, the classic digital inverter is self-invertible. A gate is zero-preserving if the all zeros input produces all zeros outputs. A gate is one-preserving if the all ones input produces all ones outputs. A gate is said to be controlled if one or more of its inputs causes a function to be performed, conditionally, on its other inputs. The inputs that determine whether the action is taken or not are called the gate's control signals.

A gate is conservative if the Hamming weight (number of logical ones) of its input equals the Hamming weight of its output. A conservative reversible gate is a gate that is both conservative and reversible simultaneously. A consequence of a gate's reversibility and conservability is that conservative reversible gates are zero preserving and ones-preserving. A conservative reversible logic gate effectively permutes its inputs to form its outputs. Conservative gates are not necessarily reversible as several inputs with equal Hamming weights can be mapped to a single output of the same Hamming weight. For example, consider the two-input, two-output logic gate where one output is the logical AND of the inputs, and the other output is the logical OR of the inputs. This logic gate is conservative and irreversible. Magnetic bubble circuits initiated much research on conservative, but irreversible, logic.

III. DPD BLOCK

An improvement to the encoding which has the same advantages but is not limited to multiples of three digits was described by M.F. Cowlishaw called Densely Packed Decimal (DPD) encoding allows arbitrary-length decimal numbers to be coded e_ciently.Densely packed decimal (DPD) is a system of binary encoding for decimal digits. Like Chen-Ho encoding, DPD encoding classifies each decimal digit into one of two ranges, depending on the most significant bit of the binary form: "small" digits have values 0 through 7 (binary 0000–0111), and "large" digits, 8 through 9 (binary 1000–1001). Once it is known or has been indicated that a digit is small, three more bits are still required to specify the value. If a large value has been indicated, only one bit is required to distinguish between the values 8 or 9. When encoding, the most significant bit of each of the three digits to be encoded select one of 8 coding patterns for the remaining bits.

The DPD encoding (BCD to DPD) and the decoding (DPD to BCD)mechanism must be very fast as it is applied for every decimal number in every calculation. Moreover, DPD encoding can also be used in data communication which can help in reducing the number of bits to be transmitted or received. This paper includes the work for a pipelined implementation of a DPD encoder and decoder, its simulation on hardware using VHDL. Densely Packed Decimal Encoding proposed by M. F. Cowlishaw is an improvement over Chen-Ho encoding. It uses the coding scheme equivalent to the Chen-Ho but instead of using Hu_man-code it uses a fresh arrangement of bits that gives it further advantages over the Chen-Ho scheme. The advantages can be listed as follows:

1. The encoding of decimal digits, unlike Chen-Ho encoding, does not require the number of decimal digits to be a multiple of three. Thus, it can encode arbitrary number of decimal digits. One or two decimal digits are compressed into the optimal four or seven bits respectively.

2. The encoded decimal numbers can be expanded into a longer _eld simply by padding with zero bits; re-encoding is not necessary. While Chen-Ho encoding requires a re-encoding instead of simple padding if an encoded two digits is expanded into three digit _eld.

3. When numbers in the range 0 through 79 are encoded by this scheme they have the same right- aligned encoding as in BCD. While in Chen-Ho encoding only the numbers 0 through 7 remains same as in BCD.

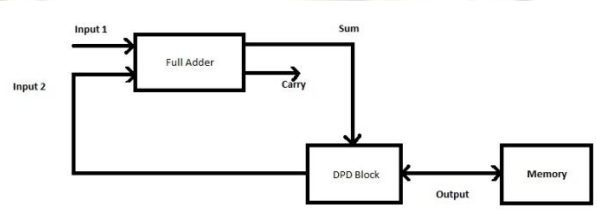

Fig.4 Simple DPD Block Diagram

The DPD converter consists of two blocks namely

A. Compression Block:

In the compression block there are two operations that is the given number is converted from binary to BCD and from BCD to DPD. In this example we consider a 12bit binary number which is converted to 10 bit DPD by which the memory storage can be increased.

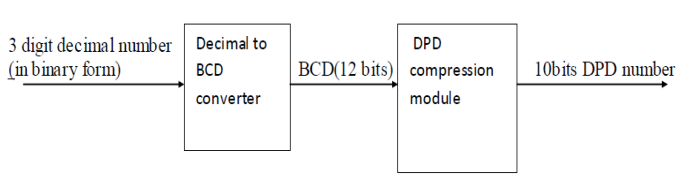

Fig.5 Compression Block Diagram

B. Expansion Block:

In this Expansion block again there are two operations that is the stored DPD format is converted to BCD and the

BCD then converted to Binary which can be used for multiple operations.

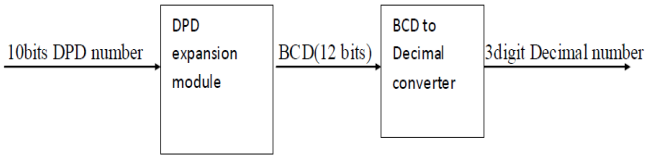

Fig.6 Expansion Block Diagram

The both modules encoding and decoding or expansion and compression are included in the DPD converter which saves the memory and increases the efficiency of the system with low power consumption.

TABLE IV
TABLE FOR BCD AND DPD ENCODING

Decimal	BCD	Densely Packed
005	0000 0000 0101	000 000 0101
009	0000 0000 1001	000 000 1001
055	0000 0101 0101	000 101 0101
099	0000 1001 1001	000 101 1111
555	0101 0101 0101	101 101 0101
999	1001 1001 1001	001 111 1111

C. Full Adder/Subtractor

Two tr gates and two fg gates are used to realize deign ii reversible full adder/subtractor unit is shown in figure 14. The three inputs are a, b and cin, the outputs are s/d and c/b. for ctrl value *zero* the circuit performs addition and subtraction for ctrl value *one*. The numbers of garbage inputs are 1 represented by logical *zero*. The garbage outputs are 3 represented by *g1* to *g3*. the quantum cost for the design is 14. a quantum cost advantage of 7 is obtained when compared to adder/subtractor design i. quantum cost advantage is due to the realization of arithmetic blocks (adder and subtractor) using two tr gates as against three numbers of 3*3 gates for design i.

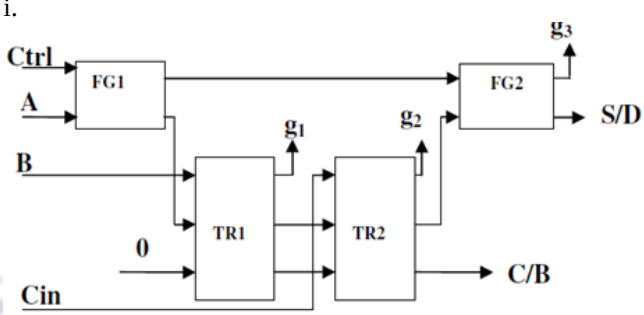

Fig.7 Reversible Full Adder/Subtracter

IV. RESULTS

The following figure is the RTL Schematic diagram of BCD to DPD circuit which consists of 12 inputs and 10 outputs. The 12 bit input is converted to 10 bit output thus reducing the memory and power consumption. The main scope finds it application in the memory capacity where an extra 2 bits can be can be accomidated in place where it uses the BCD codes. As par it is considred the design cost increases with increase in memory size, this overhead can be over ruled by this DPD codes.

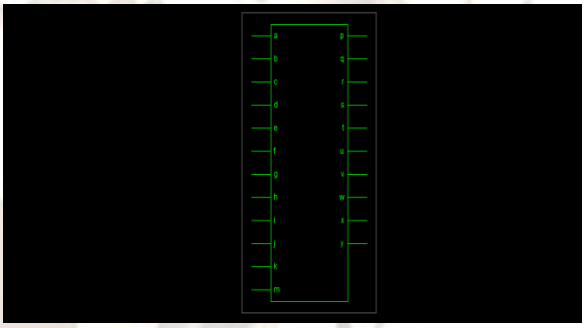

Fig. 8 RTL Schematic diagram for BCD to DPD circuit

The following figure is the RTL Schematic diagram of DPD to BCD circuit which consists of 10 inputs and 12 outputs. The 10 bit input is converted to 12 bit output which can be used for further operation.

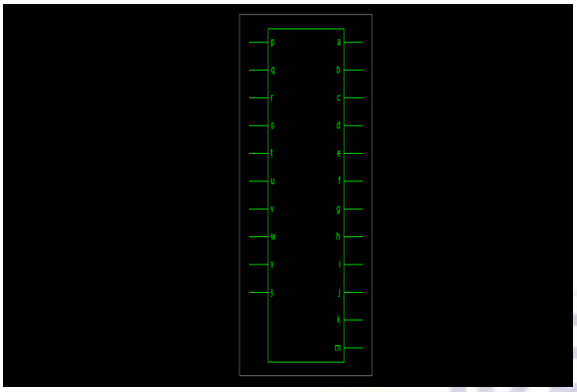

Fig. 9 RTL Schematic diagram for DPD to BCD circuit

According to the table IV which is BCD to DPD encoding in which different inputs are provided and accordingly we obtained the outputs that is the Densely Packed Decimal encoding.

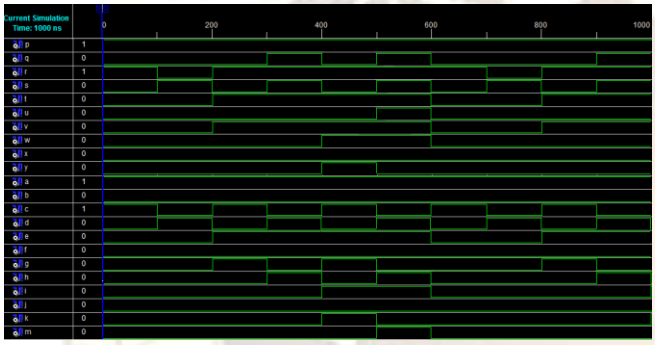

Fig.10 Output of BCD to DPD circuit

Similarly BCD outputs are obtained from DPD inputs. The outputs are shown below.

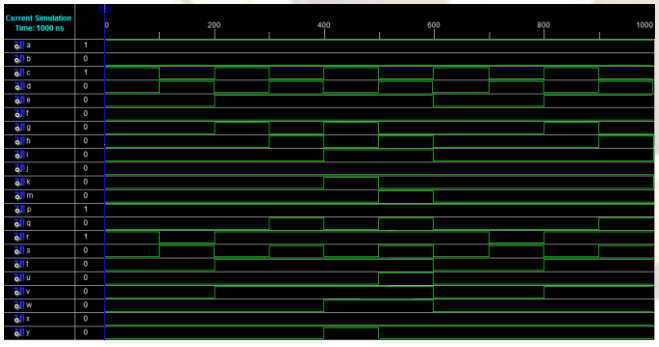

Fig.11 Output of DPD to BCD circuit

CONCLUSION

Thus design of a BCD to and from DPD converter using reversible logic gates for efficient use of memory and low power consumption using VHDL coding in Xilinx and simulated using modelsim. Such a design can be optimized in place of normal BCD converters which are having area and performance overhead. The implementation of these converters using Reversible logic achieves the low power designs for modern day VLSI portable applications.

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