Rajeev Kumar, Mandeep Singh Saini / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 3, May-Jun 2012, pp. 179-182

Design of High Speed Variable Width Integer Multiplier

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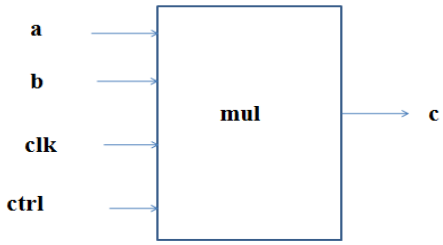
Introduction

In mathematical calculation multiplication is done using multiplier. Various types of multipliers are designed using different techniques. Here we present the design of a multiplier in which we can multiply two numbers with different size.
So there is no need to design various multipliers to perform multiplication. One multiplier is sufficient. Also this multiplier provides the high speed during multiplication.

Experimental Details

In order to design the multiplier containing different bit width encoding is done first. After that architecture of the multiplier is designed according to the specifications. Then these specifications are converted into RTL (Register Transfer Level).So RTL coding is done in Verilog HDL.
Functionality is checked using simulation on Modelsim 6.4a.After that gate level netlist is generated using Xilinx ISE 9.2i.
The block diagram of the multiplier is shown in the following figure.



Architecture Design of Variable Width Multiplier

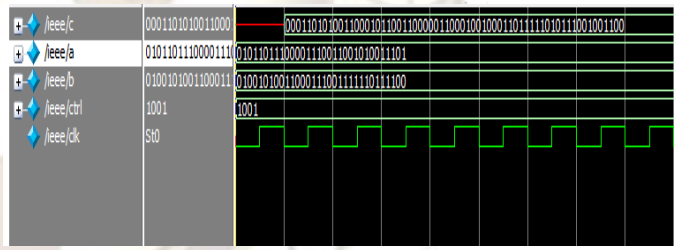
Here a, b is the variable input, clk is the negative edge clock, ctrl is the control input. To decide the bit width encoding is done using four bits of the Binary Code.
All the bit width is shown in the following table.

Operation	Code
4x4	0000
8x4	0001
8x8	0010
16x4	0011
16x8	0100
16x16	0101
32x4	0110
32x8	0111
32x16	1000
32x32	1001

As shown in the following table two 4 bit numbers are multiplied according to first row. In second row first number contains 8 bit and second number contains four bit.
Only one multiplier is required to perform all the calculations.

Experimental Results:

Simulation Result



Synthesis Report

Device Utilization Report

To generate the gate level netlist synthesis is done on Xilinx ISE 9.2i.For that purpose Virtex 4 FPGA with **4vlx15ff668** speed grade -12 is used.

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=========================================================================

Device utilization summary:
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Selected Device : 4vlx15ff668-12

 Number of Slices:                      195  out of   6144     3%
 Number of Slice Flip Flops:             32  out of  12288     0%
 Number of 4 input LUTs:                359  out of  12288     2%
 Number of IOs:                         133
 Number of bonded IOBs:                 133  out of    320    41%
    IOB Flip Flops:                      32
 Number of GCLKs:                        1  out of     32     3%
 Number of DSP48s:                      11  out of     32    34%

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Partition Resource Summary:
---------------------------
```

Slack Report

```
--------------------------------------------------------------------------------------------------------
 Constraint                                | Check  | Worst Case |  Best Case | Timing |   Timing
                                           |        |    Slack   | Achievable | Errors |    Score
--------------------------------------------------------------------------------------------------------
 Autotimespec constraint for clock net clk | SETUP  |         N/A|     0.862ns|     N/A|         0
 _BUFGP                                    | HOLD   |     0.383ns|            |       0|         0
--------------------------------------------------------------------------------------------------------


*************************
Generating Clock Report
*************************

+----------------------+--------------+------+------+------------+-------------+
|        Clock Net     |   Resource   |Locked|Fanout|Net Skew(ns)|Max Delay(ns)|
+----------------------+--------------+------+------+------------+-------------+
|          clk_BUFGP   |BUFGCTRL_X0Y15| No   |   64 |  0.188     |  1.999      |
+----------------------+--------------+------+------+------------+-------------+

* Net Skew is the difference between the minimum and maximum routing
only delays for the net. Note this is different from Clock Skew which
is reported in TRCE timing report. Clock Skew is the difference between
the minimum and maximum path delays which includes logic delays.


   The Delay Summary Report


The NUMBER OF SIGNALS NOT COMPLETELY ROUTED for this design is: 0

   The AVERAGE CONNECTION DELAY for this design is:        1.188
   The MAXIMUM PIN DELAY IS:                               3.270
   The AVERAGE CONNECTION DELAY on the 10 WORST NETS is:   2.959
```

Timing Report: Speed

```
Timing Summary:
---------------
Speed Grade: -12

   Minimum period: 0.845ns (Maximum Frequency: 1183.712MHz)
   Minimum input arrival time before clock: 10.996ns
   Maximum output required time after clock: 3.766ns
   Maximum combinational path delay: No path found

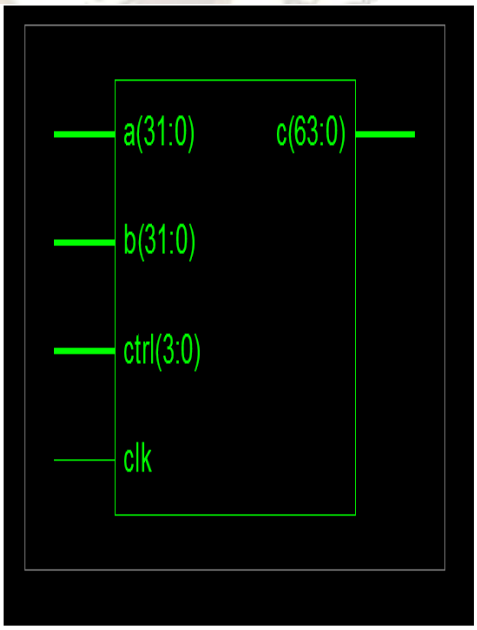
Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

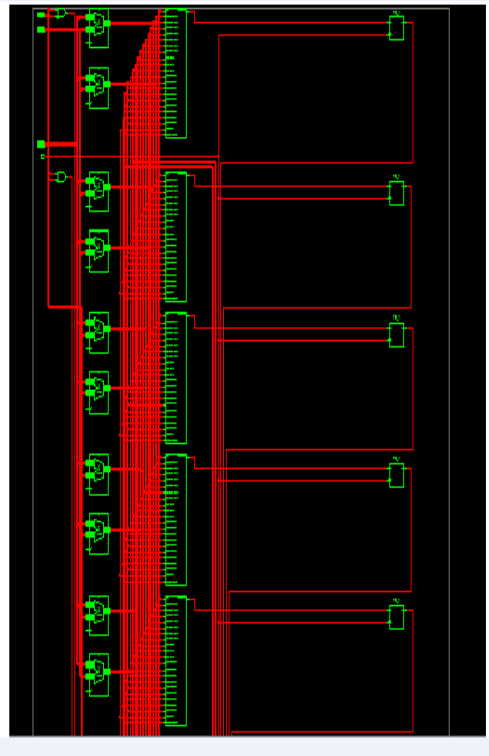
```
=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 115376192 / 128
-------------------------------------------------------------------------
Offset:              10.996ns (Levels of Logic = 6)
  Source:            b<1> (PAD)
  Destination:       c_26 (FF)
  Destination Clock: clk falling

  Data Path: b<1> to c_26
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             63   0.754   0.775  b_1_IBUF (Mmult_mult0000_a<0>_x_b<1>_mand)
     DSP48:B1->PCOUT47      1   3.523   0.000  Mmult_mult0002 (Mmult_mult0002_PCOUT_to_Mmult_mult00021_PCIN_47)
     DSP48:PCIN47->PCOUT47  1   1.890   0.000  Mmult_mult00021 (Mmult_mult00021_PCOUT_to_Mmult_mult00022_PCIN_47)
     DSP48:PCIN47->P10      1   1.816   0.496  Mmult_mult00022 (_mult0002<27>)
     LUT4:I2->O             1   0.147   0.496  c_27_mux000034_SW2 (N1451)
     LUT4:I2->O             1   0.147   0.266  c_27_mux000034 (c_27_mux0000_map12)
     FDS_1:S                    0.805          c_27
    ----------------------------------------
    Total                      10.996ns (9.082ns logic, 1.914ns route)
                                        (82.6% logic, 17.4% route)

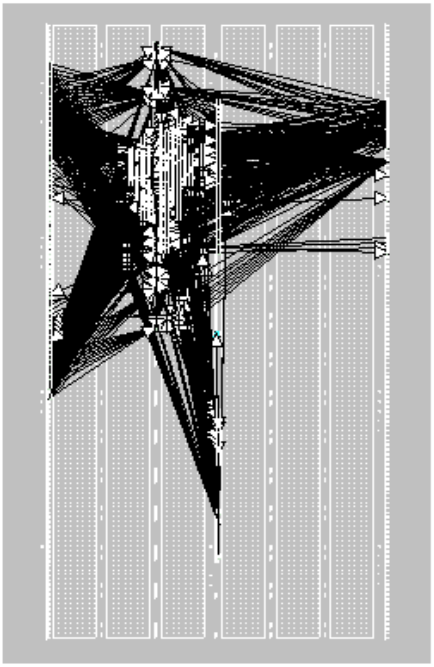
=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 64 / 64
-------------------------------------------------------------------------
```

RTL Schematic

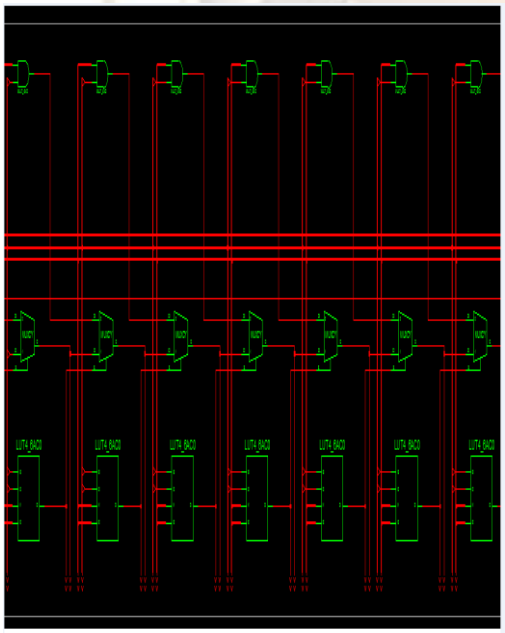




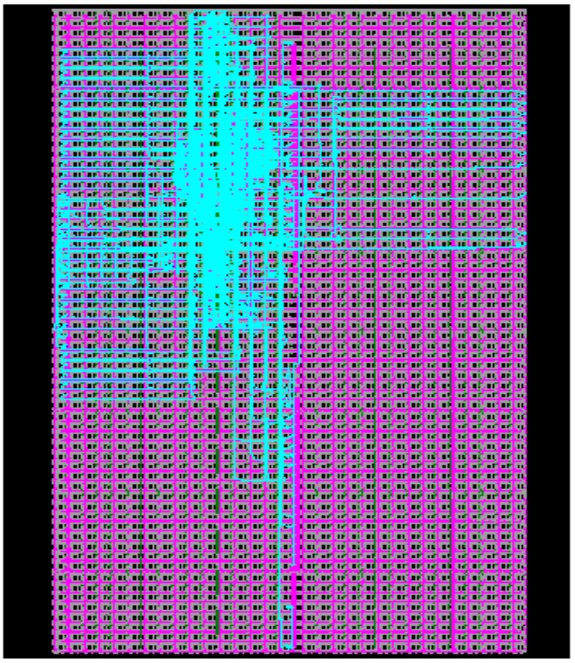
Technology Schematic



Chip Design



Chip Floor plan



Power Report

```
Power summary:                          I(mA)     P(mW)
---------------------------------------------------------------
Total estimated power consumption:                 251
                                  ---
                        Vccint 1.20V:       49       58
                        Vccaux 2.50V:       77      193
                        Vcco25 2.50V:        0        0
                                  ---
                             Clocks:        0        0
                             Inputs:        0        0
                              Logic:        0        0
                            Outputs:
                               Vcco25        0        0
                            Signals:        0        0
                                  ---
               Quiescent Vccint  1.20V:       49       58
               Quiescent Vccaux  2.50V:       77      193

Thermal summary:
---------------------------------------------------------------
   Estimated junction temperature:                 29C
                       Ambient temp:  25C
                          Case temp:  28C
                          Theta J-A:  14C/W
```

Final Report

Parameter	Value
Speed	1183.712 MHz
Gate Delay	10.996ns
Net Delay	9.082ns
Slack	0.383ns
Net Skew	0.188ns
Clock Fanout	64
Setup Time	10.996ns
Hold Time	3.766ns
Power Consumption	251mW
Gate Count	3,848
Additional JTAG Gate Count	6,384

Discussion

Here only one multiplier is required to perform variable size multiplication no separate multiplier is required .Hardware is develop using Xilinx ISE 9.2i.In future we can develop a variable bit multiplier to perform Floating Point Multiplication using IEEE 754 format. The proposed multiplier provides high speed during multiplication. In future we can design the multiplier for low power consumption. To increase speed further multiplier can be pipelined.

References

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