Rajeev Kumar, Mandeep Singh Saini / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 3, May-Jun 2012, pp. 174- 178

Design of 64 bit Integer Multiplier for Low Power Consumption

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Introduction

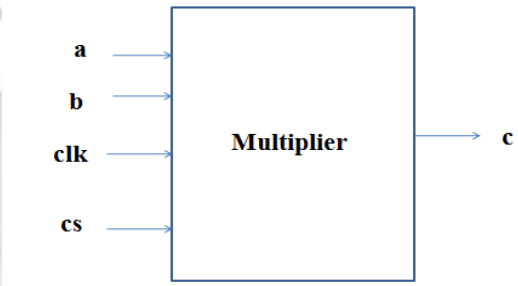
In mathematical calculations multiplication is an important operation. Multiplication is done using Multiplier. In scientific calculations large bit width are required. In the previous architectures 32 bit multipliers are designed using Hardware Description Languages. So as the bit width increases to perform long calculations, the requirement of hardware should be more. In the hardware each gate consumes power. So in this particular multiplier our aim is to reduce the power consumption of the multiplier chip. Here we present the design of a 64 bit Integer Multiplier that generates 128 bit output. This multiplier is designed using Verilog HDL.

Experimental Work

All the specifications are written first. Then they are converted in RTL using Verilog HDL.It contains two 64 bit inputs namely a and b and c is the 128 bit output. Here clk is the clock input which is taken as negative edge for fast triggering.

Here cs is the chip select signal. If cs is high then chip is disabled and no multiplication is done .On the other hand if cs signal is low then multiplication is done.

Functionality is verified using simulation on Active HDL 7.2.

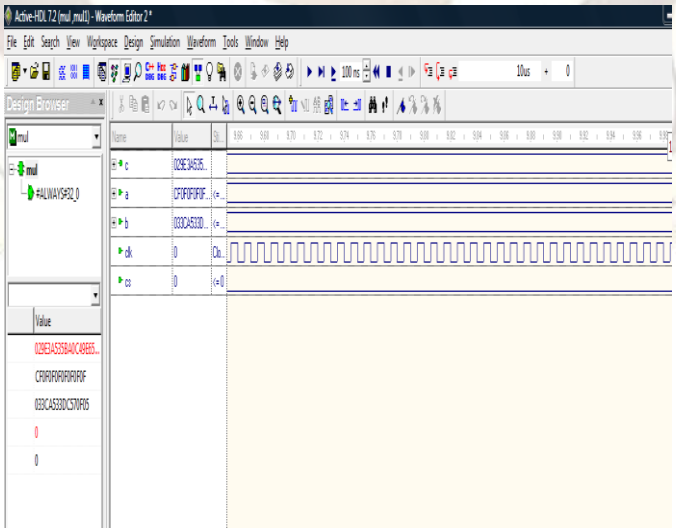


Architecture Design for 64 bit Multiplier

After simulation is over the gate level netlist is generated using Xilinx ISE 9.2i. After synthesis the design is technology specific. Finally all the necessary parameters obtained from the synthesis are given in the table.

Experimental Results

Simulation Result



Device Utilization Report

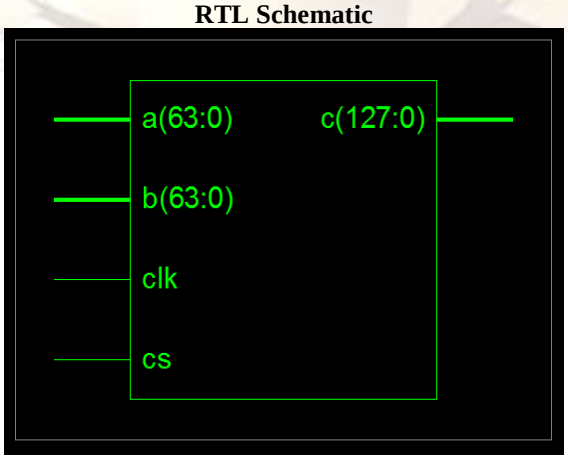
```
Device utilization summary:
---------------------------

Selected Device : 2s200fg456-6

 Number of Slices:                     2183  out of   2352    92%
 Number of 4 input LUTs:               4348  out of   4704    92%
 Number of IOs:                         258
 Number of bonded IOBs:                 258  out of    284    90%
    IOB Flip Flops:                     192
 Number of GCLKs:                        1  out of      4    25%
```

Delay Report

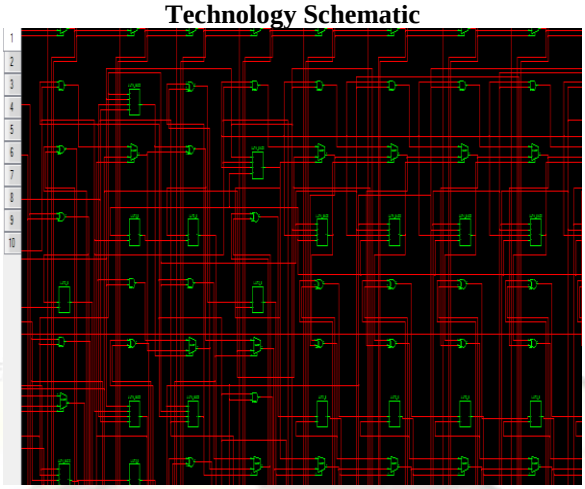
```
Timing Summary:
---------------
Speed Grade: -6

   Minimum period: No path found
   Minimum input arrival time before clock: 26.244ns
   Maximum output required time after clock: 12.381ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

```
Data Path: Mtrien_c to c<99>
                           Gate     Net
  Cell:in->out     fanout   Delay   Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   FD_1:C->Q            1   1.085   1.035  Mtrien_c (Mtrien_c)
   BUF:I->O            65   0.549   4.905  Mtrien_c_1 (Mtrien_c_1)
   OBUFT:T->O               4.807          c_9_OBUFT (c<9>)
  ----------------------------------------
  Total                    12.381ns (6.441ns logic, 5.940ns route)
                                    (52.0% logic, 48.0% route)

=========================================================================
CPU : 49.67 / 49.97 s | Elapsed : 49.00 / 50.00 s
```

RTL Schematic



Technology Schematic



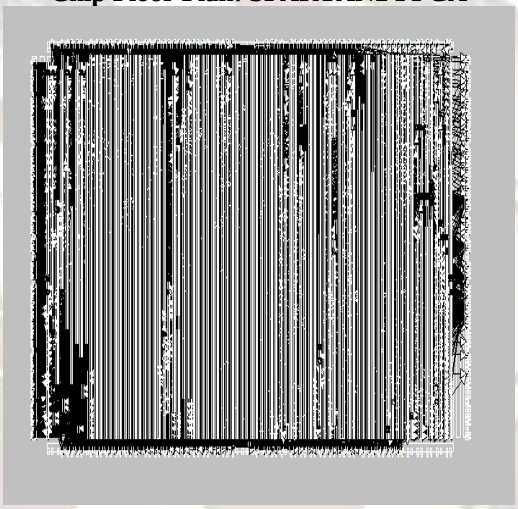
Power Report

```
Copyright (c) 1995-2007 Xilinx, Inc.  All rights reserved.
Design:       alu.ncd
Preferences:  alu.pcf
Part:         2s200fg456-6
Data version: PRELIMINARY,v1.0,07-31-02

Power summary:                          I(mA)     P(mW)
----------------------------------------------------------------------
Total estimated power consumption:                   7
                                        ---
                      Vccint 2.50V:       0         0
                      Vcco33 3.30V:       2         7
                                        ---
                           Clocks:        0         0
                           Inputs:        0         0
                            Logic:        0         0
                          Outputs:
                             Vcco33       0         0
                          Signals:        0         0
                                        ---
            Quiescent Vcco33  3.30V:      2         7

Thermal summary:
----------------------------------------------------------------------
   Estimated junction temperature:                  25C
                  Ambient temp:  25C
                     Case temp:  25C
                Theta J-A range:  27 -  22C/W
```

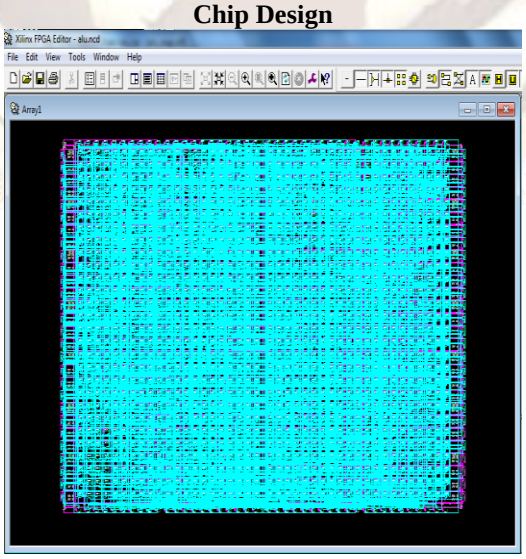
Post Layout Simulation Report

```
[Copyright]     Copyright 2000, Xilinx Inc., All rights reserved
|
|*****************************************************************************
|                       Component Spartan-II
|*****************************************************************************
|
[Component]     Spartan2
[Manufacturer]  Xilinx Inc.
[Package]
| For Package Type fg456
| variable       typ       min       max
R_pkg           161.00m   117.00m   205.00m
L_pkg           4.1500nH  1.9000nH  6.4000nH
C_pkg           1.1500pF  0.7000pF  1.6000pF
|
|*****************************************************************************
'
```

Chip Floor Plan: SPARTAN2 FPGA



Chip Design



Experimental Results & Discussion

Gate Delay	12.381ns
Net Delay	6.441ns
Clock Fanout	161
Power Consumption	7mW
Gate Count	56,644
Additional JTAG Gate Count	12,384
Setup Time	26.244ns
Hold Time	12.381ns
Technology	0.18um CMOS
Bonded IO	258

Finally the synthesis is done on SPARTAN2 FPGA using package 2s200fg456 with speed grade -6. This chip provides the low power consumption that is the prime requirement of today technology. In future the multiplier can be designed for high speed with minimum hardware.

Comparison

Parameters	**SPARTAN2**	**SPARTAN2e**
Gate Delay	12.381ns	26.851ns
Net Delay	6.441ns	18.151ns
Clock Fanout	161	161
Power Consumption	7mW	34mW
Gate Count	56,644	56,644
Additional JTAG Gate Count	12,384	12,384
Setup Time	26.244ns	26.851ns
Hold Time	12.381ns	11.330ns
Bonded IO	258	257

So from the above table it is clear that the delay (gate delay & net delay) as well as the power consumption is less in SPARTAN 2 FPGA.

References

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