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Design of High Performance & Low Power Up Down Counter on FPGA

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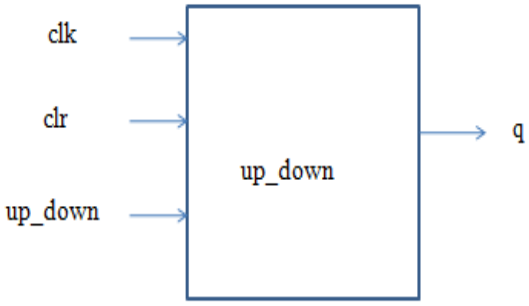
Abstract
Counters are the basic building block in embedded system design. Counters are used for counting purpose. Similarly it is used for frequency division.Counters are the Sequential Circuits in which the output depends upon the previous as well as present input.
Basically counters are classified in two categories one is Asynchronous Counter and another is Synchronous Counter. The operation of the counter is depending upon the clock which is a timing signal. Clock is required to change the state of the counter i.e. triggering. For high speed (fast response) clock is taken as negative edge triggered. Counters are designed using flip flops that are the basic storage elements in digital design.A sequential circuit is the combination of Combinational circuit and Memory.The present input is stored in combinational circuit and the previous input is stored in memory. There are various types of counters such as Ripple Counter, Up Counter, Down Counter, Johnson Counter and Synchronous Counter. Here we present the design of 64bit up down counter & implementation is done on FPGA.

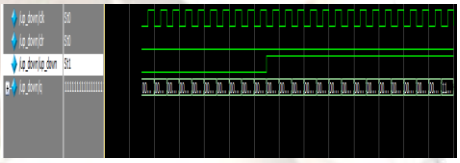
Keywords: Combinational Circuit, Sequential Circuit, Clock, Memory, FPGA

Architecture Design
In the present design clk, clr, up_down is the input and q is the 64bit output of the counter.



clk is taken as negative edge triggered. When clr is at logic 1 then counter is cleared i.e. it count 0.When clr is at logic 0 and up_down is 0 then it act as the up counter. On the other hand if up_down is 1 then it act as down counter. Now to check the functionality simulation is done on Modelsim-Altera 6.4a (Quartus 2 9.0).Synthesis is done on Xilinx ISE 9.2i.Now implementation is done on various FPGA to achieve high performance & low power consumption.

Simulation Result

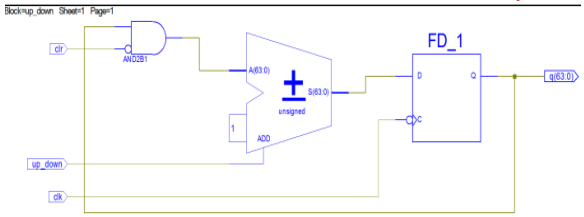


Synthesis
To generate the gate level netlist synthesis is done on Xilinx ISE 9.2i.So that the design becomes technology specific. Now synthesis is done on various FPGA. After synthesis the results obtained are given in the following table.

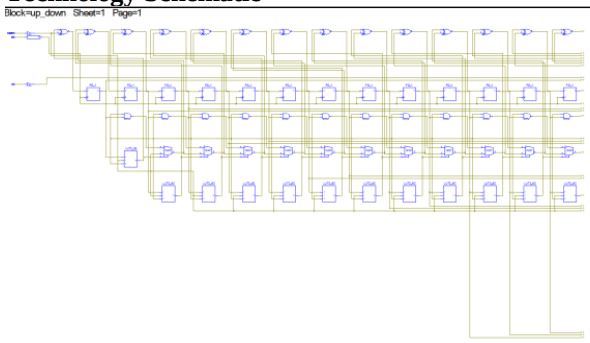
FPGA Type	Spartan2	Spartan3	Spartan3A	Virtex E	Virtex5	Virtex2 Pro
Speed	118.736MHz	148.204MHz	141.60MHz	152.091MHz	387.913MHz	219.575MHz
Setup Time	13.917ns	9.218 ns	9.015 ns	10.041ns	3.095 ns	6.125 ns
Hold Time	8.189 ns	6.280 ns	5.271 ns	5.967 ns	2.531 ns	3.340 ns
Gate Delay	8.189 ns	6.280 ns	5.271 ns	5.967 ns	2.531 ns	3.340 ns
Net Delay	6.849 ns	5.535 ns	4.891 ns	5.047 ns	2.288 ns	2.962 ns
Power Consumption	7mw	16mw	16mw	7mw	267mw	15mw
Gate Count	1409	1412	1412	1412	1409	1412

Final implementation is done on Virtex2 Pro FPGA .After synthesis speed are 219.575MHz & Power Consumption is 15mw.After simulation clock latency is 1 & clock load is 64.

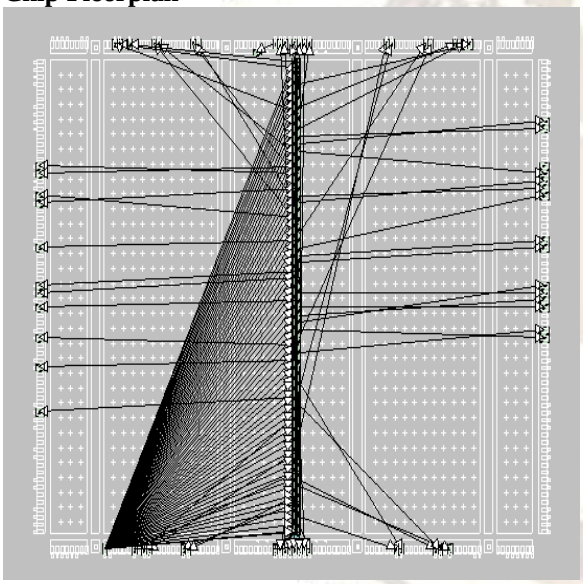
RTL Schematic



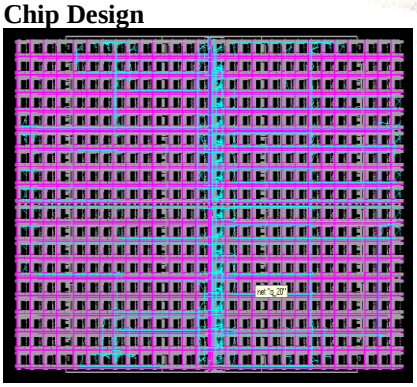
Technology Schematic



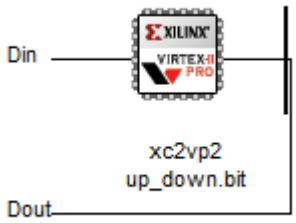
Chip Floorplan



Chip Design

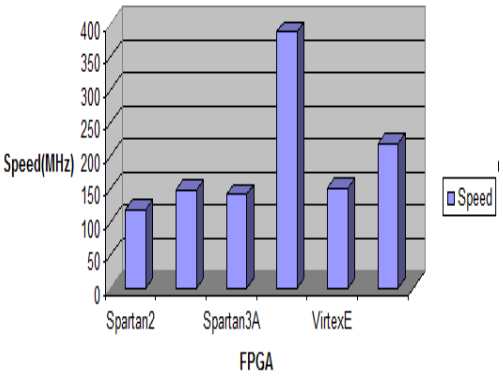


For synthesis xc2vp2-5fg256 package is used.



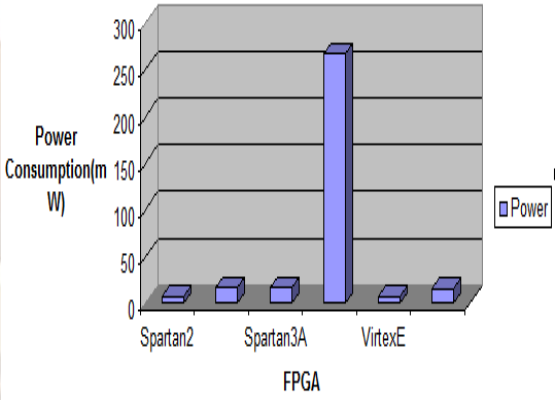
Results & Discussion

Speed



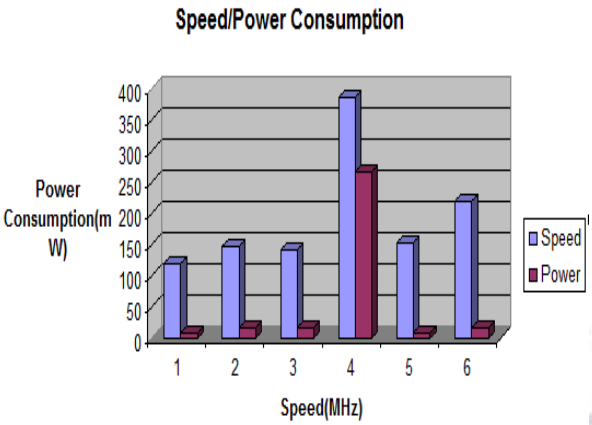
Virtex5 provides the highest speed of 387.913MHz.

Power Consumption



Here Spartan2 FPGA consumes 7mW power which is the lowest value.

Speed/Power Consumption



So Virtex2pro FPGA is required for high performance and low power consumption. In future architecture should be implemented for low chip area. And the count width can be increased from 64bit to 128bit.

Reference

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