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A Novel Fast Acting PI based Multilevel DSTATCOM

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Abstract- The instantaneous response of the distribution static compensator (DSTATCOM) is very important while compensating rapidly varying balanced, unbalanced and nonlinear loads. Any change in the load affects the dc-link voltage directly. The proper operation of DSTATCOM requires variation of the dc-link voltage within the prescribed limits. Conventionally, a proportional-integral (PI) controller is used to maintain the dc-link voltage to the reference value. It uses deviation of the capacitor voltage from its reference value as its input. However, the transient response of the conventional PI dc-link voltage controller is slow. In this paper, a fast-acting dc-link voltage controller based on the energy of a dc-link capacitor is proposed. Mathematical equations are given to compute the gains of the conventional controller based on fast-acting dc-link voltage controllers to achieve similar fast transient response. The detailed simulations are carried out on MATLAB environment to validate the proposed controller.

***Keywords*- DC-link voltage controller, DSTATCOM, fast transient response, THD, load compensation, power factor, power quality (PQ), unbalance, voltage-source inverter (VSI), Proportional-Integral (PI) control, CHB multilevel inverter, D-Q reference frame theory.**

I. INTRODUCTION

The proliferation of power-electronics-based equipment, nonlinear and unbalanced loads, has aggravated the power-quality (PQ) problems in the power distribution network. They cause excessive neutral currents, overheating of electrical apparatus, poor power factor, voltage distortion, high levels of neutral-to-ground voltage, and interference with communication systems [1], [2]. The literature says that the evolution of different custom power devices to mitigate the above power-quality problems by injecting voltages/currents or both into the system [3]–[6].

The shunt-connected custom power device, called the DSTATCOM, injects current at the point of common coupling (PCC) so that harmonic filtering, power factor correction, and load balancing can be achieved. The DSTATCOM consists of a current-controlled voltage-source inverter (VSI) which injects current at the PCC through the interface inductor. The operation of VSI is supported by a dc storage capacitor with proper dc voltage across it. One important aspect of the compensation is the extraction of reference currents. Various control algorithms are available in literature [7]–[11] to compute the reference compensator currents. However, instantaneous symmetrical component theory [11] is preferred. Based on this algorithm, the compensator reference currents are given as follows:

$$i_{fa}^{*} = i_{la} - \frac{V_{sa} + \gamma(V_{sb} - V_{sc})}{\sum_{i=a,b,c} V_{si}^{2}}\left(P_{lavg} + P_{dc}\right)$$

$$i_{fb}^{*} = i_{lb} - \frac{V_{sb} + \gamma(V_{sc} - V_{sa})}{\sum_{i=a,b,c} V_{si}^{2}}\left(P_{lavg} + P_{dc}\right)$$

$$i_{fc}^{*} = i_{lc} - \frac{V_{sc} + \gamma(V_{sa} - V_{sb})}{\sum_{i=a,b,c} V_{si}^{2}}\left(P_{lavg} + P_{dc}\right)$$

where $\gamma = \tan\varphi / \sqrt{3}$, and φ is the desired phase angle between the supply voltages and compensated source currents in the respective phases. The term P_{lavg} is the dc or average value of the load power. The term P_{dc} accounts for the losses in the VSI without any dc loads in its dc link. To generate P_{dc}, a suitable closed-loop dc-link voltage controller should be used, which will regulate the dc voltage to the reference value. The transient performance of the compensator is decided by the computation time of average load power and losses in the compensator. In most DSTATCOM applications, losses in the VSI are a fraction of the average load power. Therefore, the transient performance of the compensator mostly depends on the computation of P_{lavg}. In this paper, P_{lavg} is computed by using a moving average filter (MAF) to ensure fast dynamic response. The settling time of the MAF is a half-cycle period in case of odd harmonics and one cycle period in case of even harmonics presence in voltages and currents. Although the computation of P_{dc} is generally slow and updated once or twice in a cycle, being a small value compared P_{lavg} to, it does not play a significant role in transient performance of the compensator. In some applications, such as the telecommunications industry uses several parallel-connected switch-mode rectifiers to support dc bus voltage. Such an arrangement draws nonlinear load currents from the utility. This causes poor power factor and, hence, more losses and less efficiency. Clearly, there are PQ

issues, such as unbalance, poor power factor, and harmonics produced by telecom equipment in power distribution networks. Therefore, the functionalities of the conventional DSTATCOM should be increased to mitigate the aforementioned PQ problems and to supply the dc loads from its dc link as well. The load sharing by the ac and dc bus depends upon the design and the rating of the VSI. Here, there are two important issues. The first one is the regulation of the dc-link voltage within prescribed limits under transient load conditions. The second one is the settling time of the dc–link voltage controller. Conventionally, a PI controller is used to maintain the dc-link voltage. It uses the deviation of the capacitor voltage from its reference value as its input. However, the transient response of the conventional dc-link voltage controllers is slow, especially in applications where the load changes rapidly. Some work related to dc-link voltage controllers and their stability is reported in [16]–[20]. In this paper, a fast-acting dc-link voltage controller based on the dc-link capacitor energy is proposed. The detailed modeling and simulation verifications are carried out by using MATLAB environment to prove the efficacy of this fast-acting dc-link voltage controller. There is no systematic procedure to design the gains of the conventional PI controller used to regulate the dc-link voltage of the DSTATCOM. But some, mathematical equations are given to design the gains of the conventional controller based on the fast-acting dc-link voltage controllers to achieve similar fast transient response.

II. DESIGN OF MULTILEVEL BASED DSTATCOM

A. *Principle of DSTATCOM*

A D-STATCOM (Distribution Static Compensator), which is schematically depicted in Figure-1, consists of a two-level Voltage Source Converter (VSC), a dc energy storage device, a coupling transformer connected in shunt to the distribution network through a coupling transformer. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the D-STATCOM output voltages allows effective control of active and reactive power exchanges between the DSTATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

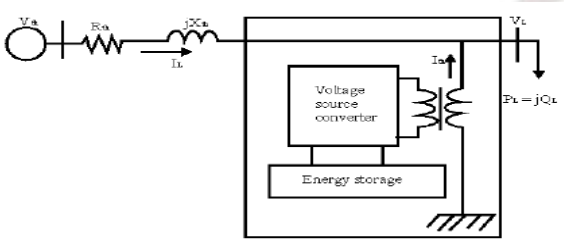

Figure – 1 Schematic Diagram of a DSTATCOM

The VSC connected in shunt with the ac system provides a multifunctional topology which can be used for up to three quite distinct purposes:

1. Voltage regulation and compensation of reactive power;
2. Correction of power factor
3. Elimination of current harmonics.

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter. As shown in Figure-1 the shunt injected current I_{sh} corrects the voltage sag by adjusting the voltage drop across the system impedance Z_{th}. The value of I_{sh} can be controlled by adjusting the output voltage of the converter. The shunt injected current I_{sh} can be written as,

$$I_{sh} = I_L - I_S = I_L - (V_{th} - V_L) / Z_{th} \quad (1)$$

$$I_{sh} /\_\eta = I_L /\_- \theta \quad (2)$$

The complex power injection of the D-STATCOM can be expressed as,

$$S_{sh} = V_L I_{sh}^* \quad (3)$$

It may be mentioned that the effectiveness of the DSTATCOM in correcting voltage sag depends on the value of Z_{th} or fault level of the load bus. When the shunt injected current I_{sh} is kept in quadrature with V_L, the desired voltage correction can be achieved without injecting any active power into the system. On the other hand, when the value of I_{sh} is minimized, the same voltage correction can be achieved with minimum apparent power injection into the system.

B. *Control for Harmonics Compensation*

The Modified Synchronous Frame method is presented in [7]. It is called the instantaneous current component (id-iq) method. This is similar to the Synchrous Reference Frame theory (SRF) method. The transformation angle is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the 3-phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages V (a,b,c) and the available currents i_l (a,b,c) in α-β components must be calculated as given by (4), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where 'θ' represents the instantaneous voltage vector angle (5).

$$\begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix} = [C] \begin{bmatrix} I_{la} \\ I_{lb} \\ I_{lc} \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} I_{ld} \\ I_{lq} \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix}, \theta = tan^{-1} \frac{V_\beta}{V_\alpha} \quad (5)$$

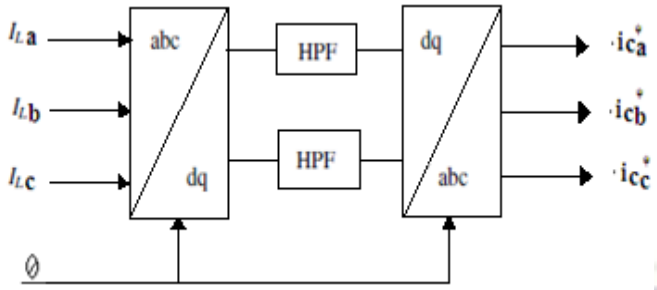

Figure-2 Block diagram of SRF method

Figure-2 shows the block diagram SRF method. Under balanced and sinusoidal voltage conditions angle θ is a uniformly increasing function of time. This transformation angle is sensitive to voltage harmonics and unbalance; therefore dθ/dt may not be constant over a mains period. With transformation given below the direct voltage component .

III. DC-LINK VOLTAGE CONTROLLERS

The sudden removal of load would result in an increase in the dc-link voltage above the reference value, whereas a sudden increase in load would reduce the dc-link voltage below its reference value. As mentioned before, the source supplies an unbalanced nonlinear ac load directly and a dc load through the dc link of the DSTATCOM, as shown in figure-1. Due to transients on the load side, the dc bus voltage is significantly affected. To regulate this dc-link voltage, closed-loop controllers are used. The proportional-integral-derivative (PID) control provides a generic and efficient solution to many control problems. The control signal from PID controller to regulate dc link voltage is expressed as

$$U_c = K_p (V_{dc\ ref} - V_{dc}) + K_i \int (V_{dc\ ref} - V_{dc})dt + Kd\ d/dt(Vdc\ ref - Vdc) \quad (7)$$

In (7), K_p, Ki and K_d are proportional, integral, and derivative gains of the PID controller, respectively. The proportional term provides overall control action proportional to the error signal. An increase in proportional controller gain (K_p) reduces rise time and steady-state error but increases the overshoot and settling time. An increase in integral gain (K_i) reduces steady state error but increases overshoot and settling time. Increasing derivative gain (K_d) will lead to improved stability. However, practitioners have often found that the derivative term can behave against anticipatory action in case of transport delay. A cumbersome trial-and-error method to tune its parameters made many practitioners switch off or even exclude the derivative term [31], [32]. Therefore, the description of conventional and the proposed fast-acting dc-link voltage controllers using PI controllers are given in the following subsections.

A. Conventional DC-Link Voltage Controller

The conventional PI controller used for maintaining the dc-link voltage is shown in figure-6. To maintain the dc-link voltage at the reference value, the dc-link capacitor needs a certain amount of real power, which is proportional to the difference between the actual and reference voltages. The power required by the capacitor can be expressed as follows:

$$P_{dc} = K_p (V_{dc\ ref} - V_{dc}) + K_i \int (V_{dc\ ref} - V_{dc})dt \quad (8)$$

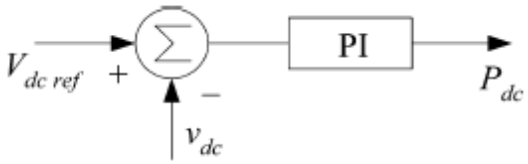

Figure-6 Schematic diagram of the conventional dc-link voltage controller

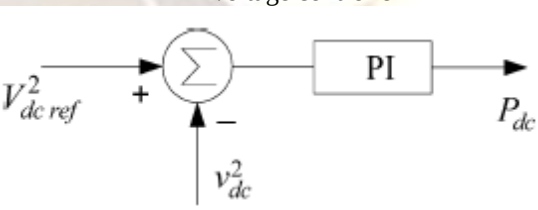

Figure-7 Schematic diagram of the fast-acting dc-link voltage controller

The dc-link capacitor has slow dynamics compared to the compensator, since the capacitor voltage is sampled at every zero crossing of phase supply voltage. The sampling can also be performed at a quarter cycles depending upon the symmetry of the dc-link voltage waveform. The drawback of this conventional controller is that its transient response is slow, especially for fast-changing loads. Also, the design of PI controller parameters is quite difficult for a complex system and, hence, these parameters are chosen by trial and error. Moreover, the dynamic response during the transients is totally dependent on the values of K_p, and K_i, when P_{dc} is comparable to P_{lavg}.

B. Fast-Acting DC Link Voltage Controller

To overcome the disadvantages of the aforementioned controller, an energy-based dc-link voltage controller is proposed. The energy required by the dc-link capacitor (W_{dc}) to charge from actual voltage (V_{dc}) to the reference value ($V_{dc\ ref}$) can be computed as

$$W_{dc} = ½\ C_{dc} (V_{dc\ ref}^2 - V_{dc}^2) \quad (9)$$

In general, the dc-link capacitor voltage has ripples with double frequency, that of the supply frequency. The dc power (P'_{dc}) required by the dc-link capacitor is given as

$$P'_{dc} = \frac{W_{dc}}{T_c} = \frac{1}{2T_c} C_{dc} (V_{dc\ ref}^2 - V_{dc}^2) \quad (10)$$

where T_c is the ripple period of the dc-link capacitor voltage. Some control schemes have been reported in [33] and [34]. However, due to the lack of integral term, there is

a steady-state error while compensating the combined ac and dc loads. This is eliminated by including an integral term. The input to this controller is the error between the squares of reference and the actual capacitor voltages. This controller is shown in figure-7 and the total dc power required by the dc-link capacitor is computed as follows:

$P_{dc} = K_{pe}(V_{dc\ ref}^2 - V_{dc}^2) + K_{ie}\int(V_{dc\ ref}^2 - V_{dc}^2)dt$ (11)

The coefficients K_{pe} and K_{ie} are the proportional and integral gains of the proposed energy-based dc-link voltage controller. As an energy-based controller, it gives fast response compared to the conventional PI controller. Thus, it can be called a fast acting dc-link voltage controller. The ease in the calculation of the proportional and integral gains is an additional advantage. The value of the proportional controller gain (K_{pe}) can be given as

$K_{pe} = C_{dc} / 2T_c$ (12)

For example, if the value of dc-link capacitor is 2200 μF and the capacitor voltage ripple period as 0.01 s, then K_{pe} is computed as 0.11 by using (12). The selection of K_{ie} depends upon the tradeoff between the transient response and overshoot in the compensated source current. Once this proportional gain is selected, integral gain is tuned around and chosen to be 0.5. It is found that if K_{ie} is greater than K_{pe} / 2, the response tends to be oscillatory and if K_{ie} is less than K_{pe} / 2, then response tends to be sluggish. Hence, K_{ie} is chosen to be K_{pe} / 2.

IV. DESIGN OF CONVENTIONAL CONTROLLER BASED ON THE FAST-ACTING DC-LINK VOLTAGE CONTROLLER

The conventional dc-link voltage controller can be designed based on equations given for the fast-acting dc-link voltage controller as in (11) and can be written as

$P_{dc} = K_{pe}(V_{dc\ ref} + V_{dc})(V_{dc\ ref} - V_{dc}) + K_{ie}\int(V_{dc\ ref} + VdcVdc\ ref - Vdcdt$ (13)

It can also be written as

$P_{dc} = K_p'(V_{dc\ ref} - V_{dc}) + K_i'\int(V_{dc\ ref} - V_{dc})dt$ (14)

Where

$K_p' = K_{pe}(V_{dc\ ref} + V_{dc})$ (15)

$K_i' = K_{ie}(V_{dc\ ref} + V_{dc}$ (16)

It is observed from the aforementioned equations that the gains of proportional and integral controllers vary with respect to time. However, for small ripples in the dc-link voltage, $V_{dc} \approx V_{dc\ ref}$, therefore, we can approximate the above gains to the following

$K_p' \approx 2K_{pe}V_{dc\ ref}$ (17)

$K_i' \approx 2K_{ie}V_{dc\ ref}$ (18)

The relations (17)–(18) give approximate gains for a conventional PI controller. This is due to the fact that $V_{dc\ ref} + V_{dc}$ is not really equal to $2V_{dc\ ref}$ until variation in V_{dc} is small during transients. Hence, the designed conventional PI controller works only on approximation. The open-loop gains for the two cases are given by

$\frac{P_{dc}}{E_{er}} = \frac{K_{pe}(s+\frac{K_{ie}}{K_{pe}})}{s}$ (19)

Where $E_{er} = V_{dc\ ref}^2 - V_{dc}^2$ and

$\frac{P_{dc}}{E_r} = \frac{K_p'(s+\frac{K_i'}{K_p'})}{s}$ (20)

where $E_r = V_{dc\ ref} - V_{dc}$. Since $\frac{K_i^1}{K_p^1}$ is the same as K_{ie} / K_{pe},the higher gain in the conventional PI controller renders less stability than that of the proposed energy-based dc-link controller. For nearly the same performance, the conventional PI controller has gains which are 364 (40/0.11 from Table-III) times larger than that of that proposed one. Also, the amplifier units used to realize these gains need more design considerations and are likely to saturate when used with higher gains.

TABLE -III: SIMULATION PARAMETERS

System Parameters	Values
supply voltage	400 V (L-L), 50 Hz
Unbalanced load	$Z_a = 25\ \Omega$, $Z_b = 44 + j25.5\ \Omega$ and $Z_c = 50 + j86.6\ \Omega$
Nonlinear load	Three-phase full wave rectifier drawing a dc current of 5 A
DC load	$R_{dc} = 100\ \Omega$
DC capacitor	$C_{dc} = 2000\ \mu F$
Interface inductor	$L_f = 26$ mH, $R_f = 0.25\ \Omega$
Reference dc link voltage	$V_{dc\ ref} = 520$ V
Hysteresis band	$\pm h = 1.0$ A
Gains of conventional dc link voltage controller	$K_p = 40$, $K_i = 20$
Gains of fast acting dc link voltage controller	$K_p = 0.11$, $K_i = 0.055$

V. SELECTION OF THE DC-LINK CAPACITOR

The value of the dc-link capacitor can be selected based on its ability to regulate the voltage under transient conditions. Let us assume that the compensator in Fig. 1 is connected to a system with the rating of X kilovolt amperes. The energy of the system is given by X x 1000 J/s. Let us further assume that the compensator deals with half (i.e.,X/2) and twice (i.e., 2X) capacity under the transient conditions for cycles with the system voltage period of Ts. Then, the change in energy to be dealt with by the dc capacitor is given as

$\Delta E = (2X - X/2)\ nT$ (21)

Now this change in energy (21) should be supported by the energy stored in the dc capacitor. Let us allow the dc capacitor to change its total dc-link voltage from 1.4 V_m to 1.8 V_m during the transient conditions where V_m is the peak value of phase voltage. Hence, we can write

$\frac{1}{2} C_{dc}[(1.8V_m)^2 - (1.4V_m)^2] = (2X - X/2)\ nT$ (22)

which implies that

$C_{dc} = \frac{3XnT}{(1.8V_m)^2 - (1.4V_m)^2}$ (23)

For example, consider a 10-kVA system (i.e., X = 10 kVA), system peak voltage V_m = 325.2 V, n = 0.5, and T = 0.02 s. The value of C_{dc} computed using (23) is 2216 μF.

Practically, 2000 μF is readily available and the same value has been taken for simulation and experimental studies.

IV MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Figure-8 shows the Matab/Simulink power circuit model of DSTATCOM. It consists of five blocks named as source block, non linear load block, control block, APF block and measurements block. The system parameters for simulation study are source voltage of 11kv, 50 hz AC supply, DC bus capacitance 1550e-6 F, Inverter series inductance 10 mH, Source resistance of 0.1 ohm and inductance of 0.9 mH. Load resistance and inductance are chosen as 30mH and 60 ohms respectively.

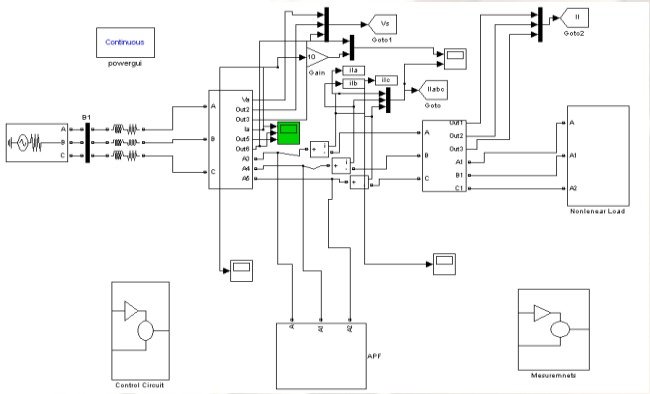

Figure-8 Matlab/Simulink power circuit model of DSTATCOM

Fig. 9 shows the phase-A voltage of five level output of level shifted carrier PWM inverter.

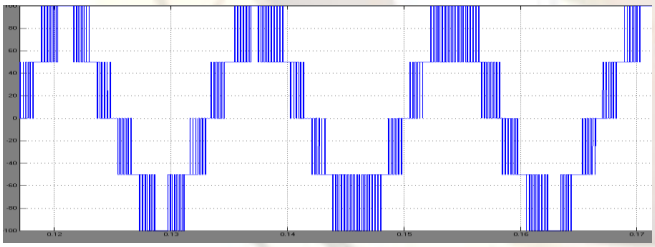

Fig. 10 five level PSCPWM output

Figure-10 shows the three phase source voltages, three phase source currents and load currents respectively without DSTATCOM. It is clear that without DSTATCOM load current and source currents are same.

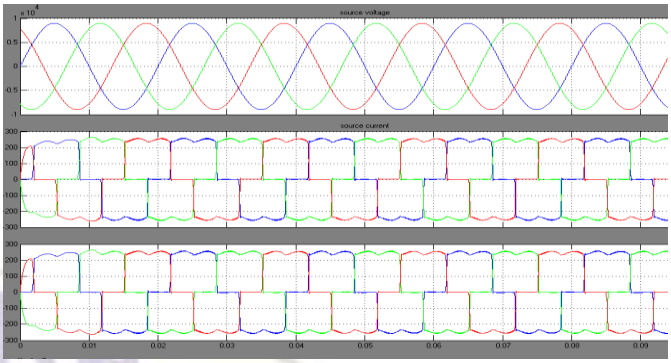

Figure-9 Source voltage, current and load current without DSTATCOM

Figure-11 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal source currents are sinusoidal.

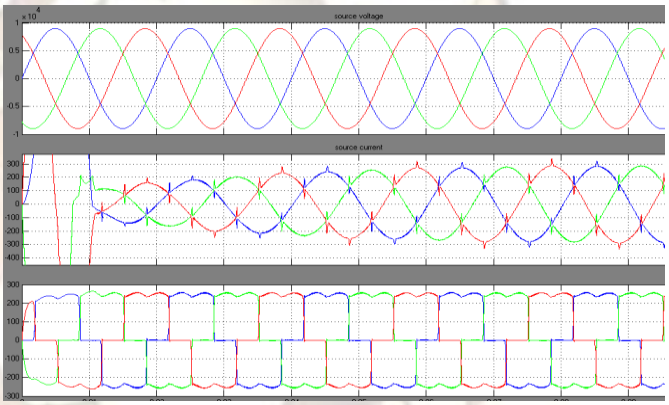

Figure-11 Source voltage, current and load current with DSTATCOM

Figure-12 shows the DC bus voltage. The DC bus voltage is regulated to 11kv by using PI regulator.

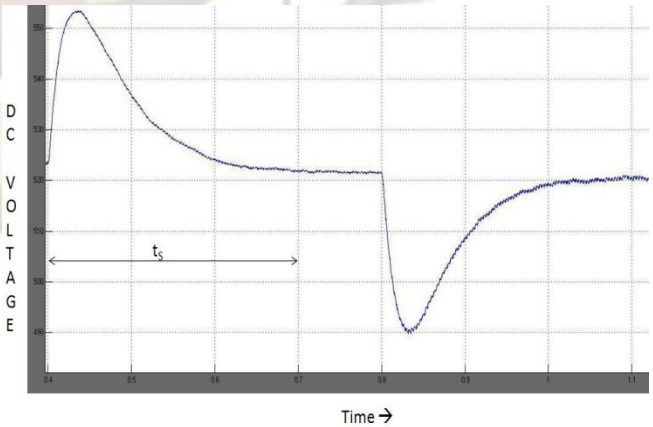

Figure-12 DC Bus Voltage with PI controller

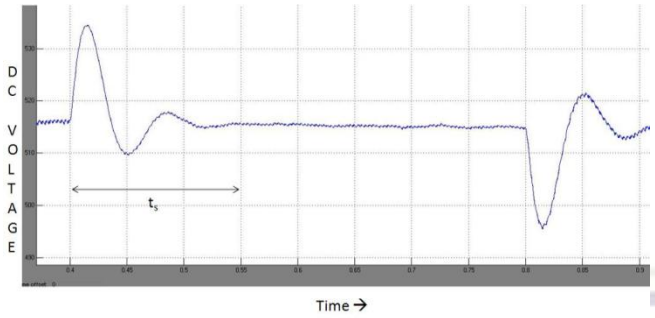

Figure-13 DC Bus Voltage with fast PI controller

Figure-13 shows the DC bus voltage with fast PI controller. Form the figure it is clear that with fast PI controller DC link voltage controlled with less time.

Figure-14 shows the phase-A source voltage and current, even though the load is non linear RL load the source power factor is unity.

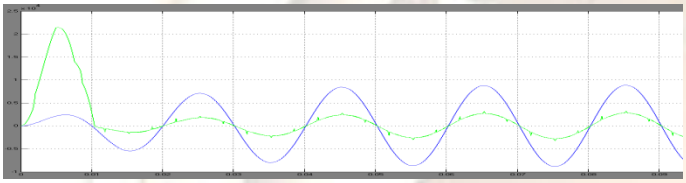

Figure-14 Phase-A source voltage and current

Figure-15 shows the harmonic spectrum of Phase –A Source current without DSTATCOM. The THD of source current without DSTACOM is 36.89%.

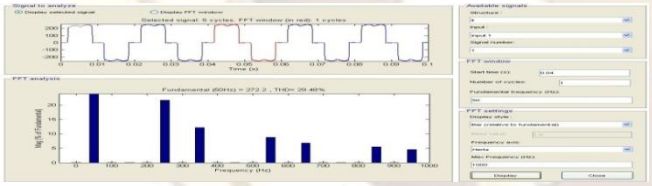

Figure-15 Harmonic spectrum of Phase-A Source current without DSTATCOM

Figure-16 shows the harmonic spectrum of Phase –A Source current with DSTATCOM. The THD of source current without DSTACOM is 5.05%

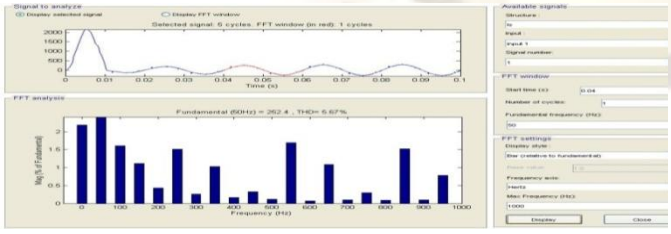

Figure-16 Harmonic spectrum of Phase-A Source current with DSTATCOM

VI CONCLUSION

A VSI topology for DSTATCOM compensating ac unbalanced and nonlinear loads and a dc load supplied by the dc link of the compensator is presented. The state-space modeling of the DSTATCOM is discussed for carrying out the simulation studies. An energy-based fast-acting dc-link voltage controller is suggested to ensure the fast transient response of the compensator. Mathematical equations are developed to compute the gains of this controller.Finally Matlab/Simulink based model is developed and simulation results are presented.

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