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Design of High Performance Phase Locked loop for Multiple outputs with Ultra Low Power Sub Threshold Logic

K.Rajasekhar[#1]
S.Adilakshmi*[2] **T.B.K. Manoj kumar**[#3]
1. Student, M.Tech (VLSI) ,Vaddeswaram, Green Fields, KL University, Vijayawada , Andhra Pradesh, India
2.Assitant Professor , DEPT of CSE, KL University, Vaddeswaram , Vijayawada , Andhra Pradesh, India
3. Student, M.Tech (VLSI) ,Vaddeswaram, Green Fields, KL University, Vijayawada , Andhra Pradesh, India

Abstract- Phased lock loop is a control system that generates an output signal whose phase of an input reference signal. This compares the phase of the input signal with the phase derived from its output oscillator adjusts the frequency of its oscillator to keep the phase matches. The signal from the phase detector is used to control the oscillator in a feedback loop. As such a operational device the PLL has wide range of application s in telecommunication, computers and electronic applications. The phase locked loop consists of frequency oscillator and a phase detector. The work represents the layout design of Phased Lock loop PLL with multiple outputs. Effort has been made to design ultra low power design and it is implemented using ultra low power sub threshold D flip flop. The proposed architecture is implemented for 45nm CMOS technology. This is carried out for the inner electronics of all sub blocks like oscillator and phase detector. The main novelties related to the 45 nm technology are the high-k gate oxide, metal gate and very low-k interconnect dielectric. The design implemented in analog design tool like Microwind 3.1 where each sub block is designed at its ultra low power design.

Keywords : PLL, ultra low power design, micro wind 3.1

I. INTRODUCTION

Power has become one of the most important paradigms of design convergence for multi gigahertz communication systems such as optical data links, wireless products, microprocessor & ASIC/SOC designs. The current leading-edge technologies (such as low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications on VLSI and systems design. One of the most important characteristics of information services is their increasing need for very high processing power and bandwidth (in order to handle real-time video, for example). The other important characteristic is that the information services tend to become more and more personalized (as opposed to collective services such as broadcasting), which means that the devices must be more intelligent to answer individual demands, and at the same time they must be portable to allow more flexibility/mobility. Since the multiple outputs Phase Locked Loop (PLL) provides multiple clock generation, it is to be needed to design PLL with multiple output for modern communication Engineering applications with low power, high stability and low jitter.

This paper introduces a design aspect for layout design of low power PLL with four multiple output using VLSI technology. PLL is widely applied for different purposes in various domains such as communication and instrumentation. Phase locked loop can be used to maintain a well-defined phase, and hence frequency relation between two independent signal sources [2].

The proposed PLL is a feed back system composed of three elements: a phase detector, a loop filter and a high performance voltage controlled oscillator (VCO). Reported work describes the use of VLSI technology to design optimum layout for Low Power, High performance phase locked loop with multiple output. The design process, at various levels, is usually evolutionary in nature. It starts with a given set of requirement. When the requirements are not met, the design has to be improved. More simplified view of the VLSI technology consists of various representations, abstractions of design, logic circuits, CMOS circuits and physical layout.

Here for the design, microwind 3.1 VLSI Backend software is used. This software allows designing and simulating an integrated circuit at physical description level. The proposed PLL is designed using 45 mm CMOS/VLSI technology in microwind 3.1software, which in turn offers high speed performance at low power.

TABLE I

Parameter	value
VDD	0.85-1.2 v
Ioff N(nA/um)	5-100
Ion P(nA/um)	5-100
Gate dielectric	Sion –hfo2
No of metal layers	6-10

Compared to 65-nm technology, 45 nm technology must offer:
1) 30% increases in switching performance
2) 30 % reduction in Power consumption
3) 2 times higher density
Considering the advantage of 45 nm technologies over 90 nm & 65 nm technologies, the proposed work is done with 45 nm technologies. Power consumption is a limiting factor in VLSI integration for portable applications. The resulting heat dissipation also limits the feasible packaging and performance of the VLSI chip. Since the dynamic power dissipation in synchronous digital integrated circuit is determined by *CV2f*, reducing the supply voltage is an effective way to reduce power consumption of the modern electronic systems [2]. As the supply voltage scales down with the technology, any power supply noise on power and ground level affects the analog circuit performance more than before. This power supply noise has a direct effect on the voltage controller oscillator (VCO) output frequency of PLL which is proportional to the control voltage from the charge pump.

2. PROPOSED PHASE LOCKED LOOP DESIGN

Until DSP technology is capable of directly processing and generating the RF signals used to transmit wireless data, raditional RF engineering will remain a fundamental part of wireless communication systems design. As it stands, wireless transceivers must still be able to generate a wide range of frequencies in order to upconvert the outgoing data for transmission and downconvert the received signal for processing. Monolithic phase locked loops have been used for clock-&-data recovery in communication system, clock generation and distribution in microprocessor and frequency synthesis in wireless application. [3]. A proposed PLL is a feedback system composed of three elements: a phase detector, a loop filter and a high performance voltage controlled oscillator (VCO). To obtain the layout of proposed PLL, CMOS circuit of each element of proposed PLL is converted into physical layout using lamda based rules of microwind 3.1 software. After cascading the layout of each element, final layout is obtained. This paper particularly focuses on analysis and design of phase-locked loop with low power consumption using VLSI technology.

3. DESIGN OF PHASE DETECTOR

The phase detector determines the relative phase difference between two incoming signalsand outputs a signal that is proportional to this phase difference. This output signal is then used to adjust the output of the VCO and thus align the two inputs via a feedback network. One of the inputs to the phase detector is a reference clock that is typically generated offchip while the other clock input is a divided version of the VCO. Two basic types of phase detectors are commonly used. These include the XOR gate and the phase frequency detector (pfd).

3.1 XOR Phase Detector: The XOR phase detector is the simplest phase detector. The XOR is useful as a phase detector since the time when the two inputs are different (or same) represents the relative phase. Figure 10.59 shows the XOR of two waveforms. The output of the XOR is low pass filtered and acts as a control voltage to the VCO. The output (low pass filtered) as a function of the phase error is also shown.

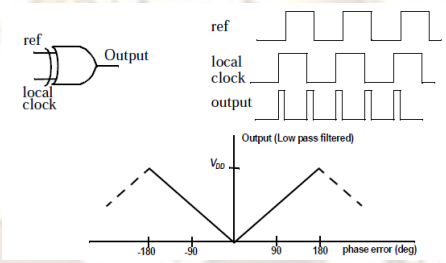

Fig 1 :xor as a phase detector

For this detector any deviation in a positive or negative direction from the the perfect in-phase condition (i.e., phase error of zero) produces the same change in duty factor resulting in the same average voltage. Thus the linear phase range is only 180 degrees. Using such a phase detector, a PLL will lock to a quadrature phase relationship (i.e., ¼ cycle offset) between the two inputs. A drawback of the XOR phase detector is that it may lock to a multiple of the clock frequency. If the local clock is a multiple of the reference clock frequency, the output of the phase detector will still be a square wave of 50% duty cycle, albeit at a different frequency. The filtered version of this signal will be identical to that of the truly locked state and thus the VCO will operate at the nominal frequency.

3.2Phase-Frequency Detector:

The phase-frequency detector (PFD) is the most commonly used form of phase detector, and it solves several of the shortcomings of the detectors discussed

above. As the name implies, the output of the PFD is dependent both on the phase and frequency difference of the applied signals. Accordingly, it cannot lock to an incorrect multiple of the frequency. The PFD takes two clock inputs and produces two outputs, UP and DOWN as shown in Figure.

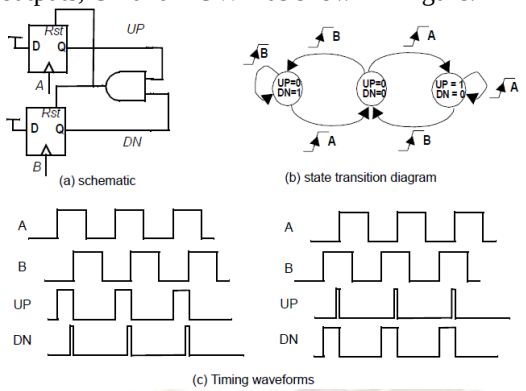

Fig 2 : phase frequency detector

The PFD is a state machine with 3 states. Assume that both UP and DN outputs are initially low. When input A leads B, the UP output is asserted on the rising edge of input A. The UP signal remain in this state until a low-to-high transition occurs on input B. At that time, the DN output is asserted, causing both flip-flops to reset through the asynchronous reset signal. Notice that a short pulse proportional to the phase error is generated on the DN signal, and that there is a small pulse on the DN output, whose duration is is equal to the delay throught he AND gate and register reset delay. The pulse width of the UP pulse is equal to the phase error between the two signal. The roles are reversed for the case when input B lags A, and a pulse proportional to the phase error is generated on the DN output. If the loop is in lock, short pulses will be generated on the UP and DN outputs.

4. Charge Pump and loop filter : The UP/DN pulses must be converted to an analog voltage that controls the VCO. One possible implementation is shown in Figure. A pulse on the UP signal adds a charge packet proportional to the size of the UP pulse, and a pulse on the DN signal removes a charge packet proportional to the DN pulse. If the width of the UP pulse is large than the DN pulse, then there is a net increase in the control voltage. This effectively increases the frequency of the VCO.

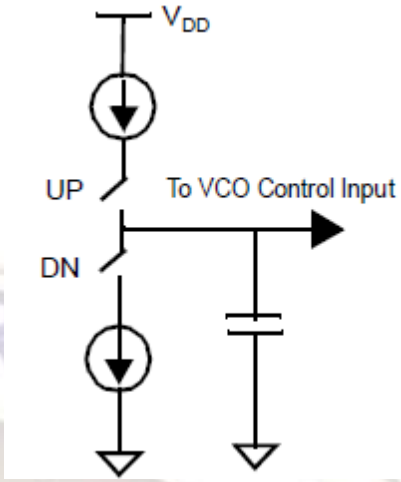

Fig 3 : charge pump

Charge pump sources current if output frequency/phase is too slow. Charge pump sinks current if output frequency/phase is too high. Charge pump in high impedance state if output frequency/phase is correct (with in tolerance). Charge pump Figures of merit want source and sink currents closely equal. Charge pump Figures of merit want tri-state to be very low leakage current. Theoretically the charge pump should sink and source the same current but in practice there will be always be some degree of mismatch. The mismatch can cause reference spurs and effect lock time, and is undesirable.

In the charge-pump PLL, the PFD outputs, *up* and *dn*, produce a narrow pulse in each phase comparison period (T_{ref})Noises in PLL generate the random part of the charge-pump output current (I_{out})while mismatches in the charge-pump generate deterministic and periodic part of I_{out}.

The charge pump gas 3 states.

1. Sink Current
2. Source current
3. Tri-state (High Impedance)

Loop filter is a low pass filter. It can also be thought of as an integrator with some added components. The loop filter determines a lot about PLL performance-switching time, Loop Bandwidth, Reference spurs. The loop filter is external to chip and is application specific

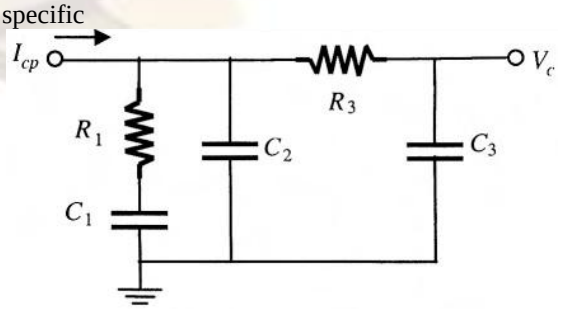

Fig. 4 loop filter

the low-pass filter smooth out the abrupt control inputs from the charge pump. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable inputs. The low pass filter for proposed PLL is designed using virtual
resistance of 1000 ohm with capacitor of 2 Pico farad.

5.VOLTAGE CONTROLLED OSCILLATOR:

The VCO is the most important functional unit in the PLL. Its output frequency determines the effectiveness of PLL. In addition to operating at highest frequency, this
unit consumes the most of the power in the system. Obviously, this unit is of particular focus to reduce power consumption. PLL with multiple outputs means to VCO with multiple output. Voltage Controlled Oscillator
required for PLL should posses following characteristics.

1) The oscillating frequency should be restricted to the required bandwidth. For
example, in European mobile phone applications, the VCO frequency should be
varying between flow= 1700 MHz and High=1800 MHz [3].

2) Due to process variations, the VCO frequency range should be extended to fmin,
fmax, typically 10% higher and lower than the request range.

3) When the control voltage Vc is equal to VDD/2, the clock should be centered in
the middle of the desired frequency range.

4) The duty cycle of VCO clock output should be as close as possible to 50%. If
this is not the case, the PLL would have problems locking, or would not produce
a stable output clock [3].

The proposed PLL uses high performance VCO as shown in fig. It provides very good linearity. The principle of this VCO is a delay cell with linear delay dependence on the control voltage. The delay cell consists of a p-channel MOS (pmos) in series,
controlled by Vcontrol, and a pull-down n-channel MOS (nmos) controlled by Vplage. The delay dependence on Vcontrol is almost linear for the fall edge. The key point is to design an inverter just after the delay-cell with a very low commutation point Vc. The rise edge is almost unchanged

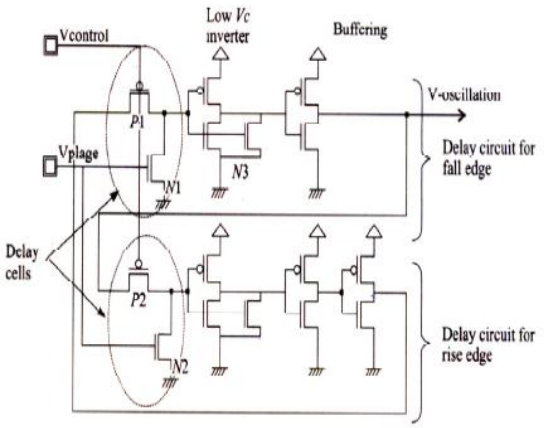

Fig 5: high performance vco

6.Low Power Sub threshold D Flip Flop:

Sub-threshold circuits operate with a supply voltage that is less than the threshold voltage of the transistor—far below traditional levels and consequently the transistor operates essentially based on leakage. While traditional digital CMOS transistors run either in the ON state (saturation) or OFF state (subthreshold), the subthreshold circuits are either in an OFF state or an almost-ON state (still in subthreshold region but with weak inversion). Running at these nonstandard operating points, limit the performance, which remains acceptable for low-to-medium cost applications giving substantial increase in the corresponding energy efficiency. As power is related quadratically to the supply voltage, reducing the voltage to these ultra-low levels results in a dramatic reduction in both power and energy consumption in digital systems. Due to the exponential current-voltage (I-V) characteristics of the transistor, subthreshold logic gates provide near ideal voltage transfer characteristics. Furthermore, in the subthreshold region, the transistor input capacitance is less than that of strong inversion operation. The transistor input capacitance, in subthreshold, is a combination of intrinsic (oxide capacitance and depletion capacitance) and parasitic (overlap capacitance, fringing capacitances) of a transistor. The subthreshold region is particularly important for low voltage, low-power applications, such as when the MOSFET is used as switch in digital logic and memory applications, because the subthreshold region describes how the switch turns on and off.

6.1. *Gate Diffusion Iinput Technique:*

The GDI approach allows implementation of a wide range of complex logic functions using only two transistors This method is suitable for design of fast, low power circuits, reduced number of transistors

while allowing simple top-down design. Gate-Diffusion-Input (GDI) design technique is an efficient alternative for the logic design in standard CMOS and SOI technologies [1],[3]. A basic GDI cell contains four terminals – G node (the common gate input of the NMOS and PMOS transistors), P node (the outer diffusion node of the PMOS transistor), N node (the outer diffusion node of the NMOS transistor), D node (the common diffusion of both transistors). P, N and D may be used as either input or output nodes, depending on the circuit structure shown in Fig.1 Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased in contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard p-well CMOS process, but can be successfully implemented in twin-well

CMOS or SO1 technologies. Multiple-input gates can be implemented by combining several GDI cells [4]. GDI enables simpler gates, lower transistor count, and lower power consumption in many implementations. This technique allows reducing power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design. The overall area and complexity of the circuit is minimized using GDI technique .Alsoimprovements areobserved in static power dissipation and logic level swing. Most of the functions which are complex (6-12 transistors) in CMOS, are very simple (only 2 transistors perfunction) in GDI design method.

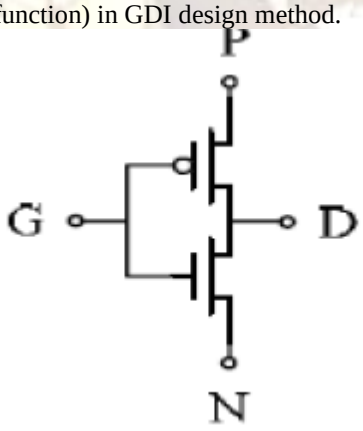

Fig 5 GDI symbol

6.2Flip Flop Design:

The NMOS of the proposed circuit shown in Fig.5 is delay element. Without this delay, the selected input of the Mux1 would toggle on the positive-edge of the clock before the updated value had arrived at its feedback input. NMOS is preferred over PMOS as NMOS has less on resistance and hence shows less power consumption. From the simulation results reveals that proposed circuit shows least power consumption as compared to all other circuits. This D flip flop require a delay on the clock fed to the selector of Mux1. In this case, the Inv1 could switch and change the state of the entire FF. Mux1 should toggle only after the Q (the feedback input of Mux1) reaches the sufficient level. Here NMOS provides sufficient delay so that until feedback has reached at the input of the MUX1.The presence of NMOS transistor would ensure that the MUX1 should toggle only when the output is generated at the positive edge of the clock. After this input is provided to MUX2 and the slave latch is enabled. Thisadded delay is necessary for right operation of the flipflop.

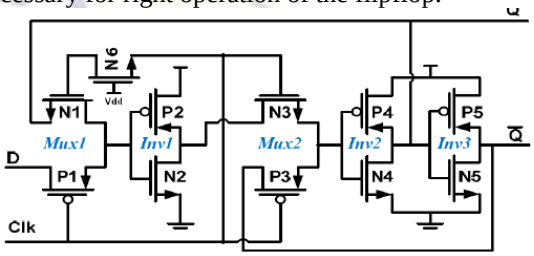

Fig 6:Proposed D Flip-Flop circuit using NMOS as delay element

7. Design of proposed pll:

For multiple output PLL, 1x is the basic output of PLL, the 900 phase shifted output is generated using delay circuits or using logic circuits which in turn offers his speed performance at low power. It have multiple outputs 1x, 2x, 4x and 8x, which can be utilized in multiphase clocking circuits.

To achieve the proposed target fallowing steps are include in the design and analysis of
proposed PLL.

1) Schematic design of each block of proposed PLL using CMOS transistors.
2) Performance verification of the above for different parameters.
3) CMOS layout for the proposed PLL using Lamda defined rules of VLSI
backend3.1 software.
4) Verification of CMOS layout and parameter testing.
5) If the goal is achieved for all proposed parameter including detail verification, sing
off for the design analysis and design will be ready for IC making.
6) If detail verification of parameters would not completed then again fallow the first step with different methodology.

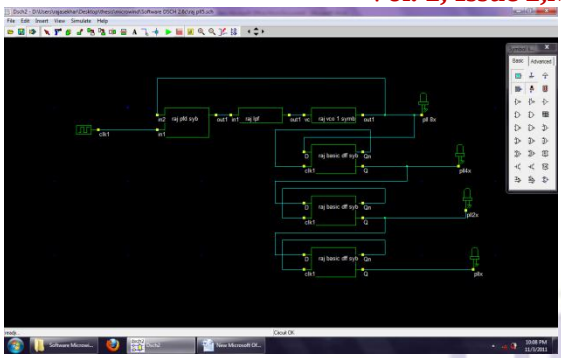

Fig 7:block diagram pll with four multiple outputs

Above Figure shows the optimum, high efficient chip design of low power PLL with fourbmultiple output using 45nm VLSI technology.

Fig 8. freqencies vs time response of propsed pll

Fig 9 layout design for pll with four outputs

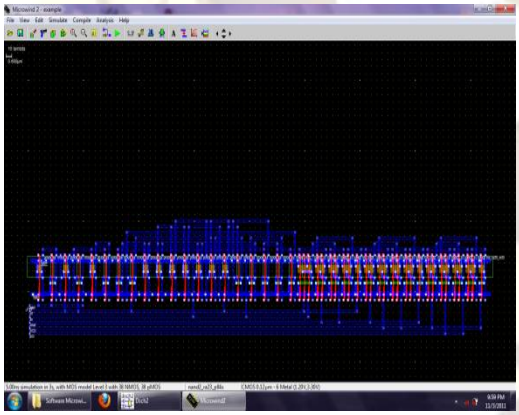

Fig 10 voltage vs time response of propsed pll

The PLL is locked at 3.3 GHz frequency. Figure-8 shows voltage verses time waveforms of PLL's outputs and inputs. When control voltage is reaches to 0.415 volt, PLL is locked to the frequency of 1.3 GHz. Multiple output of the PLL gives multiple frequencies of amplitude 1volt.

Thus the effort has been taken to design high efficient, optimum area chip for PLL with four outputs and low power.

CONCLUSION:

The proposed PLL is designed using 45 nm CMOS/VLSI technology with microwindn3.1. This PLL gives a four multiple outputs as PLL8x, PLL4x, PLL2x and PLL1x simultaneously. This can be used for multichanneling communication system which in turn provides a very fast multitasking communication. . Though there is the variation of supply voltage VDD from 0.5V to 1.2V, all the output of proposed PLL is found stable which proves the high stability of the PLL. From the parametric analysis of design tool, the power dissipation measured by VDD at 1Volt is found µwatt, which shows that power consumption is very low. In this way very high efficient, low power optimum area chip is designed for phase locked loop with four multiple outputs as PLL8x, PLL4x, and PLL2x & PLL1x of 1.3 GHz 1.25 GHz, 0.615 GHz, and 0.312 GHz respectively.

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KONARI.RAJASEKHAR received the B.Tech. degree in Electronics & Communications Engineering from JNTU KAKINADA in 2010 and pursuing M.Tech (VLSI) in K L University. . His research interests include Digital VLSI Design and low power vlsi.

T.B.K MANOJ KUMAR received the B.Tech. degree in Electronics & Communications Engineering from JNTU KAKINADA in 2010 and pursuing M.Tech (VLSI) in K L University. . His research interests include Digital VLSI Design and and low power vlsi.

Ms.S.Adilakshmi received her B.Tech degree in Electronics & Communications Engineering from RVR&JC College of Engineering which is affiliated to Acharya Nagarjuna University in 2005, AP, and India. M.Tech degree in VLSI Design in TKR College of Engineering & Technology which is affiliated to JNTU Hyderabad in 2011. Presently she is working as Assistant Professor, Department of ECE in K.L.University, Guntur, AP, and India. She research intrest in development of Low-Power VLSI, DSP, and Embedded Systems .