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Design And Analysis Of 8-Bit Multiplier Using Body Biasing Techniqe

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Abstract—
Design of high-speed low-power VLSI logic circuits with CMOS technology has been a major research problem for many years. Several logic families have been proposed and used to improve the circuit performance beyond that of conventional static CMOS family. Dynamic domino logic circuits are widely used in modern digital VLSI circuits. These dynamic circuits are often favored in high performance designs because of the speed advantage over static CMOS logic circuits. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power Consumption. Body biasing is another method of improving energy/efficiency, by reclaiming performance lost to margins due to variations. After fabrication, the threshold voltage (*Vth*) of transistors can be modulated by changing the body-to-source voltage. In this work we are going to design Adder and Multiplier circuits with the body biasing technique and compare the power and performance variations.

Keywords- Low power, CMOS, Dynamic, Body biasing

1. Introduction

VLSI designers have different options to reduce the power dissipation in the various design stages. For example, the supply voltage may be reduced through fabrication technology, circuit design or dynamically through the system level. An effective way to reduce power consumption is supply voltage scaling. Lowering the supply voltage, however, degrades circuit speed. Threshold voltages are scaled to reduce the degradation in speed caused by supply voltage scaling while maintaining the dynamic power consumption within acceptable levels [1].

Energy efficient circuit techniques aimed at lowering leakage currents are, therefore, highly desirable. Dynamic Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics compared to static CMOS circuits. The main drawbacks of dynamic logic are a lack of design automation, a decreased tolerance to noise and increased power consumption [2]-[3].

Thus for low power applications, sub threshold operation is a better option. Low power systems are slower ones, because of trade-off between power and speed [4]. The sub threshold logic operates with the power supply Vdd less than the threshold voltage (Vth) of the transistor. Body biasing is a method of improving energy/efficiency, by reclaiming performance lost to margins due to variations. After fabrication, the threshold voltage (*Vth*) of transistors can be modulated by changing the body-to-source voltage.

Much of the research efforts of the past years is the requirement of portability and the moderate improvement in battery performance indicate that the power dissipation is one of the most critical design parameters[5]. The three most widely accepted metrics to measure the quality of a circuit or to compare various circuit styles are area, delay and power still demands high computational speeds. Hence, in recent VLSI systems the power-delay product becomes the most essential metric of performance.

The operation of adder and multiplier circuits are elucidated and it is simulated using TANNER EDA tool Version 14.11, and it is compared with static CMOS logic circuits in terms of, power dissipation and propagation delays at 65nm technology is carried out.

2. Limitations Of Dynamic Circuits

In today‘s fast processing environment, the use of dynamic circuits are becoming increasingly popular [7]. Dynamic CMOS circuits are defined as those circuits which have an additional clock signal inputs along with the default combinational circuit inputs of the static systems. Dynamic systems are faster and efficient than the static systems.

The main problem in Dynamic circuits is suffers from charge sharing problem because of parasitic capacitances at different nodes of a circuit. This results in lower voltage levels at the output terminals.

In general, dynamic logic greatly increases the number of transistors that are switching at any given time, which increases power consumption over static

CMOS. There is several power saving techniques that can be implemented in a dynamic logic based system.

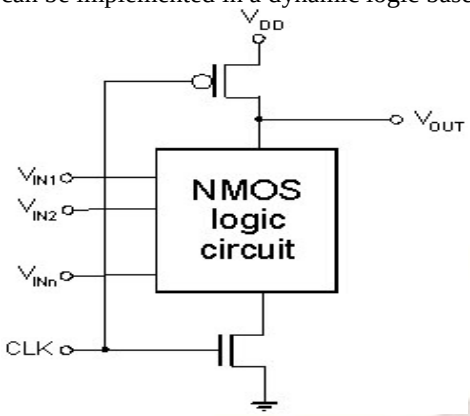


Fig.1: dynamic logic circuit

3. Body Biasing

Body bias involves connecting the transistor bodies to a bias network in the circuit layout rather than to power or ground. The body bias can be supplied from an external (off-chip) source or an internal (on-chip) source.

Body biasing is a method of improving energy/efficiency, by reclaiming performance lost to margins due to variations. After fabrication, the threshold voltage (*VTH*) of transistors can be modulated by changing the body-to-source voltage.

3.1. BODY BIASING TECHNIQES

In order to enhance the performance of the circuit, various body biasing techniques are used. The substrate of the MOS transistors is connected in six different ways. Six body biasing schemes for the evaluation networks are shown below.

1. The substrate of NMOS is connected to clock and the substrate of PMOS is connected to supply Voltage V_{DD} (SB1).It is shown in figure 2(a).

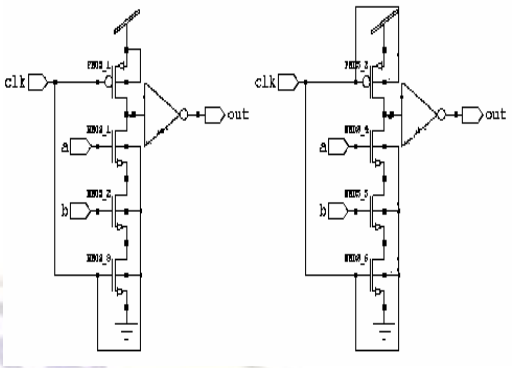
2. The substrate of NMOS and PMOS is connected to clock (SB2). It is shown in figure 2(b).

3. The substrate of NMOS is connected to supply voltage VDD and the substrate of PMOS is connected to clock (SB3). It is shown in figure 3(a).

4. The substrate of NMOS is connected to supply voltage VDD and the substrate of PMOS is connected to Ground (SB4). It is shown in figure 3(b).

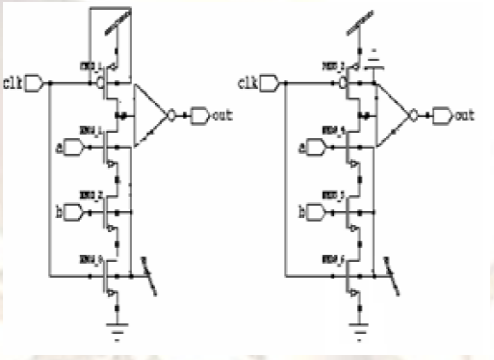
5. The substrate of NMOS and PMOS both connected to supply voltage VDD (SB5). It is shown in figure 4(a).

6. The substrate of NMOS is connected to its source terminal and the substrate of PMOS is connected to clock (SB6). It is shown in figure 4(b).



a b

Fig. 2.(a)SB1,(b)SB2



a

b

Fig.3(a) SB3,(b) SB4

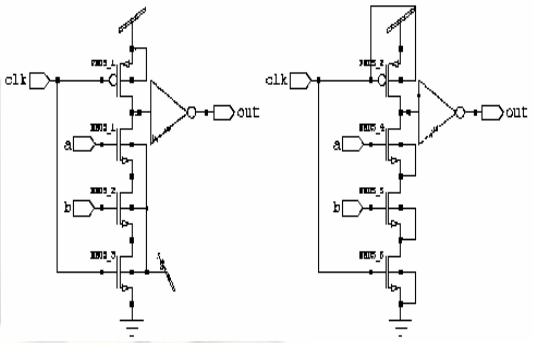


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Fig.4(a) SB5,(b) SB6

3.2 ENERGY/EFFICIENCY OF BODY BIASING

Body biasing was proposed as a means of improving energy/efficiency, and has been implemented in a wide range of chips. After fabrication, the threshold voltage (*VTH*) of transistors can be modulated by changing the body-to-source voltage. In bulk MOSFETs, the *VTH* is given by

$$V_{TH} = V_{TH_0} + \gamma \left(\sqrt{|2\Phi_F - V_{BS}|} - \sqrt{|2\Phi_F|} \right)$$ Here *VTH*0 is the device threshold voltage with no body bias

applied, $2\Phi F$ is the surface potential at strong inversion, and γ is the body effect coefficient[7]-[9].

4. Design Of Adders With Body Biasing

This section presents the basic construction and simulation of primitive gates and adders. Here we are using Proposed SB4 biasing, in which the substrate of NMOS is connected to its source terminal and the substrate of PMOS is connected to its Ground terminal. Shows minimum power consumption, delay and Power delay product. The designs are tested and compared at 65 nm technology.

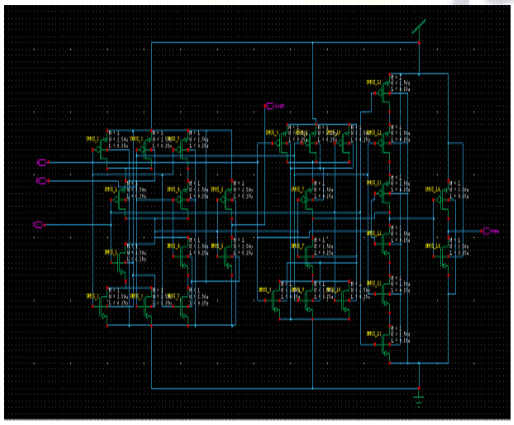
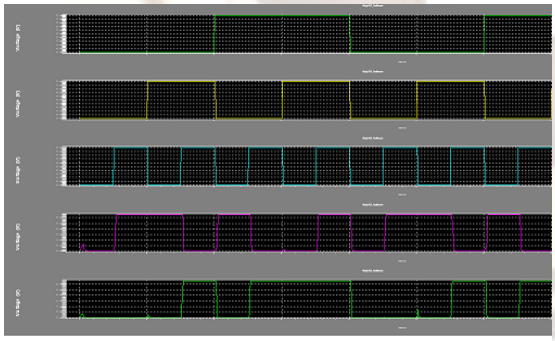


Fig.3: full adder schematic diagram

Figure.3 represents the schematic for full adder with body biasing. Here we are using SB4 biasing technique.



Fg.4: Waveform full adder

Figure.4 represents the output wave form for full adder with body biasing circuit, which gives minimum delay and power dissipation compared to conventional adder.

5. Design Of 8-Bit Multiplier & Comparision

5.1 BINARY MULTIPLIER

In the binary number system the digits, called bits, are limited to the set [0, 11]. The result of multiplying any binary number by a single binary bit is either 0, or the original number. This makes forming the intermediate partial-products simple and efficient. Summing these partial-products is the time consuming task for binary multipliers.

5.2 ARRAY MULTIPLIERS

Binary multiplication of positive operands can be implemented in a combinational two dimensional logic array. A 4X4 array multiplier is shown in figure 1. The functions of M0, M1, M2, and M4 are also shown in figure 1. X3X2X1X0 is the 4 bit multiplicand and Y3Y2Y1Y0 is the 4 bit multiplier. The main component in each cell is a full adder. The AND gate in each cell determines whether a multiplicand bit, Xj is added to the incoming partial product bit based on the value of the multiplier bit Yi. Each row adds the multiplicand (appropriately shifted).

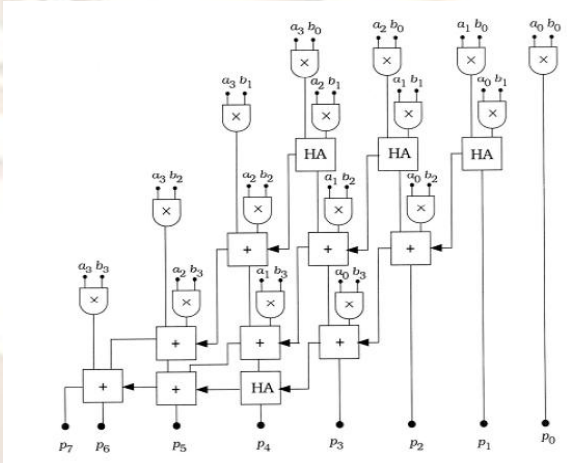


Fig.5. Array multiplier

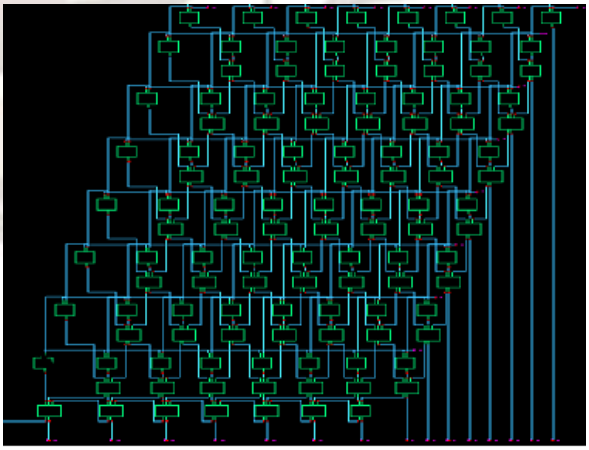


Fig.6.Schematic for 8- bit multiplier using body biasing.

The above figure represents the schematic for an 8 bit multiplier with body biasing. In which the entire circuit is designed with body biasing and, adder blocks

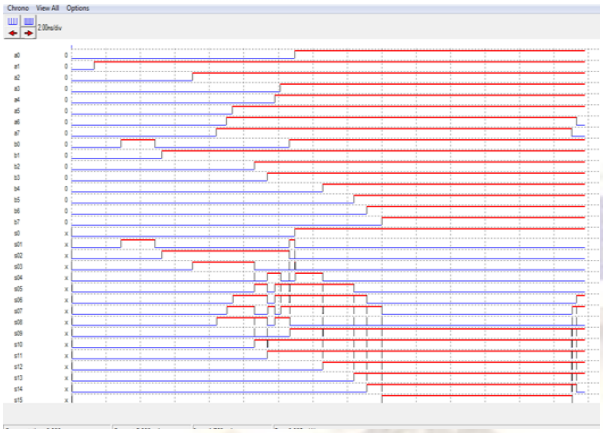


Fig.7.wave form for 8 bit multiplier using body biasing

The above shown figure represents an output wave form for 8 bit multiplier. In the figure A0-A7 and B0-B7 are represented as input signals corresponding to this the output signals are represented as S0-S15.

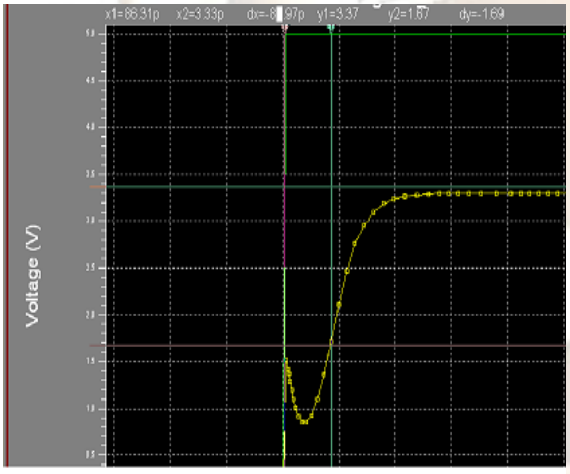


Fig.8.Delay of 8 bit multiplier using body biasing

The above shown figure represents the delay calculation for an 8 bit multiplier with body biasing circuit. Delay calculation is done for signals those having maximum signal levels. From this we calculated the rise and fall delays which are tabulated in below tabular form.

Comparison between conventional CMOS logic and body biasing logic circuits

Topology	**Rise delay** ps	**Fall delay** ps	**Power dissipation µW**
AND	8.35	6.88	0.36
HALF ADDER	12.45	11.53	0.026
FULL ADDER	17.00	14.67	0.44
8 BIT MULTIPLIER	4.7	3.51	2.79

Table1 Power dissipation and delay of body biasing circuits

Topology Topology	**Rise delay** ps	**Fall delay** ps	**Power dissipation µW**
AND	21.07	19.45	1.27
HALF ADDER	29.37	23.64	1.87
FULL ADDER	23.65	22.53	2.65
8 BIT MULTIPLIER	13.45	13.21	5.13

Table2 Power dissipation and delay of conventional CMOS circuits

6. Conclusion

In this paper, an exhaustive analysis and design methodology for commonly used high-speed primitive gates, adder and multiplier circuits using body biasing technique is implemented in 65-nm CMOS technologies. The goal is to reduce the power consumption. So we are designed the circuits with body biasing. Hence the power consumption for the above 8-bit multiplier design using body biasing technique is 45.61% less compared to the conventional static CMOS logic circuit.

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