Power Saving in CMOS Using a Half-Swing Clock Scheme

Deepti Kachhara*, Rajendra Prasad**, Ruchi Agarwal***, Mukesh Maheshwari****

*Department of Electronics and Communication, Mewar University, Chittorgarh-312901(Rajasthan), India
**School of Electronics Engineering, KIIT University, Bhubaneswar, India
***Department of Electronics and Communication, Mewar University, Chittorgarh-312901(Rajasthan), India
**** Department of Electronics and Communication, Mewar University, Chittorgarh-312901(Rajasthan), India

ABSTRACT
Reducing power consumption without sacrificing processing speed is a critical factor in VLSI design, especially for hand-held devices. In CMOS circuits, dynamic power consumption is proportional to the transition frequency, capacitance, and square of supply voltage. Consequentially, reducing supply voltage provides significant power savings at the expense of speed. The clocking circuitry generally consumes a large portion of the total power in digital VLSI's. So clock power can be reduced using half swing of clock scheme. In Digital circuits by using double-edge triggered flip flops (DETFFs), the clock frequency can be significantly reduced ideally, in half while preserving the rate of data processing. Using lower clock frequency may translate into considerable power savings for the clocked portions of a circuit, including the clock distribution network and flip-flops.

Keywords – Clock, edge triggered flip-flop, half swing, power, T-SPICE tool.

1. INTRODUCTION
In recent years major concerns of VLSI designers were area, performance, cost and reliability, and power. Power is being most important factor of the in VLSI design. These factors have been the remarkable for success and growth of the systems which demand high-speed and complex functionality with low power consumption.

In an increasing market of portable applications battery capacity limits time of operation. Higher speed and complexity increase power dissipation of stationary applications so cooling requirements become more expensive. These are the few factors which approach towards low power.

Due to the large capacitance and the high switching activity, the clock system dissipates a large portion of the total power (18-40% in [1]. Using a half-swing clock scheme is an efficient way of power reduction.

This paper meanly deals with the half swing clock scheme. First explain the half swing clock driver [2], which provides clock signals to the latches. The next session

discuss the behaviour of latches and edge triggered flip-flop with half swing clock scheme. Investigation of the latch behaviour at half-swing clock shows the suitability of C^2MOS latches. The increased latch delay is compensated by resizing of latch transistor. The final session will discuss

the result, which shows using double edge triggered flip-flop with half swing clock reduces power.

2. HALF-SWING CLOCK SCHEME
The half-swing clock scheme, in which all the clock signal swings are reduced to half of the VLSI supply voltage. This technology allows us to reduce power consumption of clocking circuitry. The key to the clocking scheme is the concept that the voltage swing is reduced only for clock circuitry, but is retained for all other circuits in the chip. This results in significant power reduction with minimal speed degradation.
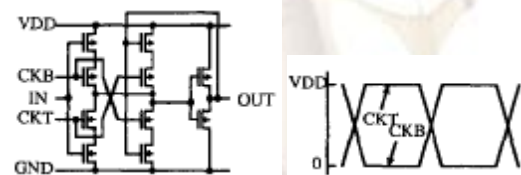
(a)
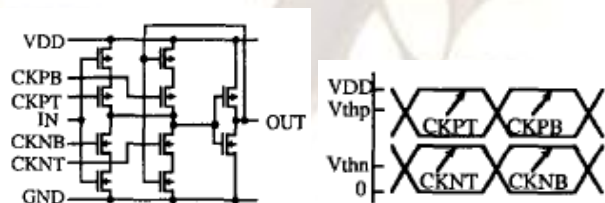
(b)

Fig.1 Concept of half-swing clocking scheme.

(a) Conventional clocking scheme. (b) Half-swing clocking scheme.

Fig.1 shows the half-swing clocking scheme compared with a conventional scheme. In Fig.1 (a), a conventional latch is gated by two full-swing clocks. To decrease the clocking power, the voltage swing of the clock is reduced to half V_{DD} ('V_{DD}' represents the VLSI supply voltage). The proposed scheme, as shown in Fig.1 (b), uses two separate clock signals for NMOS and PMOS transistors, respectively. The clock for NMOS's swings from zero to half V_{DD}, and the clock for PMOS's swings from V_{DD} to half V_{DD}. The power consumed by clocking circuitry is decreased to 25% of conventional clocking circuitry.

In latch based design, non overlapping two phase clock system is used. C²MOS latches and transmission–gates (TMG) require two pairs of complementary clock phases $\Phi_{1,f}/\overline{\Phi}_{1,f}$ and $\Phi_{2,f}/\overline{\Phi}_{2,f}$. $\Phi_{1,f}$ and $\Phi_{2,f}$ controls the NMOS gates, whereas $\overline{\Phi}_{1,f}$ and $\overline{\Phi}_{2,f}$ are connected to PMOS gates. Fig. 2 shows the two complementary full swing phases and a C²MOS latch.
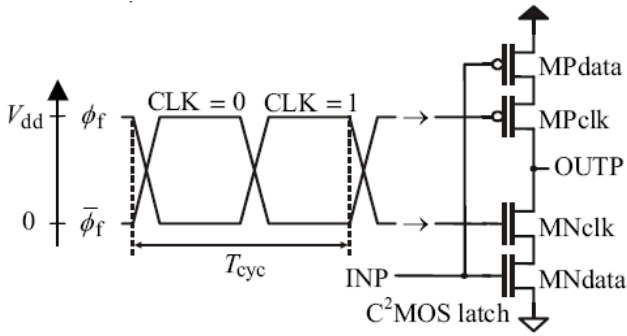

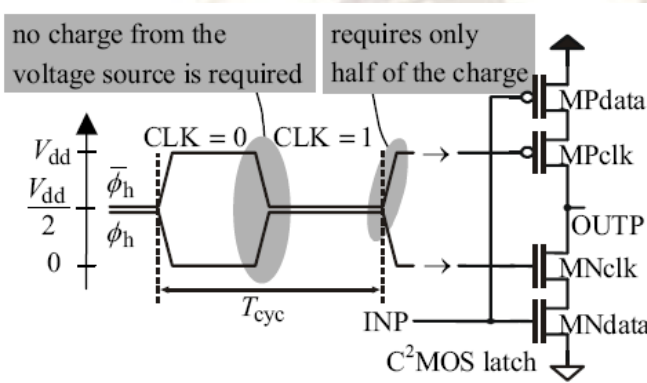**Fig. 2 Complementary full swing clocking.**

Fig. 3 Complementary half swing clocking.

As there is four phases of clock and the energy consumption per clock period is determined by two full-swing transitions. Thus two discharging edges does not require any charge from voltage source and two rising edges of clock require charge from voltage source. The power consumed by the clock is given by:

$$P_{clk,f} = C_{clk,f} \cdot V_{dd}^2 \cdot f_{clk} \qquad (1)$$

Where $C_{clk,f}$ is the total capacitance of the four clock phases, V_{dd} is power supply voltage and f_{clk} is the switching frequency of clock. Fig.3 shows two complementary phases $\Phi_h / \overline{\Phi}_h$ of half swing clocking scheme. In the low to high transition (LH) of Φ_h can be obtained by connecting it to $\overline{\Phi}_h$ [5], which does not require any charge from the voltage source. The energy dissipating by $\overline{\Phi}_h$ is used by Φ_h . So shorting these two complementary phases no energy requires from voltage source. The only energy consuming state is low to high transition of $\overline{\Phi}_h$. Thus a power reduction to 25% with respect to (1) can be achieved:

$$P_{clk,h} = \frac{1}{4} C_{clk,h} \cdot V_{dd}^2 \cdot f_{clk} \qquad (2)$$

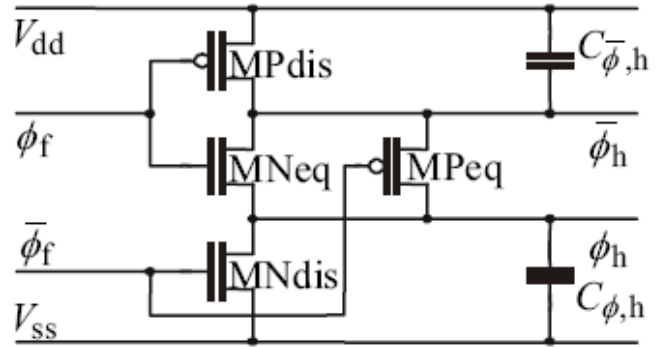Half swing clock drivers are suggested in [2] and [5] is shown in fig. 2.6.

Fig.4 Half-swing clock driver

This clock driver generated the half swing clock and half V_{dd} voltage. When voltage at phase of full swing clock $V_{\Phi f}$ = 0, transistor MPeq and MNeq are off, Φ_h and $\overline{\Phi}_h$ are discharge by MNdis and MPdis to V_{ss} = 0 and V_{dd} respectively. When $V_{\Phi f}$ =V_{dd}, these MNdis and MPdis are off and MPeq and MNeq are short circuit Φ_h and $\overline{\Phi}_h$, which met at potential V_{eq}:

$$V_{eq} = \frac{C_{\overline{\Phi}h}}{C_{\Phi,h}+C_{\overline{\Phi}h}} V_{dd} \qquad (3)$$

With $C_{\overline{\Phi}h} = C_{\Phi,h}$,V_{eq} become equal to $V_{dd}/2$.

2.1 BEHAVIOUR OF LATCH WITH HALF-SWING CLOCK

Reduced clock voltage swing leads to reduced drain current causes longer latch delay. Resizing (increasing) channel width of latch transistors is necessary. The resizing- factor (RF) of the transistors is determined by the timing of the logic path following the latch. The output edge has to be restored only if there is long path with critical timing. With only shorter paths at the latch output, a longer latch delay may be permitted and RF can be smaller with two consecutive latches, resizing of the first is not necessary.
Depending on the timing when a transition occurs at a latch input, the clock-to–output delay or the input-to-output delay has to be considered. In order to avoid RF becoming too large, a 0.1ns latch delay is tolerated at half swing clock. The use transmission gate produces a kink at the output edge hence not suitable for half swing clock.

3. EDGE TRIGGERED FLIP FLOP

In a synchronous system, operations and data sequences take place with a fixed and predetermined time relationship. The timing of computations is controlled by flip-flops and latches together with a global clock. Flip-flops and latches are clocked storage elements, which store values applied to their inputs. They are classed according to their behavior during the clock phases. A flip-flop is edge triggered if it captures its input and propagates it to the output at a clock edge (rising or falling), while keeps the output constant at any other time. The design of these clocked storage elements are highly depended on the clocking strategy and circuit topology.

3.1 SINGLE AND DOUBLE EDGE TRIGGERED FLIP FLOP

Both double-edges triggered (DET) and single-edge triggered (SET) flip-flops are edge-sensitive devices, that is, data storage in these flip-flops occurs at specific edges of the clock signal. During each clock period, single edge triggered flip-flops are triggered by and store data at only one—either the *rising* or the *falling*—edge of the clock signal. Double-edge triggered flip-flops sample the input data at both the rising and the falling edges of the clock signal during each period of the clock signal.
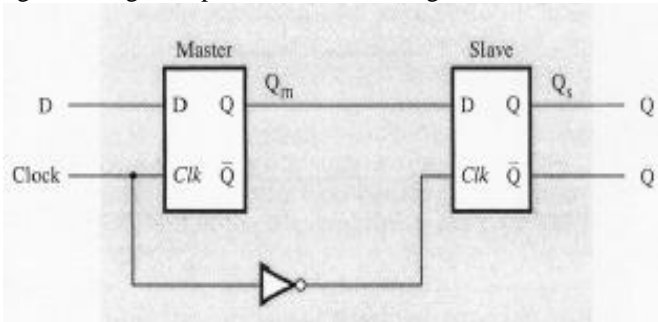
Fig.5 Single-edge triggered (SET) flip-flops

A classical double-edge triggered flip-flop in CMOS technology can be implemented as shown in Fig. 6. In this design, two opposite polarity level-sensitive latches are used. Specifically, D_1 and D_2 are a positive level sensitive and a negative level-sensitive latch, respectively, and, the block labeled $M1$ is a multiplexer described by the equation:

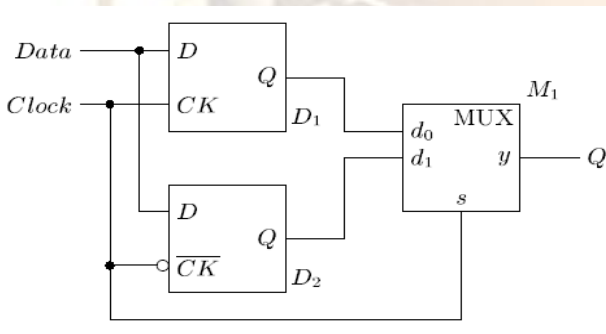$$y = d_0 \bar{s} + d_1 S \qquad (4)$$

Fig. 6 Double edge triggered (DET) flip-flops

The fig.7 shown design of Single edge triggered flip-flop (SETFF) and double edge triggered flip-flop (DETFF) with transmission gate latch [7]. Since the clock signal of the DETFF is running at half the frequency, there is also a power saving in the clock distribution network outside the flip flops relative to SETF. As the transmission gate latch output with half swing is kink so this DETFF is implemented with C^{2}MOS latch.
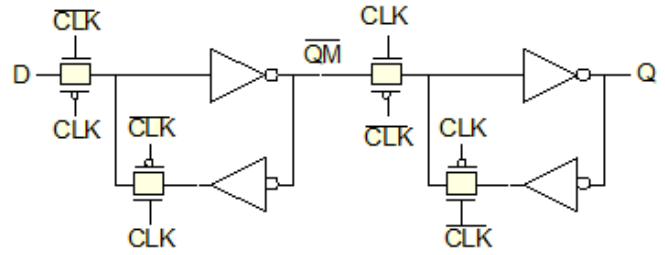
(a)
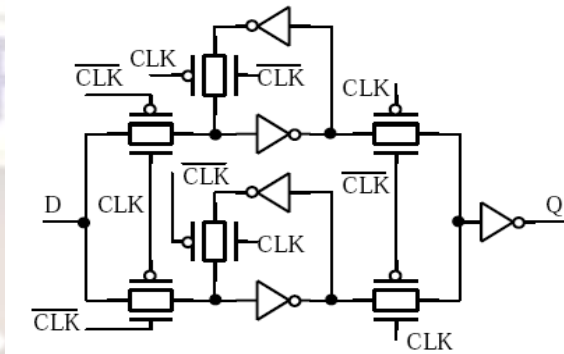
(b)

Fig.7 The Design of CMOS flip flop (a) Single edge triggered flip flop (b) Double edge triggered flip flop

4. SIMULATION RESULTS

For this Technology used in it is 180nm and simulated with TSPICE in Tanner EDA Tool. Simulation of half-swing clock driver shown in fig.8, the upper waveform of half-swing clock used for PMOS and lower waveform is used for NMOS. The resizing of transistor is randomly changed to achieve this half swing clock. The width of PMOS is 9μm and MNeq is 2μm and MNdis is 5μm.The value of capacitance $C_{\bar{\Phi}h} = 1$pF and $C_{\Phi,h}=0.7$pF.
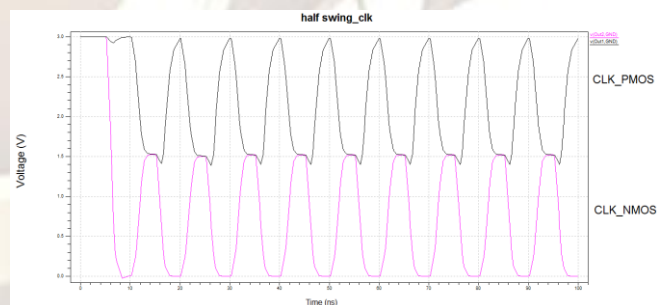

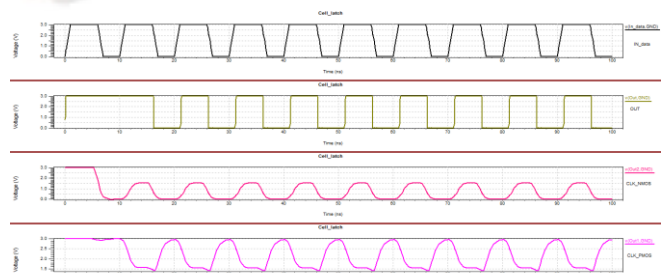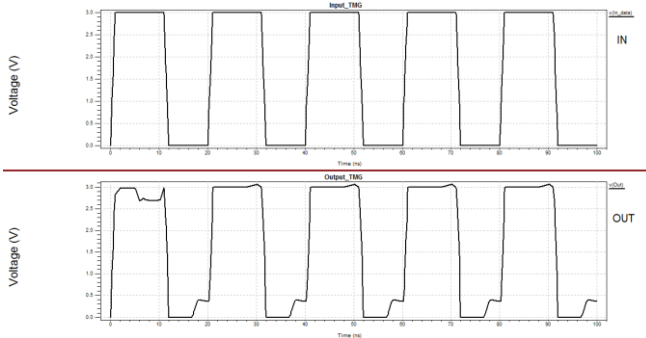**Fig.8 Simulation result for half-swing clock driver**

**Fig.9 Simulation result for C^{2}MOS latch for half-swing clock**

C²MOS latch waveform is shown in fig.9.The resizing of latch transistor is necessary to restore the shape and timing of output edge. The delay observed for input to output for low to high transition is T_{PLH} = 603.17ps, and high to low transition T_{PHL} = 18.85ps, which is very low.


Fig.10 Simulation result for Transmission gate latch for half-swing clock.

The transmission gate (TMG) latch behavior with half swing clock is shown in fig.10. The output of TMG latch is kink in the output edge (can be minimized by fast input transitions). So transmission gate latch is less suitable with half swing clocking scheme.
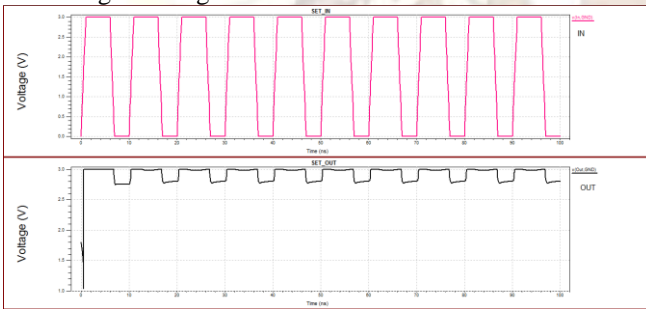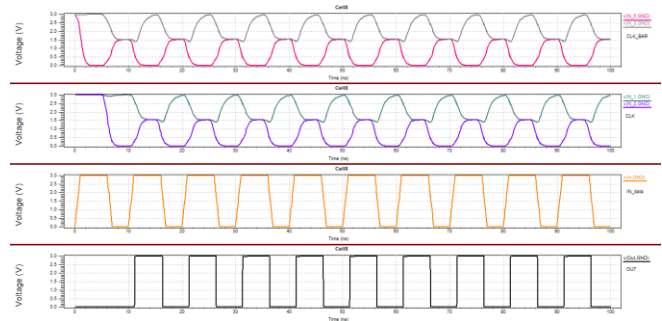

Fig. 11 Simulation of single edge triggered flip-flop using transmission latch with half swing clock

The waveform shown in fig.11 is SET using transmission gate latch for half swing clock .As output waveform is not accurate so as previously say that the transmission gate latch is not suitable for half swing clocking scheme.
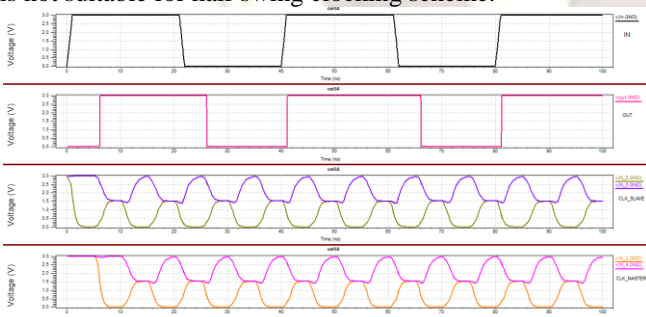
Fig.12 Simulation of single edge triggered flip flop using C²MOS latch with half-swing clock

The fig.12 shown output waveform for SET Flip Flop using C²MOS latch. The width of all transistors is equal to 2.5µm. The waveform of DET flip flop with C²MOS latch using half swing clock is shown in fig.13 the width of transistor is also 2.5µm.

Fig.13 Simulation result for double edge triggered flip-flop using C²MOS latch with half swing clock

The power and delay calculated for single edge triggered and double edge triggered flip-flop with half-swing clock scheme is compared in and show that the power is reduced about 50% when double edge trigged flip-flop is used with half swing clock. The power is calculated using T-SPICE in Tanner EDA software.

Table.1 Comparison between edge triggered flip-flop for half-swing clock

Flip Flop	Clock swing	Power(watt)	Delay(rise) in sec.
DETFF	Half swing	1.00694×10^{-3}	674.07p
SETFF	Half swing	1.964×10^{-3}	840.96p

5. CONCLUSION

The proposed design is an attempt to design a low power, half-swing clock double edge triggered flip-flop. Clock and clock circuitry generally consume more power, so Half-swing clock system reduces clock power.

Clocked C²MOS latches suitable for half-swing clock. But Transmission-gates latch output is kinked with half swing clock.

Double edge triggered flip flop using half swing clock results in power reduction. Double edge triggered flip flop responds to both clock edges, the clock frequency can be halved to achieve the same computation throughput compared to single edge triggered flip flop. This results in overall system power reduction because clock distribution is a major source of power consumption in a synchronous computation system. It has been shown that the usage of DETFFs in VLSI systems is beneficial in low power, low voltage applications and high speed applications.

REFERENCES
[1] Hirotsugu Kojima, Satoshi Tanaka and Katsuro Sasaki "Half-Swing Clocking Scheme for 75% Power Saving in Clocking Circuitry" *IEEE solid state circuits, vol. 30, no. 4, April 1995.*

[2] Loew, M.; Pfleiderer, H.-J.; Bruels, N. "Power Saving in CMOS using Half swing clocking scheme", *Solid-State Circuits Conference, 2001 .ESSCIRC 2001.*

[3] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits, vol. 27, no. 4, pp. 473484, Apr. 1992.*

[4] Neil Weste, Devid Harris, Ayan Banerjee *"CMOS VLSI Design"* (Pearson Education)

[5] E.De Man, M. Schoebihger: "Power Dissipation in the Clock System of highly pipelined ULSI CMOS Circuits", Proc. Int'l Workshop on Low-Power Design, April 1994

[6] Pedram, M. Qing Wu and Xunwei Wu "A New Design for Double Edge Triggered Flip-flops" *Design Automation Conference 1998. Proceedings of the ASP-DAC '98.*

[7] Gary Yeap "*Practical Low Power Digital Design*" (Kluwar Academic Publications).