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A Low Power Delay Buffer Using Gated Driver Tree

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Abstract— This project presents circuit design of a low-power delay buffer. The proposed delay buffer uses several new techniques to reduce its power consumption. Since delay buffers are accessed sequentially, it adopts a ring-counter addressing scheme. In the ring counter, double-edge-triggered (DET) flip-flops are utilized to reduce the operating frequency by half and the C-element gated-clock strategy is proposed. A novel gated-clock-driver tree is then applied to further reduce the activity along the clock distribution network. Moreover, the gated-driver-tree idea is also employed in the input and output ports of the memory block to decrease their loading, thus saving even more power.

Keywords-FIFO, gated clock, ring counter

I. INTRODUCTION

The skyrocketing increasing transistor count and circuit density of modern very large scale integrated (VLSI) circuits have made them extremely difficult and expensive to test comprehensively. The DFT method In a digital processing chip of mobile communications, the delay buffer takes up a large portion of the circuit layout. If the power consumption of the delay buffer could be reduced significantly, the overall power consumption of the digital processing chip could be reduced significantly as well. On the other hand, as these chips are working at even higher operation frequencies, a new, low-power delay buffer should be operable under high frequencies. Within parentheses, following the example. Some components, such as multi-leveled equations, graphics, and tables are not prescribed, although the various table text styles are provided. The formatter will need to create these components, incorporating the applicable criteria that follow.

II. EASE OF USE

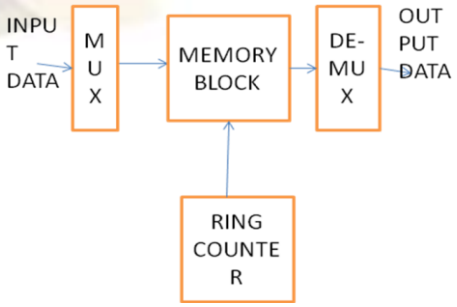
A. MEMORY ORGANISATION:

Memory organization is two-fold. First we discuss the hardware (physical) organization, then the internal architecture. The type of computer and its size do not reflect the type of memories that the computer uses. Some computers have a mixture of memory types. For example, they may use some type of magnetic memory (core or film) and also a semiconductor memory (static or dynamic). They also have a read-only memory which is usually a part of the CPU. Memory in a computer can vary from one or more modules to one or more pcb's, depending on the computer type. The larger mainframe computers use the modular arrangement, multiple modules, to make up their memories. Whereas, minicomputers and microcomputers use chassis or assemblies, cages or racks, and motherboard or backplane arrangements.

B. *PHYSICAL FERATURES:*

The first defining feature of RAM is form factor. RAM modules can be in compact SO-DIMM form for space constrained applications like laptops, printers, embedded computers, and small form factor computers, and in DIMM format, which is used in most desktops.The other physical characteristic determine with by physical examination are the number of memory chips, and whether both sides of the memory "stick" are populated.

.(A) PREVIOUS TECHNIQUE



Generally, multi inputs are fed to multiplexer and at a time single input is given to the memory block depends on selection line. In our project we are creating 256 rows and 8 columns RAM. Random-access memory (RAM) is a form of computer data storage. Today, it takes the form of integrated circuits that allow stored data to be accessed in any order (that is, at random). "Random" refers to the idea that any piece of data can be returned in a constant time, regardless of its physical location and whether it is related to the previous piece of data. A ring counter is a type of counter composed of a circular shift register. The output of the last shift register is fed to the input of the first register. There are two types of ring counters:

1.A straight ring counter or Over beck counter connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring.

2.A twisted ring counter (also called Johnson counter or Moebius counter) connects the complement of the output of the last shift register to its input and circulates a stream of one's followed by zeros around the ring.

(B) PRESENT TECHNIQUE

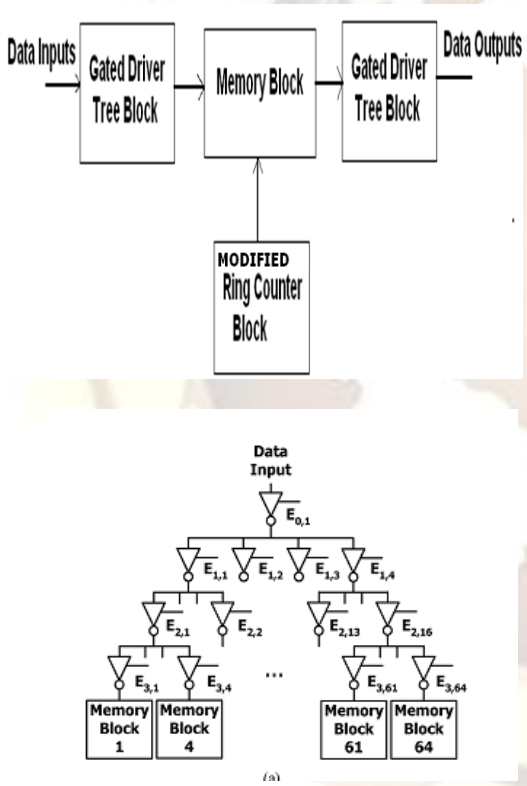


Fig: Gated Driver Tree

Mainly, it is used to synchronize the input data with memory. And it is used to eliminate loading effect.Derived from the same clock gating signals of the blocks that they drive. Thus, in a quad-tree clock distribution network, the "gate" signal of the th gate driver at the th level (CKE) should be asserted when the active DET flip-flop .

DET :(Double edge triggered flip-flops: double-edge-triggered (DET) flip-flops are utilized to reduce the operating frequency by half The logic construction of a double-edge-triggered (DET) flip-flop, which can receive input signal at two levels the clock, is analyzed and a new circuit design of CMOS DET In this paper, we propose to use double-edge-triggered (DET) flip-flops instead of traditional DFFs in the ring counter to halve the operating clock frequency. Double edge-triggered flipflops are becoming a popular technique for low-power designs since they effectively enable a halving of the clock frequency. Instead of clocked RS flip-flop we are using clock less C-gated elements. And, instead of single edge trigger flip-flop, we are going to use Double edge triggered flip-flops.

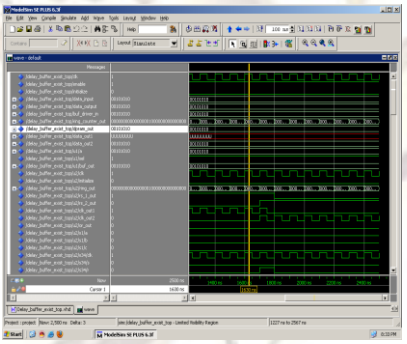
(C) APPLICATIONS AND ADVANTAGES

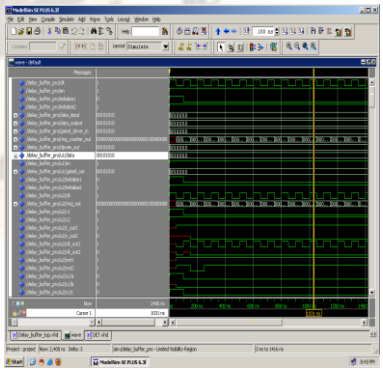
1. D.S.P processors
2. FPGA
3. SYSTEM ALU
4. Low power consumption
5. Less loading effect
6. Occupies less area to implement practically.

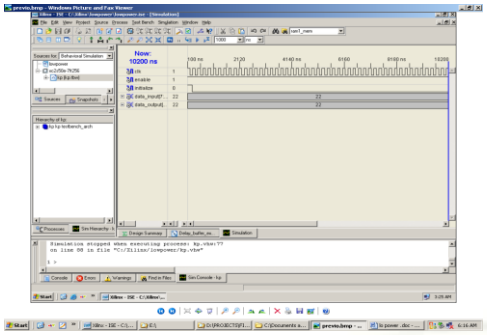
(D) Conclusion

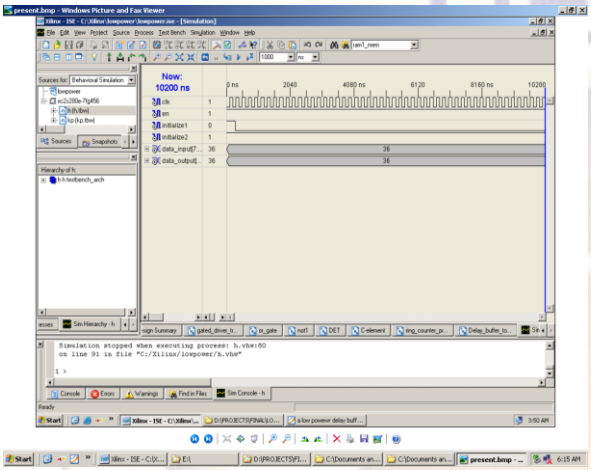
Finally, I was conclude in this paper, I have developed a memory with low power and area delay buffer by using VHDL coding and related synthesis reports.

(E) RESULTS









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