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# Design of Compact Transformer-type Power Combiner for Watt-level PA in CMOS Technology

**Dariush Tavakolifar*, Javad Javidan****
*Department of Electrical Engineering, East Tehran Branch, IAU, Tehran, Iran
**Technical Engineering Department, University of Mohaghegh Ardabili, Iran

## ABSTRACT
**This paper presents a compact structure in several transformers layout as a power combiner with high-efficiency and small chip area characteristics using current silicon-based technology. Multi-transformers are composed of several single-turn inductors inside each other to obtain high quality factor because of single-turn inductors and reduce the entire chip area because of compact structure, simultaneously. According to the different topologies of power stage, the performance of power combiners is fully analyzed and optimized for obtaining high efficiency versus physical dimensions. The behavior of the proposed power combiner versus frequency with combining analytical and numerous methods is derived in this study. The proposed power combiner will be benefit in watt-level and fully integrated CMOS power amplifier.**

*Keywords* - **Power Amplifier, Power Combiner, Transformer, Efficiency Optimization**

## I. INTRODUCTION
CMOS technology is one of the best candidates for achieving low cost in high volume and high levels of integration in designing wireless communication systems. Despite intrinsic drawbacks in the implementation of the standard CMOS process such as lossy substrate, low quality factor and low breakdown voltage of active devices, Most of the radio frequency (RF) building blocks have been successfully integrated into CMOS process. Typically, in fully integrated systems, the power amplifiers (PA) and RF switches are mostly implemented in an expensive and different process technology or connected to chip as external component. Therefore the implementation of RF PA and RF switch is a challenging task for CMOS RF integration [1] [2].

In literature, Two broad categories of power combining are introduced, circuit-level and spatial (also referred to as quasi-optical). The circuit-level combiner divides the power from a single input to several amplifiers combined in parallel through the use of transmission lines. These transmission lines may be microstrip, coplanar waveguide (CPW), rectangular waveguide, strip line, etc. Each of these has its own advantage at various frequencies and for various applications. Clearly the microstrip and CPW transmission lines have the greatest advantage in Monolithic Microwave Integrated Circuits (MMICs), due to their ease of integration into such semiconductor processes. It is obvious that, as additional amplifiers are combined, the transmission line lengths and circuit complexity increase. As the line lengths increase to add more devices, the losses accumulate in the circuit, eventually exceeding the gain of the amplifiers being added and nullifying the advantage of the additional amplifiers[3]-[4]. The spatial power combiner does not use transmission lines to divide an input signal to the amplifiers. thus it does not suffer from the gathering of losses in the transmission lines by the addition of more amplifiers. Instead, a signal is radiated from a source and received by an array of parallel amplifying unit cells. Each cell amplifies the signal and then re-radiates it into free space. This, however, creates new design challenges. The overall system size may be large; the design may be complex due to the proximity of amplifying and radiating elements; the dissipation of heat is fundamentally more difficult; and the system may be difficult to model due to its large electrical size[5].

Recently, the implementation of fully integrated high power PA by using transformer-type output networks in realizing power combining and impedance transformation at the same time has been successful effort to overcome process bottlenecks. According to voltage and current combining at the load, power combiners can be categorized as series-combining transformers (SCTs) and parallel-combining transformers (PCTs); a series combiner will sum output voltages and a parallel combiner will sum currents of individual elements. Distributed active transformers (DATs) [2] and Figure 8 transformers [1] whose secondary windings are cascaded are examples of existing series combiner implementations. Parallel combiners have also been reported using interleaved transformers [6], [2], monolithic voltage-boosting parallel-primary transformer [7], lumped-element baluns [8], and external λ/4 networks [9].

Using “slab” inductors because of excellent quality factor to realizing fully integrated transformer has been proposed in [10] and called distributed active transformer (DAT). Because of generic circular geometry of DAT, the power devices are very close to transformer network and there is cross coupling between input and output nodes, therefore strong magnetic coupling between them causing instability for amplifier block [11]. Furthermore, the relatively bulky power combining structure compared to the active device

area primarily determines the total die size, which is not desirable for an efficient cost model [7]. A monolithic voltage-boosting parallel-primary transformer with multiple primary loops interweaved in parallel form and boosting voltage by increasing the turn ratio from primary loop to secondary loop is another proposed power combining [7]. The structure needs DC-feed inductor as the result of asymmetric shape which is not proper for fully integrated design and moving between multi-layers with a single thick metal layer degrading the quality factor of the coils.

A 'figure 8' style layout is proposed in [1]. Single loop inductor because of high Q used in primary side and the transformer secondary side is implemented in alternating orientation. This layout minimizes the effects of internal flux cancellation and extraneous lead inductance connected to transistor. Realizing this structure for watt level power combiner in 1 GHz operating frequency in standard CMOS process requires very large and unacceptable die area. This paper proposed a structure occupying minimum possible area which produces watt level output powers.

The paper is organized as follows. Section II describes the proposed new transformer network as power combiner. Section III presents an analysis of efficiency optimization in proposed architecture and gives simulation results. Section IV illustrates EM-simulation of proposed transformer network. Section V describes power amplifier design and finally section VI gives the conclusion.

## II. PROPOSED TRANSFORMER NETWORK AS POWER COMBINER

On-chip inductors are the largest silicon area consuming device for RFICs and play a crucial role in performance characteristics. The inductor is one of the key elements in RFIC designs. Scalable and accurate characterization of the behavior of spiral inductors is therefore invincible for RFIC designers. Conventional on-chip inductors can be categorized to micro-strip line, single-turn and multi-turn inductors. Micro-strip line inductors have superior quality factor; nonetheless they impose much more constraints in implementation and occupy more area. Negative magnetic coupling and proximity effect significantly reduces the quality factor of a multi-turn inductor and power efficiency of the transformer formed by multi-turn inductors. The multi-turn inductor also suffers from a large parasitic capacitance between adjacent turns that lowers its self-resonant frequency [12] [13]. A compromise between a multi-turn and a micro-strip line inductor is a single-turn inductor. Single-turn or multi-turn spiral inductors occupy much less area and are easy to be laid out compared with micro-strip line inductors. In single-turn inductor, if existing distance between opposite sides is large, negative magnetic coupling will be negligible [13]. Fig. 1 illustrates the physical layout of the proposed transformer networks as

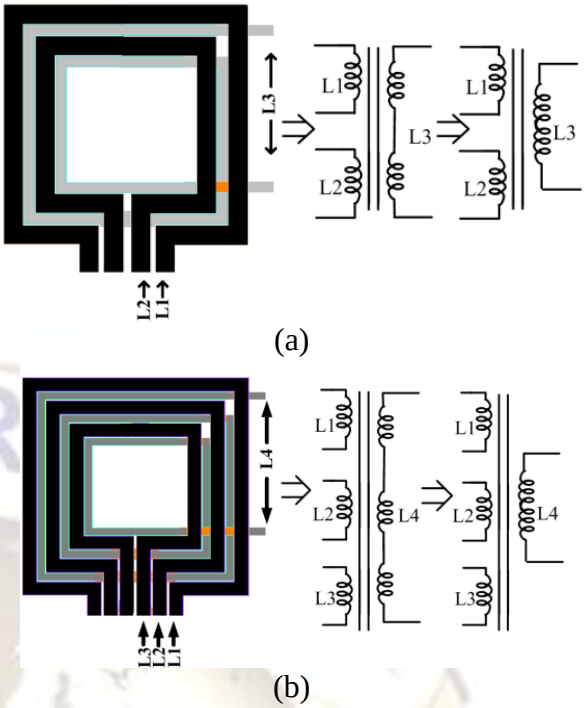



Fig.1. Proposed transformer network and equivalent circuit as power combiner with (a) two transformers (b) three transformer and third transformer is single-turn inductor

power combiner, in which several single-turn primary and secondary loops are employed. The transformers are designed such that the currents of the primary loops are always in the same direction as the neighboring traces to prevent self cancellation. The secondary side inductors are connected in series. As a result, there are several single-turn inductors in the primary side and one multi-turn inductor in the secondary side. Fig.1 and Fig.2 show the different configurations of transformers for PAs that need two, three… transformer as power combiner and this structure will be extended to more number of transformer. Sometimes, for small outer length (OL) or wide width metal, the inner inductance size in the third transformer will be very small, which is not suitable for most applications. To solve this problem, a two-turn inductor for the third transformer (L3) can be used [see Fig. 2(a)]. In order to fully extract the transformer network specifications, e.g., for the transformer shown in Fig. 1(a), one should measure two differential inductors (L1 and L2), one single-ended inductor (L3), two differential–single transformers (L1 & L3 and L2 & L3), and a differential–differential transformer (L1 & L2). All measurements are necessary because of the coupling between inductors. The measurement methodology for the coupling factor was described in [14].

In this design, a standard 0.18-um CMOS process with six aluminum metal layers is used. This process provides the top metal of 2.34 um thickness and the dielectric thickness of 8 um. The space between the two parts of the transformer is 3 um. To draw the layout of the proposed transformers,

there are several design guidelines to follow. First, Magnetic flux must be allowed to pass through the center of the

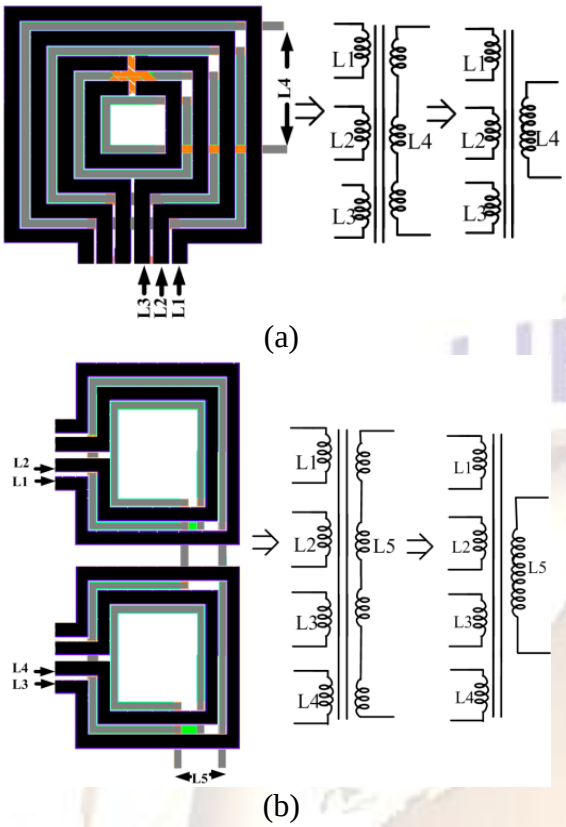



Fig.2. Proposed transformer network and equivalent circuit as power combiner with (a) three transformer and third transformer is two-turn inductor (b) four transformers

winding coil of the inductor. This guarantees that negative mutual coupling between opposite sides of the inductor does not significantly affect the inductance and the Q-factor. Hence a space (inner diameter) of greater than five line width is recommended. And the inner diameter has the influence on Q peak, so we can tune the appropriate inner diameter for our interesting frequency range. Second, adjacent metal traces should belong to different windings, that is, the primary winding does not neighbor the same or different primary windings while the secondary winding does not neighbor the secondary winding itself to decrease self inductance and increase mutual inductance. In addition, the magnetic coupling between adjacent metal lines is maximized by using the minimum spacing (S) between lines that is allowed by the technology. Third, the distance between opposite edges should be as far as possible to suppress negative magnetic coupling, that is, the shape should be close to a regular polygon. Fourth, In order to achieve high quality factor, the output transformer is designed using half-turn inductors and a single-turn metal strip instead of spiral coupled-inductors. The half-turn inductors, forming the primary loop of the transformer, combine output power from a couple of the differential pairs of power transistors. The power is then magnetically coupled to the secondary loop, and delivered to the load. Fifth, the ports of primary windings are aligned at one edge of the layout for easy connection to unit power cells, while the secondary port is positioned at the opposite side to

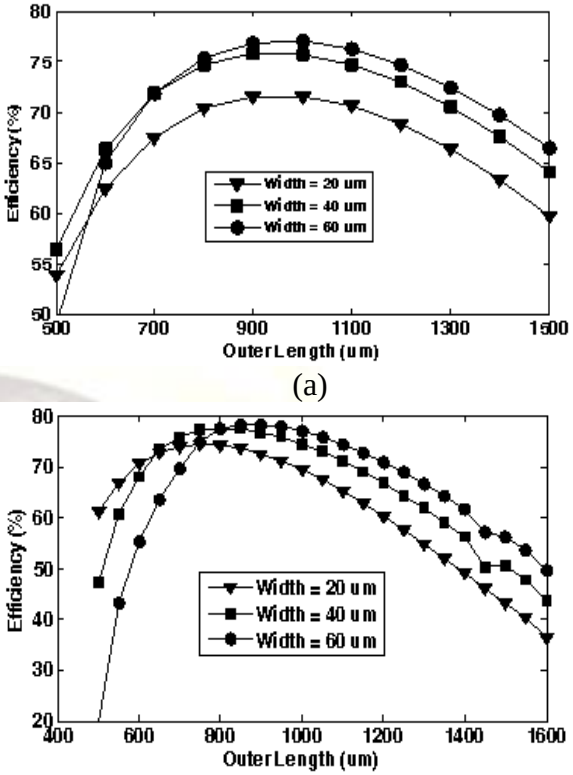


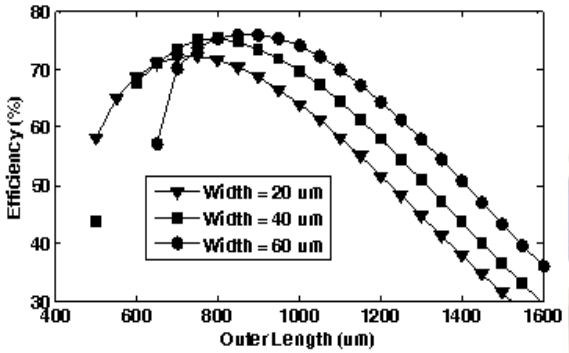

Fig. 3. Efficiency versus OD and metal width for power combiner with (a) two transformers or Fig. 1a (b) three transformers and third transformer is single-turn inductor or Fig.1b

maximize the distance between the input and output. Considering Figs. 1and Figs. 2, there are several different transformers that should be optimized in order to achieve the maximum efficiency. Physical specifications such as the outer length (OL), the width of the metal traces and the spacing between them are the key design parameters to obtain the optimum result. According to these parameters, in next section the optimization process will be explained in detail.

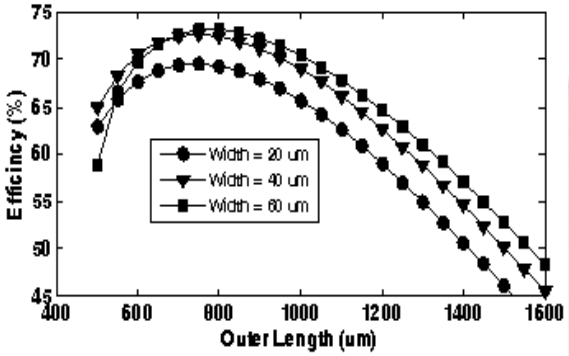
## III. EFFICIENCY OPTIMIZATION OF THE PROPOSED STRUCTURE

The complete electrical behavior of a monolithic integrated lumped inductor and transformer cannot be accurately predicted from closed-form equations. In the distributed model of a transformer, each pair of segments where one forms the primary coil and other forms the secondary coil of the transformer is modeled and they are cascaded depending on the number of turns in the spirals to obtain a distributed model. Even though the distributed model accurately models the transformer behavior, it becomes difficult to incorporate it in circuit simulations and hence a lumped-element model

[15] of the transformer is preferable. An alternative for design and optimization is a lumped-element equivalent circuit. Lumped-element approximation of the transformer is valid for narrow band frequency range. A good rule of thumb for lumped element approximation to be valid would be that extension of the structure is less than λ/10 at any




(a)



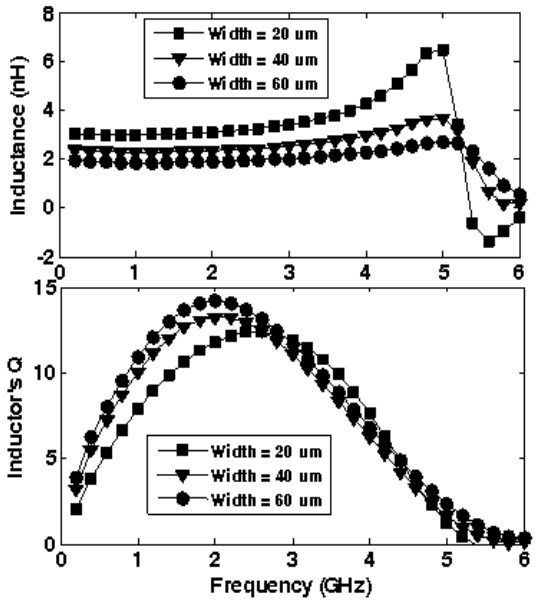

(b)

Fig. 4. Efficiency versus OD and metal width for power combiner with (a) three transformers and third transformer is two-turn inductor or Fig.2a (b) four transformers or Fig.2b

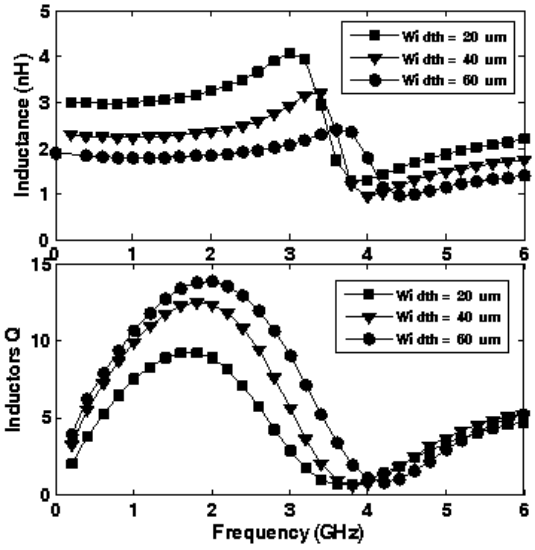
frequency. The aim of precise and fast transient analysis of RF circuits using monolithic transformers was reached with a compact lumped low order model. The complexity of this model is low enough and the precision is high enough to perform fast and accurate analysis of the integrated circuits. The most used model for spiral inductors is the pi-model. Inductors are generally simulated with electro-magnetic (EM) simulators, which can compute the scattering (S-) parameters of the structure [16].

From the S-parameters of the EM-simulated inductor, we can calculate the admittance (Y-) parameters, from which the general PI network can be derived. Several transformer layouts should be simulated in ADS Momentum to find a design which has good coupling and minimal loss. To model the transformer in Momentum, the substrate, oxide layers and all used metal layers must be modeled based on the data provided by the foundry. The iterations included changes to trace widths and overall dimension.

Designers usually take advantage of EM simulators that are highly accurate but also very time-consuming and thus more suitable for design verification rather than optimization. To this aim, simple lumped scalable models are largely employed. Some analytical approaches and closed-form expressions for all the lumped elements and especially for the inductance calculation based on the Greenhouse method, which is accurate enough and suitable for simple lumped modelling were published in last few years [17]. To achieve fast result and to maximize power efficiency or minimize power loss, we obtain physical dimensions using closed-




(a)




(b)

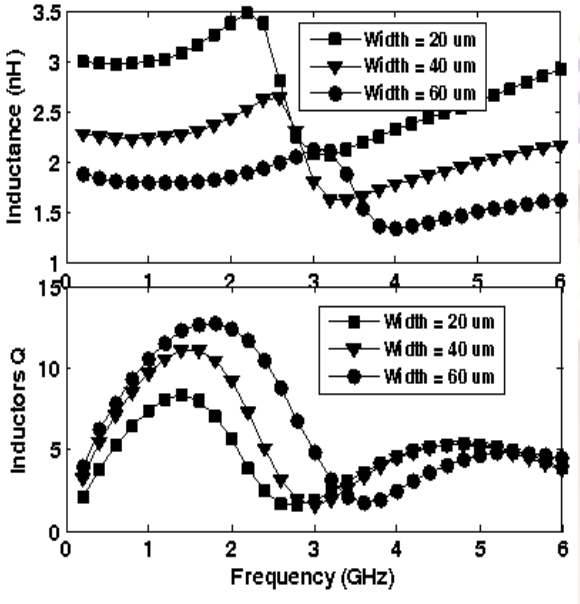
Fig. 5. Inductance and Q-factor of the proposed network with different metal width for power combiner with (a) two transformer or Fig.1a (b) three transformer and third transformer is single-turn inductor or Fig.1b

form expressions in MATLAB. According to extracted physical dimensions, EM simulator will be used to extract accurate pi-model components. For several different transformers as power combiner, writing the power efficiency equation for whole combiner and optimizing its value is necessary. The power efficiency of the matching

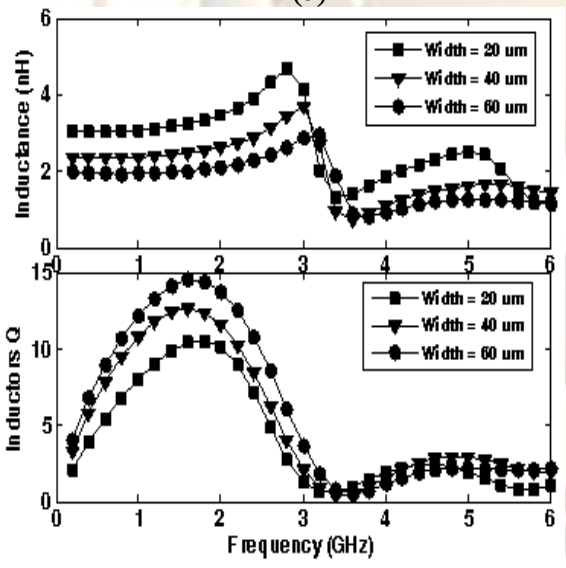
network can be calculated as the ratio between the power delivered to the load and power delivered into the network:

$$\eta = \frac{R_{eq} I_{out}^2}{(R_{eq} + R_{out}) I_{out}^2 + \sum R_i I_i^2} \quad (1)$$

Where $R_i$ is the series resistance of the ith inductor in the primary side. $R_{out}$ and $R_{eq}$ are inductor resistance in the secondary side and load resistance, respectively. $I_i$ and $I_{out}$ are ith inductor current and output current, respectively.
According to the classified topologies for power stages




(a)




(b)

Fig. 6. Inductance and Q-factor of the proposed network with different metal width for power combiner with (a) three transformer and third transformer is two-turn inductor or Fig.2a (b) four transformer or Fig.2b

connected to power combiner by author in [18], the current and voltage relations for N transformers connected series in secondary sides can be represented by:

$$Vin(i) - \frac{I_i}{C_i \omega j} = (R_i + L_i \omega j) I_i + \sum_{j \neq i} M_{ij} \omega j I_j - M_{io} \omega j I_{out} \quad (2)$$

i=1,2,…N, the number of inductor in the primary side

$$(\sum_{i=1}^{N} M_{io} I_i) \omega j = (R_{eq} + R_{out}) I_{out} \quad \text{Secondary side} \quad (3)$$

Also for some topologies, the equations can be represented by:

$$Iin_i - I_i = C_i \omega j [(R_i + L_i \omega j) I_i + \sum_{i \neq j} M_{ij} \omega j I_j - M_{io} \omega j I_{out}] \quad (4)$$

i=1, 2,…,N, the number of inductor in the primary side

$$(\sum_{i=1}^{N} M_{io} I_i) \omega j = (R_{eq} + R_{out}) I_{out} \quad \text{Secondary Side} \quad (5)$$

Table 1. Transformer network characteristics of Fig. 1(a)

| | L1(nH) | L2(nH) | L3(nH) | Q1 | Q2 |
|---|---|---|---|---|---|
| TN1 | 3 | 2.7 | 7.5 | 7.8 | 7.4 |
| TN2 | 2.3 | 2 | 6.3 | 10 | 9.9 |
| TN3 | 1.86 | 1.57 | 5.3 | 10.9 | 11.1 |
| | Q3 | K12 | K13 | K23 | |
| TN1 | 9.9 | 0.51 | 0.55 | 0.7 | |
| TN2 | 8.1 | 0.56 | 0.53 | 0.67 | |
| TN3 | 6.8 | 0.56 | 0.5 | 0.65 | |

Table 2. Transformer network characteristics of Fig. 1(b)

| | L1(nH) | L2(nH) | L3(nH) | L4(nH) | Q1 | Q2 | Q3 |
|---|---|---|---|---|---|---|---|
| TN1 | 3 | 2.7 | 2.5 | 13.6 | 7.5 | 6.5 | 6.6 |
| TN2 | 2.2 | 1.96 | 1.7 | 10.4 | 9.9 | 8.2 | 9.2 |
| TN3 | 1.8 | 1.5 | 1.2 | 7.9 | 10.6 | 8.7 | 10.2 |
| | Q4 | K12 | K13 | K14 | K23 | K24 | K34 |
| TN1 | 8.3 | 0.55 | 0.34 | 0.5 | 0.53 | 0.66 | 0.64 |
| TN2 | 8.2 | 0.62 | 0.33 | 0.48 | 0.58 | 0.64 | 0.6 |
| TN3 | 6.5 | 0.63 | 0.3 | 0.45 | 0.57 | 0.6 | 0.54 |

Where, $L_i$ is ith inductor, $M_{ij}$ is the mutual inductances between ith and jth inductors. Manipulating the equations (2)-(5), $I_i$ (i=1, 2 ...) has been calculated versus $I_{out}$ , thus, the efficiency equation (1) would be independent of currents amount. Maximum efficiency is obtained by taking the derivative with respect to inductance amount, but the inductances size in proposed transformer are dependent to each other. In fact, all inductances and their resistances size depends on outer length and metal widths. Calculating a closed-form equation for power efficiency after taking the derivative with respect to outer length and the width of traces is very difficult. Therefore, a sweep of outer dimension and the width of traces are carried out to ascertain the best operating point for maximal efficiency in equation (1). Fig. 3 and Fig.4 show the efficiency versus metal widths and outer length. Metal width for the secondary side is constant (metal width= 20 um) and for the primary side was chosen 20, 40 and 60 um. The authors have published more details about equations and methods in [18].

## IV. EM-SIMULATION OF PROPOSED TRANSFORMER NETWORK

It is important to accurately predict the characteristics and performance of the output transformer because it is the most crucial component in this circuit: transforming impedance, converting differential signals to single-ended, combining output power, and having relation with operating frequency. The main geometric parameters such as outer length and metal widths extracted from previous simulations are used in layout style. The layout in ADS is simulated and s-parameter matrix is generated, which contains sufficient information to characterize each individual component. It should be noted that a large ratio of line width to line

Table 3. Transformer network characteristics of Fig. 2(a)

| | L1(nH) | L2(nH) | L3(nH) | L4(nH) | Q1 | Q2 | Q3 |
|---|---|---|---|---|---|---|---|
| TN1 | 3 | 2.8 | 6.6 | 19.9 | 7.4 | 6.3 | 5.8 |
| TN2 | 2.23 | 1.97 | 4 | 14 | 9.7 | 7.8 | 6.8 |
| TN3 | 1.79 | 1.48 | 2.34 | 9.39 | 10.5 | 8.24 | 8.4 |

| | Q4 | K12 | K13 | K14 | K23 | K24 | K3 |
|---|---|---|---|---|---|---|---|
| TN1 | 7.3 | 0.55 | 0.35 | 0.48 | 0.49 | 0.62 | 0.7 |
| TN2 | 6.87 | 0.62 | 0.3 | 0.45 | 0.51 | 0.61 | 0.6 |
| TN3 | 5.89 | 0.62 | 0.26 | 0.43 | 0.49 | 0.57 | 0.6 |

Table 4. Transformer network characteristics of Fig. 2(b)

| | Ll | L2 | L3 | L4 | L5 | Q1 | Q2 |
|---|---|---|---|---|---|---|---|
| TN1 | 3.1 | 2.8 | 3.03 | 2.77 | 16.2 | 8.03 | 7.2 |
| TN2 | 2.36 | 2.07 | 2.33 | 2.03 | 13.4 | 10.8 | 9.86 |
| TN3 | 1.93 | 1.62 | 1.93 | 1.6 | 11.3 | 12.1 | 10.7 |

| | Q3 | Q4 | Q5 | K12 | K13 | K14 | K15 |
|---|---|---|---|---|---|---|---|
| TN1 | 7.93 | 7.2 | 8.3 | 0.44 | 0.02 | 0.01 | 0.38 |
| TN2 | 10.9 | 9.54 | 7.1 | 0.44 | 0.03 | 0.01 | 0.37 |
| TN3 | 12 | 10.3 | 5.97 | 0.42 | 0.03 | 0.02 | 0.34 |

| | K23 | K24 | K25 | K34 | K35 | K45 |
|---|---|---|---|---|---|---|
| TN1 | 0.01 | 0.004 | 0.49 | 0.43 | 0.37 | 0.47 |
| TN2 | 0.014 | 0.004 | 0.48 | 0.43 | 0.35 | 0.45 |
| TN3 | 0.01 | 0.004 | 0.46 | 0.42 | 0.33 | 0.43 |

spacing is desirable in order to maximize the coupling between adjacent micro-strip lines in the spiral inductor. Generally, the maximum quality-factor value is more technology than geometry dependent, and hence, the absolute sheet resistance and thickness values highly affect the results of the quality-factor value. On the contrary, inductance values are more geometry dependent and hence the absolute sheet resistance and thickness values less affect the results of the inductance values for a wide range of IC technologies.

The quality factor Q can be expressed by the ratio between the imaginary and real part of the input impedance when other port is opened or shorten.

$$Q_1 = \frac{imag(Z_{11})}{real(Z_{11})}\bigg|_{i2=0} = \frac{imag(1/Y_{11})}{real(1/Y_{11})}\bigg|_{v2=0}$$

$$Q_2 = \frac{imag(Z_{22})}{real(Z_{22})}\bigg|_{i1=0} = \frac{imag(1/Y_{22})}{real(1/Y_{22})}\bigg|_{v1=0} \qquad (6)$$

The inductance can be extracted from the input resistance when other port is opened or shorten.

$$L_1 = \frac{imag(Z_{11})}{\omega}\bigg|_{i2=0} = \frac{imag(1/Y_{11})}{\omega}\bigg|_{v2=0} \qquad (7)$$

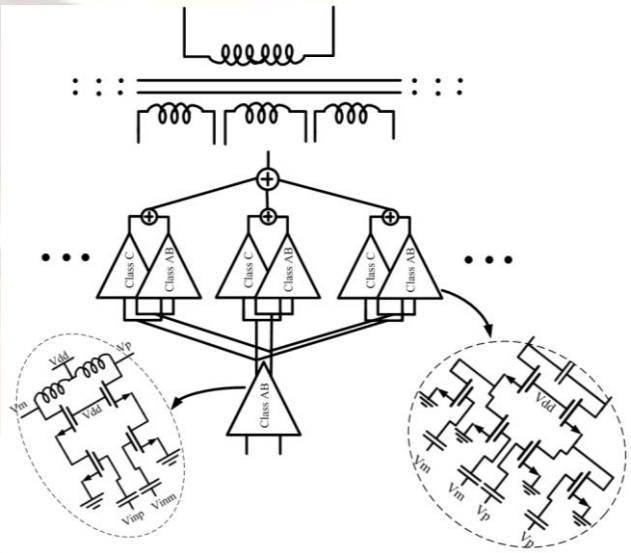



Fig. 7. Circuit schematics of the Power Amplifier

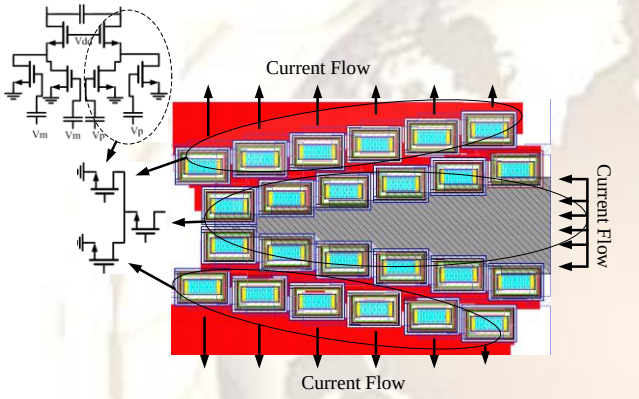
$$L_2 = \frac{imag(Z_{22})}{\omega}\bigg|_{i1=0} = \frac{imag(1/Y_{22})}{\omega}\bigg|_{v1=0}$$

The magnetic coupling between the windings is expressed by the mutual inductance M. alternatively, from the specification of the mutual inductance, it is possible to define a coupling coefficient k. It represents the strength of coupling between the primary and secondary winding.

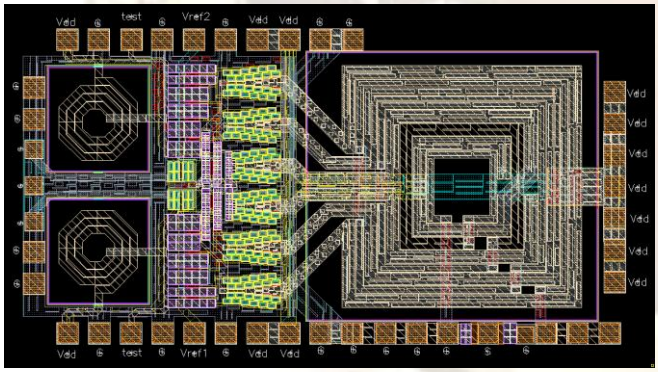
$$M = \frac{imag(Z_{12})}{\omega} \qquad K_{12} = \frac{M}{\sqrt{L_1 L_2}} \qquad (8)$$

Simulations of transformer networks with same outer length and same metal width for the secondary side and metal width 20, 40 and 60 um for the primary side are compared in Fig. 5 and Fig. 6 as a function of frequency. Summarizing, the parameters of first inductor for each transformer network are illustrated in Fig. 5 and Fig. 6. Parameters are simulated in a frequency range between f=100MHz and f=6GHz. Fig. 5 and Fig. 6 show that the self-inductance below 6 GHz increases as the widths of the inner coils decrease due to the increase in inner diameter as well as magnetic flux linkage.

The quality factor dependency on frequency is caused by the influence of the parasitic resistance and capacitance. At low frequency, quality factor is determined by the series resistance of inductor turns while at higher frequency skin effect reduces the effective area for the current flow and thus increase the heat dissipation losses. Beyond self-resonate frequency, the value of inductors become negative, they change into capacitances, and thus coupling coefficients lose their physical meaning. In other words, at the high frequency, the phenomenon of the current crowding and substrate loss will be revealed by the parasitic resistance and capacitance which will reduce the quality factor and the self-resonant frequency of the inductor. As a result, the multi-layer shunt and pattern ground shield can be used to improve the quality factor of the inductor in the silicon technology. Fig. 5 and Fig. 6 show that the quality factor of each inductor below self-resonate frequency decreases as the




(a)



(b)

Fig. 8. (a) Layout diagram of Power Stage (b) Layout diagram of Power Amplifier

widths of the inner coils decrease due to the increase in inner diameter. In addition, compared to different transformer network, the quality factor of each inductor as well as self-resonate frequency decreases as the inner diameter of the transformer network decrease.

The extracted values for transformer lumped model parameters in 1 GHz operating frequency illustrated in Fig. 5 and Fig. 6 are listed in Table 1 to Table 4. Three designs are considered here having the following physical dimensions. In the Transformer Network 1, TN1, outer length = 900 um, the metal width of the primary side = 20 um and the metal width of the secondary side = 20 um, respectively. In the Transformer Network 2, TN2, outer length = 900 um, the metal width of the primary side = 40 um and the metal width of the secondary side = 20 um, respectively. In the Transformer Network 3, TN3, outer length = 900 um, the metal width of the primary side = 60 um and the metal width of the secondary side = 20 um, respectively.

## V. POWER AMPLIFIER DESIGN

A schematic of the designed PA is shown in Fig. 7. In order to achieve sufficiently large power gain, power amplifier was designed to have two stages, driver stage and power stage, with approximately 20 dB of power gain. The driver stage is biased in class AB mode to obtain good linearity. The DC power supply voltage is provided to the amplifier via the mid-point of the primary slab inductors (a virtual

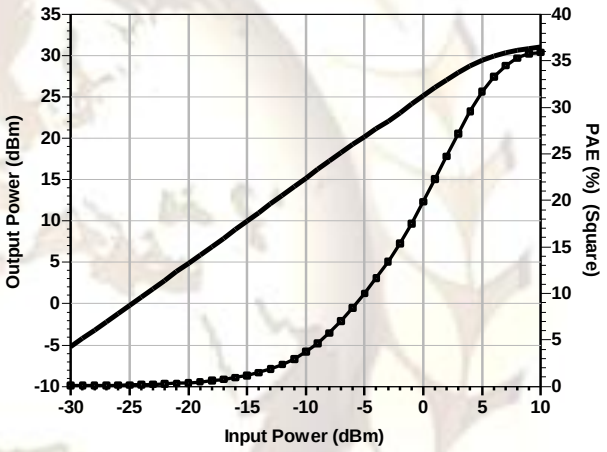



Fig. 9. Output power and PAE simulation result

ground). Therefore, the transformer functions as a matching network as well as a radio frequency (RF) chock.

Since this DC voltage appears directly at the drain of the drive transistors, its maximum value is limited by transistor breakdown voltage. A cascode structure can be used to increase the supply voltages that can be tolerated by the transistors. The cascode helps by allowing a larger voltage to appear on the drain of the top transistor without degrading the device performance. Moreover, the cascode structure is used to provide isolation between the input and output and to avoid any instability and to greatly reduce the inter-modulation caused by the second-order interaction. The PA is designed with a differential structure to avoid the gain reduction due to the ground metal lines and bond-wire and to reduce the sensitivity to the noise at the supply and ground lines. For non constant-envelope modulation schemes, nonlinearity can cause severe regrowth in the spectral sidebands and an increase in the transmitted error-vector magnitude. In such cases, stringent requirements are placed on amplifier linearity. To meet the simultaneous

requirements of high linearity and reasonable efficiency, power amplifiers in non constant-envelope systems are often operated in a class-AB mode; the linearity can be superior to that in class-B or higher operation and the efficiency is superior to that in class-A operation. A parallel combination of a class AB and a class C amplifier can be used to improve both the linear operation range and the power efficiency. In a parallel class AB&C amplifier, the class AB amplifier is the primary transconductance contributor at low signal levels; however, the class C amplifier is the primary contributor at high signal levels, with the result that the class C amplifier can compensate for the compression of the class AB amplifier when they are combined with the appropriate ratio.

The partial layout diagram of power stage is illustrated in Fig. 8a. In this layout, 6 transistor cells as down transistor and 12 transistor cells as up transistor are connected in parallel. Observing the layout, the drain is arranged above and the source is located below. The drain current flows downward to the source and is allocated by all the transistor cells. Therefore, the current flowing in the metal line of the drain has the largest value only at the top of the layout and decreases on the way. Oppositely, the source current flowing in the metal line of the source is still relatively small on top, but it increases downwards. The largest value of it exists at the bottom of the layout. Therefore, the largest width of the metal line for the drain is only necessary on the top of the transistor layout, which is reduced top down. On the other side, the line width for the source can start at the top with a very small value; however, it increases top down up to the largest width at the bottom of the transistor layout.

The layout diagram of the fully integrated PA with differential input and single-ended output is shown in Fig. 8, occupying an area of 2.5 mm* 1.3 mm, including bond pads. New proposed inductors are used for power stage and two inductors prepared by the foundry were used for driver stage. The inductors in power stage and in driver stage were laid out as far as possible to reduce magnetic coupling between them. The center of the differential inductors in the power stages was placed in same direction to save die area. The post layout simulated output power and PAE results are shown in Fig. 9. The maximum output power is over 29 dBm and the maximum PAE is over 35%.

## VI. CONCLUSION

In this paper a new transformer combination for power combiner block was presented. The proposed structure is easily extendible to the higher output power. Depends on desired output power, the design methodology of power combiner based on transformer type was demonstrated in this paper. To maximize the power efficiency, the physical dimension of transformers was obtained by mixing the analytical and numerical methods. The choice of layout style is tightly correlated with the technology features which the transformer is to be implemented with. To extract accurate pi-model component values, the layout prepared according to the result of MATLAB simulation will be simulated again using the Momentum EM-solver in RF mode.

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