

## Leakage Power Reduction Techniques: A New Approach

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### ABSTRACT

Exceeding Leakage power has become a major concern for the CMOS circuits in deep sub-micron process. As process moves to finer technologies, there is a decrease in the feature sizes and increase in the device density. Lowering the supply voltage leads to lower threshold voltages and oxide thickness. High device density and low threshold voltages result in a significant increase in the leakage power dissipation. The main objective of this paper is to first extensively study the existing Leakage reduction techniques and compare them in terms of ability to reduce leakages and their associated delay overhead. In addition, several combinations of drain gating and power gating are discussed. In the end a new approach of combining different leakage reduction techniques in a single design in accordance to incur minimum delay overhead is proposed and feasibility issues with depending on the path's nature of criticality has been discussed. Extensive SPICE simulation results were reported using 180nm and 45nm process technologies. Significant power reduction is achieved with zero or little increase in the critical path delay of the overall circuits.

**Keywords** –critical path, delay overhead, leakage power consumption, power gating, path delay

### 1. INTRODUCTION

Increase in the transistor speed and number of transistors result in high performance in the current generation processors. The performance improvements have been accompanied by an increase in the power dissipation. High power dissipation systems increase cost of cooling and reduce the system reliability. Two principal sources of power dissipation in modern processors are static power and dynamic power.

Static leakage power dissipation occurs due to the current flowing through the transistors in the idle state. Leakage power dissipation depends on threshold voltage, gate size and oxide thickness. Components of static power dissipation are junction leakage, sub-threshold leakage, gate-oxide leakage, gate induced drain leakage, punch through leakage and hot carrier injection.

Dynamic leakage power dissipation occurs due to Switching power dissipation in a circuit results from charging/discharging the output load capacitance to supply/ground voltage. Dynamic power depends on switching current, short circuit current.

In this paper, we will first conduct experimental analysis on existing leakage power reduction techniques and Their comparative results using 180nm, 100nm and 45nm process technologies. We propose and discuss the method of using different leakage reduction mechanisms in a single circuit depending on the suitability of the technique with the path criticality. Next we discussed the issue of area overhead due to the increase in number of transistors hence the increased cell size and also proposed a possible solution for it.

The rest of the paper is organized as follows. In Section 2

Previous works regarding existing leakage power reduction techniques have been discussed. In Section 3 the drain gating technique and its variations are described. In Section 4, experimental results of the drain gating technique and its variations are presented, followed by a description of the proposed overall low-power circuit design procedure utilizing the proposed selective gating methodology in accordance to the path criticality for reducing leakage power consumption. In Section 5 we discuss the possible solution for reducing area overhead due to the enhanced cell sizes. Finally section 6 concludes the paper.

### 2. RELATED WORK

In this section, we briefly review existing leakage power reduction techniques.

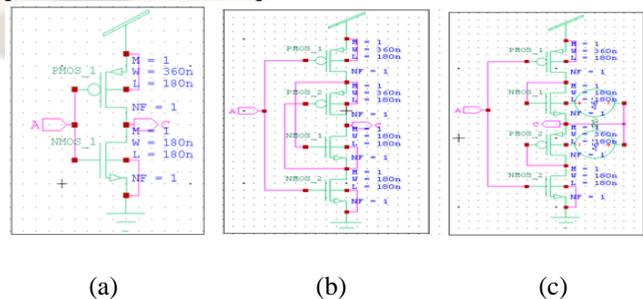


Fig1(a)original not gate. (b)LECTOR not gate. (c)GALEOR not gate.

2.1 LECTOR technique uses two extra transistors (a p-type and a n-type) called leakage control transistors (LCTs ) inserted in series between pull-up network and pull- down network in each CMOS gate as shown in Fig.1(b) In this arrangement, one of the LCTs is always “near its cutoff voltage” for any input combination. This increases the resistance of the path from Vdd to ground, thereby decrease in leakage currents. The significant feature of LECTOR is that it works effectively in both active and idle states of the circuit, resulting in better leakage reduction. The basic idea behind the approach for reduction of leakage power is the effective stacking effect of transistors in the path from supply voltage to ground.

2.2 GALEOR technique uses two extra transistors (a n-type and a p-type) called gated leakage transistors (GLTs) inserted in series between pull-up network and pull- down network in each CMOS gate as shown in Fig. In this technique high threshold voltage used for gated leakage transistors. Transistor states and stacking effect introduced by the transistors in a GALEOR implemented gate family for all possible input combinations.

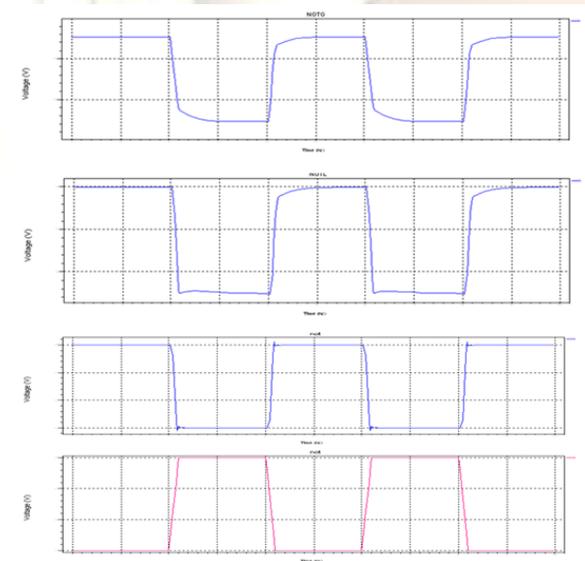


Fig.2 Transient characteristics of ORIGINAL not, LECTOR not, GALEOR not gate simulation.

When we used these techniques LECTOR & GALEOR then voltages of the output wave forms suffered a significant problem. That is, the low signal is very much higher than 0 volt in addition, GALEOR causes high signal much lower than the Vdd. Such phenomena

can make the use of both techniques infeasible. The output wave form as shown in fig.2 the low signal is 0.2v for both LECTOR & GALEOR and the high signal for GALEOR is 1.3V, rather than 0V and 1.5V, respectively. Similar troubling behaviors are consistently observed for all other gate types such as OR, AND, XOR.

### 3. DRAIN GATING TECHNIQUES

In previous two techniques the output voltage level is not exactly same as input voltage level, for removing this problem drain gated technique is used. The proposed circuit family, which will be described in this section, is capable of maintain the original signal quality and avoiding problem. It reduces the leakage current by inserting extra sleep transistors between pull-up and pull-down networks. As shown in Fig. 3 (a), a PMOS sleep transistor (S) is placed between pull-up network and network output and an NMOS sleep transistor(S') is placed between network output and pull-down network.

During active mode, both sleep transistors are turned on so resistance of conducting paths is reduce, thereby reducing performance degradation. During standby mode, both sleep transistors are turned off mode, and produce stacking effect which reduces leakage current by increasing resistance of the path from power supply to ground. By applying two turned-on sleep transistors in active mode, drain gating produces exact logic levels due to less resistance of the path from Vdd to ground than LECTOR and GALEOR which always have one turned-on LCT/GLT and the other near cutoff region LCT/GLT, thus preventing exact logic state.

The drain gating technique & its variations were tested pn various gates. There are three combinations of Power Gating, Drain-Header & Power-Footer Gating (DHPF) and Drain-Footer & Power-Header Gating (DFPH).

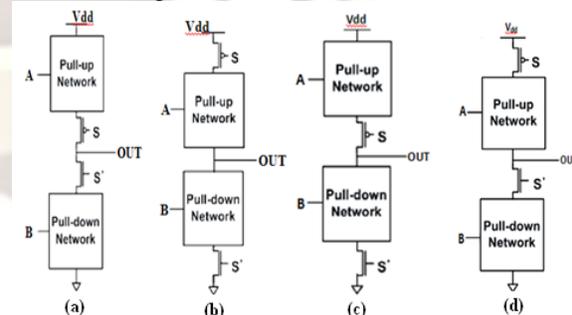


Fig. 3 (a) Drain Gating. (b) Power Gating (c) Drain-Header & Power-Footer Gating (DHPF) (d) Drain-Footer & Power-Header Gating (DFPH).



Fig. 4 Drain gating output waveforms

#### 4. SIMULATION AND RESULTS

Simulations were conducted on various gates and static leakage power and dynamic leakage power measured by Tanner Tool. Two different process technologies (180nm 100nm, and 45nm) from latest version (2.0) of PTM were used in Tanner Tool simulations. Analysis of the results shows that after lector, drain header gating technique has the least propagation delay, while the power gating has the best savings in leakage power reduction due to the location of sleep transistors which are located outside the network, thereby creating more stacking effect. According to delay analysis critical path is decided, Gates in the absolute non-critical groups will always use power gating. For the slightly non-critical and average non-critical, a mixture of power gating and others will be used. Experiments have shown that reduced power consumption is achieved with little or no increase in critical path delay for the whole circuit.

TABLE 1 STATIC POWER (180 NM)

180 nm Process technology, supply voltage=1.5V		
NOT gate	Leakage Power (W) of input Vector	
	0	1
Original	1.2729e-10W	3.39357e-10W
Lector	1.06416e-10W	3.12449e-10W
Galeor	4.4621e-10W	2.45384e-10W

TABLE 2 PERSANTAGE POWER SAVING

IN PUT	% SAVING LECTOR	% SAVING GALEOR
0	16.4	64.95
1	7.93	27.69

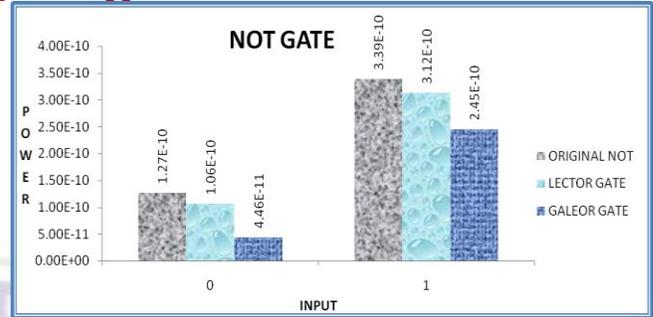


Fig. 4 static power comparison

TABLE 3 DYNAMIC POWER (180 NM)

180 nm Process technology, supply voltage=1.5V		
NOT gate	Leakage Power (W) of input Vector	
	0→1	1→0
Original	1.947267e-7W	2.390681e-7W
Lector	1.626406e-7W	1.743562e-7W
Galeor	1.369424e-7W	1.411925e-7W

TABLE 4 PERSANTAGE POWER SAVING

IN PUT	% SAVING LECTOR	% SAVING GALEOR
0→1	16.48	29.67
1→0	27.07	40.94

TABLE 5 STATIC POWER COMPARISON (100nm)

INPUT AB	NAND GATE	LECTOR NAND	GALEOR NAND	DG NAND	PG NAND	DHPF NAND	DPPH NAND
00	2.66E-10	1.98E-10	1.82E-10	9.84E-11	9.84E-11	9.84E-11	9.84E-11
01	9.70E-09	5.12E-09	2.66E-09	1.84E-10	1.84E-10	1.84E-10	1.84E-10
10	7.28E-09	4.97E-09	2.66E-09	1.84E-10	1.84E-10	1.84E-10	1.84E-10
11	6.53E-09	2.47E-09	1.23E-09	9.69E-11	9.69E-11	9.69E-11	9.69E-11

TABLE 6 DELAY COMPARISON

NAND	(TWO INPUT)	(THREE INPUT)	LECTOR	GALEOR	DG	PG	DHPF	DPPH	FG	HG
DELAY(NS)	0.13	0.205	0.075	0.165	0.16	0.205	0.15	0.195	0.165	0.145

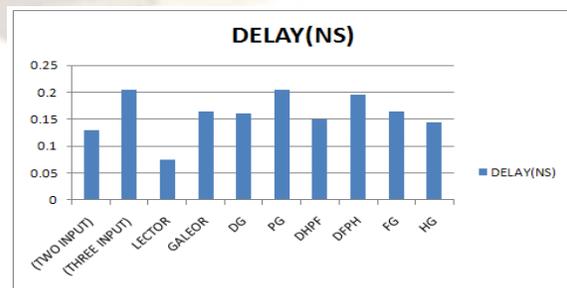


Fig. 5 delay comparison

TABLE 7 DYNAMIC POWER COMPARISON (180nm)

NAND	(TWO INPUT)	(THREE INPUT)	LECTOR	GALEOR	DG	PG	DHPF	DFPH	FG	HG
POWER (W)	1.57E-06	1.98E-06	1.20E-06	9.95E-07	1.40E-06	1.36E-06	1.43E-06	1.42E-06	1.54E-06	1.38E-06

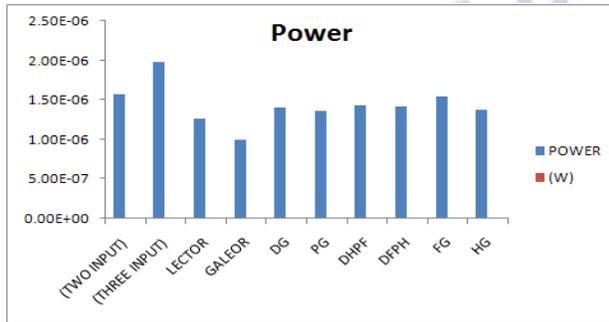


Fig. 6 dynamic power comparison

TABLE 8 STATIC POWER COMPARISON (180nm)

180nm process technology, supply voltage=1.5v				
NAND GATE	leakage power (w)of input vector			
	00	01	10	11
ORIGINAL 2 I/P	1.20E-11	2.52E-10	2.09E-10	3.44E-10
LECTOR	1.16E-11	2.10E-10	2.02E-10	3.23E-10
GALEOR	1.09E-11	9.68E-11	1.01E-10	2.48E-10
POWER GATED	9.17E-12	1.76E-11	1.75E-11	7.42E-11
DRAIN GATED	9.17E-12	1.76E-11	1.76E-11	7.36E-11
DFPH	9.17E-12	1.76E-11	1.76E-11	7.42E-11
DHPF	9.17E-12	1.76E-11	1.75E-11	7.36E-11

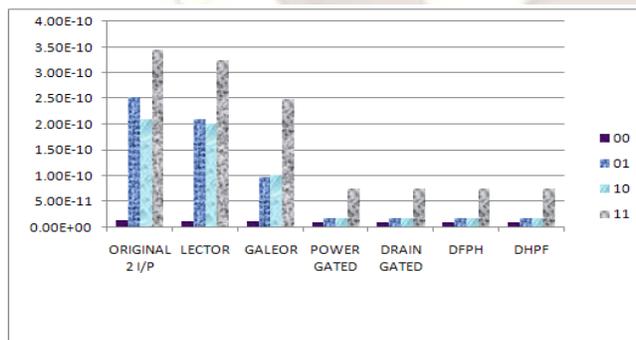


FIG. 7 STATIC POWER COMPARISON

## 5. PATH SELECTION TECHNIQUE TO COMPENSATE DELAY OVERHEAD

After the detail analysis of the above experimental results, It has been found that the techniques which provide lesser leakage and dynamic power dissipations have much higher delay penalties. Power gating, Power header and Power footer techniques have consecutively lesser power dissipation and higher delay overhead.

Therefore we propose to design a circuit with a mixture of them. Circuits along critical path will first use only original circuit types. Then gates along critical paths are analyzed to measure their criticality. Gates with low criticality will be considered to be replaced with drain-gating based gates as long as the critical path delays are within acceptable range. Gates not along critical paths are then analyzed and divided into a number of groups (such as slightly non-critical, average non-critical, and absolute non-critical). Gates in the absolute non-critical groups will always use power gating. For the slightly non-critical and average non-critical, a mixture of power gating and others will be used. Through a number of design iterations, highly optimized circuit type can then be determined for each gate. Experiments have shown that reduced power consumption is achieved with little or no increase in critical path delay for the whole circuit.

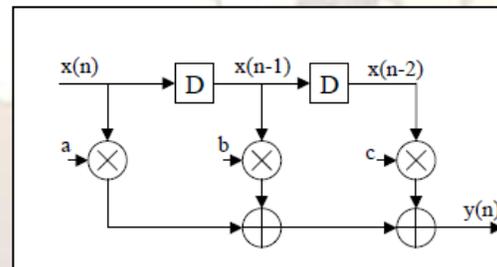


Fig. 7 A 3-tap FIR filter

Consider a 3-tap FIR filter:  $ax(n)+bx(n-1)+cx(n-2)$ . The critical path (or minimum time required for processing a new sample) is limited by 1 multiply and 2 add times. Thus, this path should include only original logic cells. The other two paths can be categorized as slightly non-critical and average non-critical and a suitable power gating technique can be used in accordance with the allowed delay penalty.

## 6. PROPOSED APPROACH FOR BALANCED CELL LAYOUT

The extra transistors used in leakage power reduction techniques have an obvious extra overhead and also leads to an unbalanced layout of the cell. This

extra area overhead further increases the overall chip power dissipation, since there is a direct relationship between chip power per unit area and chip area. The entire purpose of this low power design will be mitigated due to the above issue.

To resolve this we propose to use a new process technology, based on the following studies on strained silicon technologies. NMOS transistors have traditionally been 2-3 times faster than PMOS transistors. This large ratio gap is primarily due to the inherent mobility difference between electrons and holes. However, process scaling over the last few generations has significantly slowed down this trend thanks to advances in strained silicon engineering. First introduced in the 90nm node, new strain innovations compress (stretch) the silicon crystal lattice inducing higher mobility of holes (electrons) moving through the channel. The strained silicon approach to improving drive current comes with a much lower impact on sub-threshold leakage ( $I_{OFF}$ ) current compared to the traditional method of reducing threshold voltage ( $V_{TH}$ ). Fourth generation strained silicon used in the 32nm node continues to use strain enhancement techniques that are more useful for PMOS than NMOS. In the PMOS case, increasing the Ge concentration in the SiGe stressor to ~40%, proximity reduction of the SiGe stressors to the channel, and increased effectiveness of the SiGe stressors in the gate-last flow result in a 28% increase in  $I_{DSATP}$  over the 45nm technology. On the other hand, straining the NMOS using contact fill and metal gate stressors gives only a 19% increase in  $I_{DSATN}$ . As a result, the ratio of  $I_{DSATN}$  to  $I_{DSATP}$  in the 32nm node is 1.18, implying that circuit designers can use smaller PMOS devices in CMOS logic design. Significant results-We can build a symmetric layout since no. of pmos and nmos are equal in size, hence a balanced layout.

## 7. CONCLUSION

In this paper, we thoroughly discussed the techniques used in reducing leakage power consumption. We then elaborated a circuit design methodology for reducing leakage current. Based on the experimental investigation on static power and dynamic power consumption of the circuit family, Experiments using 180nm, 100nm and 45nm process technologies have shown that the proposed technique is capable of reducing significant leakage power consumption. These techniques are feasible for the design of every other cell like ex-or gate & other combined functional gates. All different functions and other cells can be used for the

library development of the tools. This will lead to easier design of larger circuits.

During the Analysis of all these techniques we found that power dissipations have reduced but the area and delay overheads have also increased significantly. The possible solutions of reducing these were discussed. In this paper we proposed the use of strained silicon in place of silicon. This shows better results in designing balanced layout of the CMOS logic family circuits.

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